

bq2430x/1x/8x DSG EVM (HPA245) for Li+ Charger Front-End Protection IC

The bq2430x/1x/8x evaluation module is a complete charger module for evaluating a charger front-end protection and charger solution using the bq2430x/1x/8x and bq24080 devices. This user's guide presents test summary information, printed-circuit board layout guidelines, bill of materials, board layout, and schematics.

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1 Introduction

1.1 EVM Features

- Evaluation module for bq2430x, bq2431x, and bq2438x DSG
- Evaluation module for bq24080 charger integrated circuit (IC)
- Evaluation module for bq2430x/1x/8x and bq24080 chipset solution
- Input operating range for bq2430x/1x/8x 4.5 V–26 V
- Input operating range for bq24080 4.5 V–6.5 V
- Input overvoltage protection
- Input overcurrent protection
- Battery overvoltage protection
- Input reverse voltage protection for bq2430x
- LED indication for status signals
- Test points for key signals available for testing purpose. Easy probe hook-up
- Jumpers available. Easy to change connections

1.2 General Description

The bq2430x/1x/8x evaluation module is a complete charger module for evaluating a charger front-end protection and charger solution using the bq2430x/1x/8x and bq24080 devices. It is designed to deliver up to 200 mA (bq2430x) or 700 mA (bq2431x/8x) of charge current to Li-ion or Li-polymer applications. The charger front-end protection current is designed to 300 mA (bq2430x) or 1000 mA (bq2431x) or no limit (bq2438x).

The bq2430x/1x/8x protects the charging system against three types of failures: input overvoltage when the AC adapter fails to regulate its voltage; load overcurrent when failures such as a short-circuit occurs in the charging system; and battery overcharge.

In addition, bq2430x provide a PFET gate drive signal to an external PFET for input reverse-polarity protection.

For details, see the relevant bq2430x/1x/8x data sheet.

1.3 I/O Description

Jack	Description
J1-DC+	AC adapter, positive output
J1-DC-	AC adapter, negative output, ground
J2-OUT	CFE OUT pin
J2-DC-	CFE VSS pin, ground
J2-BAT+	Connect to battery positive output
J2-FAULT	CFE FAULT pin
J3-CHGIN	bq24080 IN pin, connect to external power supply positive output
J3-DC-	bq24080 VSS pin, ground
J4-BAT+	Connect to battery positive output
J4-BAT-	Connect to battery negative output, ground

1.4 Controls and Key Parameters Setting

Jack	Description	Factory Setting
JMP1	CFE input voltage is indicated by LED.	Jumper On
JMP2	CFE output voltage is indicated by LED.	Jumper On
JMP3	CFE $\overline{CE}$ pin is connected to 5 V.	Jumper On
JMP4	bq24080 STAT1 pin is indicated by LED.	Jumper On
JMP5	bq24080 STAT2 pin is indicated by LED.	Jumper On
JMP6	bq24080 $\overline{PG}$ pin is indicated by LED	Jumper On
JMP7	bq24080 $\overline{CE}$ pin is connected to 5 V.	Jumper On
JMP8	CFE OUT pin is connected to bq24080 IN pin.	Jumper Off

1.5 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
Supply voltage, V_{IN}	Input voltage from ac adapter input	4.5	5	26	V	
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal of J4	0	3-4.2	5	V	
Supply current, I_{AC}	Maximum input current from ac adapter input	0		1.5	A	
Charge current, I_{chg}	Battery charge current	0.02–0.07	0.2–0.7	1	A	
Operating junction temperature range, T_J		0		125	°C	

2 Test Summary

2.1 Definitions

This procedure details how to configure the evaluation board. On the test procedure, the following naming conventions are followed. See

the schematic for details.

VXXX :	External voltage supply name (VIN, VBAT, VOUT)
LOADW:	External load name (LOADR, LOADI)
V(TPyyy) :	Voltage at internal test point TPyyy. For example, V(TP1) means the voltage at TP1.
V(Jxx):	Voltage at jack terminal Jxx.
V[TP(XXXXX)]:	Voltage at test point XXXXX. For example, V(ACDET) means the voltage at the test point which is marked as <i>ACDET</i> .
V(XXX, YYY):	Voltage across point XXX and YYY.
I[JXX(YYY)]:	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON :	Internal jumper Jxx terminals are shorted
Jxx OFF:	Internal jumper Jxx terminals are open
Jxx (-YY-) ON:	Internal jumper Jxx adjacent terminals marked as YY are shorted
Measure:	A,B Check specified parameters A, B. If measured values are not within specified limits, the unit under test has failed.
Observe:	A,B Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points, and individual components.

2.2 Equipment

2.2.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 20 V at 2 A is required.

Power Supply #2 (PS#2): a power supply capable of supplying 5 V at 1 A is required.

2.2.2 Load #1

A 10-V (or above), 2-A (or above) electronic load that can operate at constant current mode.

2.2.3 Load #2

A 10-V (or above), 2-A (or above) electronic load that can operate at constant voltage mode.

2.2.4 Meters

Four Fluke 75 multimeters, (equivalent or better)

Or: Three equivalent voltage meters and one equivalent current meter. The current meters must be capable of measuring 2-A+ current.

2.2.5 Wire Gauge

All wires connected to EVM input power supply and output load should use at least AWG 22. The maximum current is up to 1 A.

2.3 Equipment Setup

(A) Set the power supply #1 for 0 V $\pm$ 100 mVDC, 2 $\pm$ 0.1-A current limit and then disable the output.

(B) Connect the output of power supply #1 to J1 (DC+, DC-)

- (C) Connect a voltage meter across J1 (DC+, DC-).
- (D) Set the power supply #2 for 3.7 V $\pm$ 100 mVDC, 0.2 $\pm$ 0.1-A current limit and then disable the output.
- (E) Connect power supply #2 to J2 (BAT+, DC-).
- (F) Connect a voltage meter across J2 (BAT+, DC-).
- (G) Connect the output of the Load #1 in series with a current meter (multimeter) to J2 (OUT, DC-).
Ensure that a voltage meter is connected across J2 (OUT, DC-). Turn on the power of the Load #1.
Set the load current to 0.2 A $\pm$ 50 mA but disable the output.
- (H) JMP1: ON, JMP2: ON, JMP3: ON, JMP4: ON, JMP5: ON, JMP6: ON, JMP7: ON, JMP8: OFF.
- After the preceding steps, the test setup for HPA245 (bq2430x/1x/8x DSG EVM) is shown in [Figure 1](#).

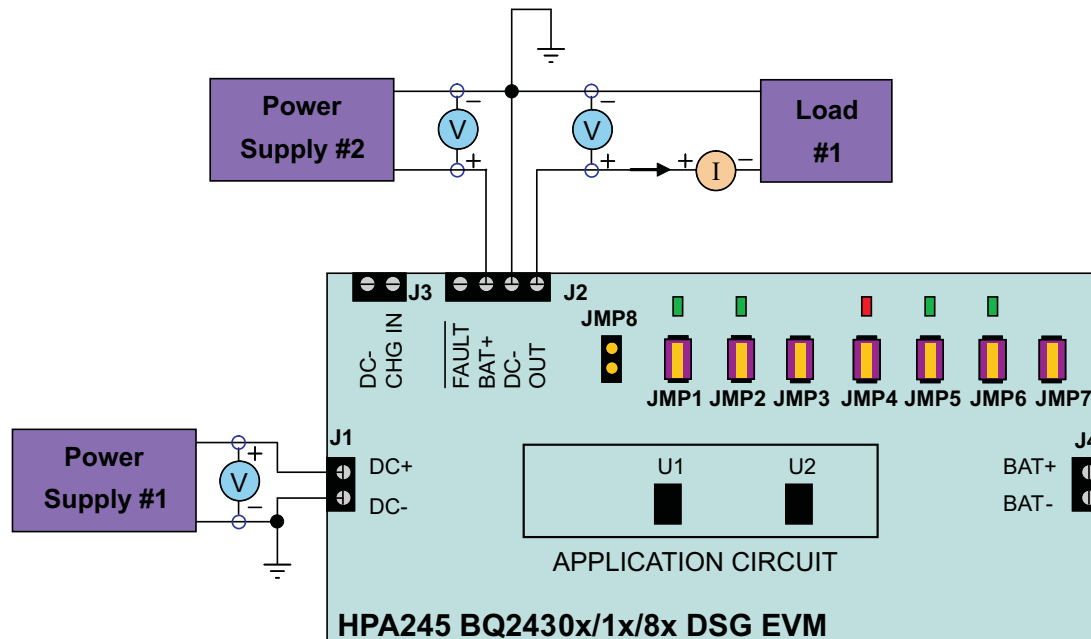


Figure 1. Original Test Setup for HPA245 (bq2430x/1x/8x DSG EVM)

2.4 Procedure

2.4.1 CFE ENABLE and Voltage Regulation

1. Ensure that the preceding Equipment Setup steps are followed.
2. Enable output of PS#2.
3. Enable output of PS#1.
4. **(For HPA245-001, -002, -003, -004, -009, -010, -013 only)** Increase the output voltage of PS#1 to 6 V $\pm$ 0.1 V.
Measure $\rightarrow$ V(J2(OUT)) = 0 V $\pm$ 500 mV
Observe $\rightarrow$ D2 on, D3 off.
5. **(For HPA245-005, -006, -007, -008, -011, -012 only)** Increase the output voltage of PS#1 to 5 V $\pm$ 0.1 V.
Measure $\rightarrow$ V(J2(OUT)) = 0 V $\pm$ 500 mV
Observe $\rightarrow$ D2 on, D3 off.
6. Uninstall JMP3 (enable U1).
Measure $\rightarrow$ V(J2(OUT)) = 5.5 V $\pm$ 200 mV **(For HPA245-001, -002, -009 only)**
Measure $\rightarrow$ V(J2(OUT)) = 4.5 V $\pm$ 200 mV **(For HPA245-003 only)**
Measure $\rightarrow$ V(J2(OUT)) = 5 V $\pm$ 200 mV **(For HPA245-004, -005, -006, -007, -008, -010, -011, 012, -**

013 only)

Observe → D2 on, D3 on.

2.4.2 CFE Input Overvoltage Protection

1. **(For HPA245-001, -002, -003, -004, -013 only)** Increase the voltage of PS#1 to 11V $\pm 0.1V$
Measure → V(J2(OUT)) = 0 V $\pm$ 500 mV
Observe → D2 on, D3 off.
2. **(For HPA245-005, -006, -007, -008, -009, -010, -011, -012 only)** Increase the voltage of PS#1 to 8 V ± 0.1 V.
Measure → V(J2(OUT)) = 0 V $\pm$ 500 mV
Observe → D2 on, D3 off.
3. Decrease the voltage of PS#1 to 5 V ± 0.1 V.
Observe → D2 on, D3 on

2.4.3 CFE Load Overcurrent Protection

1. **(For HPA245-009, -010, skip 2.4.3 test and go to 2.4.4 test.)**
2. Enable the output of the Load #1.
Observe → D2 on, D3 on.
3. **(For HPA245-001, -002, -003, -004, -013 only)** Increase the current of Load #1 to 0.5A $\pm 0.1A$
Observe → D2 on, D3 off.
4. **(For HPA245-005, -006, -007, -008, -011, -012 only)** Increase the current of Load #1 to 1.2 A ± 0.1 A.
Observe → D2 on, D3 off.
5. Turn off Load #1.
6. Decrease the voltage of PS#1 to 0 V ± 0.1 V.

2.4.4 CFE Battery Overvoltage Protection

1. Increase the output voltage of PS#1 to 5 V $\pm 0.1V$.
Observe → D2 on, D3 on
2. Increase the voltage of PS #2 to 4.6 V $\pm 0.1V$.
Observe → D2 on, D3 off.
3. Decrease the voltage of PS #2 to 3.7 V $\pm 0.1V$.
Observe → D2 on, D3 on.
4. Turn off all the power supplies and loads. Remove all connection between test board and power supplies or loads.

2.4.5 Charge IC Test Setup

1. Set the power supply #1 for 0 V ± 100 mVDC, 2-A ± 0.1 -A current limit and then disable the output.
2. Connect the output of power supply #1 to J3 (CHG IN, DC-).
3. Connect a voltage meter across J3 (CHG IN, DC-).
4. Set the voltage of Load #2 to 3.6 V ± 0.1 V, disable output of Load #2.
5. Connect output of the Load #2 in series with a current meter (multimeter) to J4 (BAT+, BAT-). Ensure that a voltage meter is connected across J4 (BAT+, BAT-).
6. JMP1: ON, JMP2: ON, JMP3: ON, JMP4: ON, JMP5: ON, JMP6: ON, JMP7: ON, JMP8: OFF
7. After the preceding steps, the test setup for HPA245 (bq2430x/1x/8x DSG EVM) is shown in [Figure 2](#).

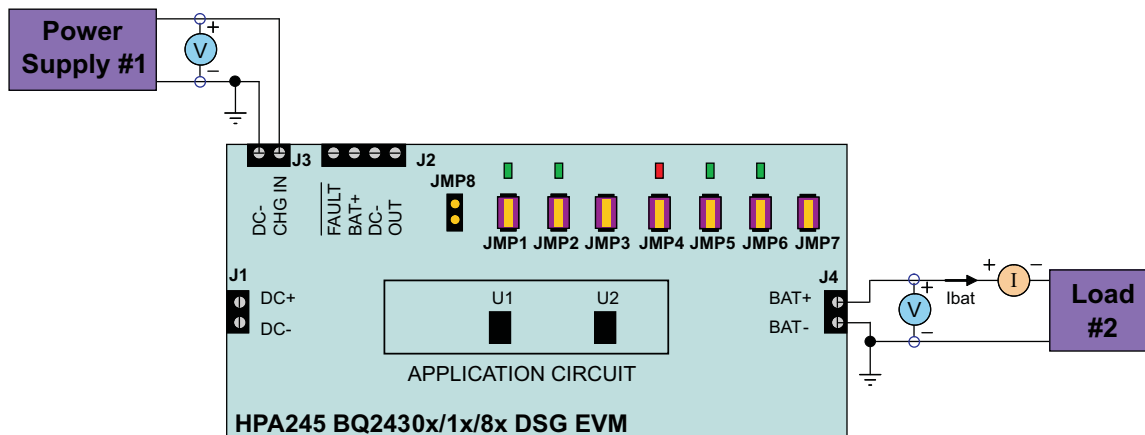


Figure 2. Charger IC Test Setup for HPA245 (bq2430x/1x/8x DSG EVM)

2.4.6 Charge IC Test

1. Enable output of Load #2
2. Enable output of PS#1
3. Increase the voltage of PS #1 to 5 V ± 0.1 V.
Observe $\rightarrow$ D4 off, D5 off, D6 on.
4. Uninstall JMP7 (enable U2).
Measure $\rightarrow$ Ibat = 200 mA ± 20 mA (**For HPA245-001, -002, -003, -004, -013 only**).
Measure $\rightarrow$ Ibat = 700 mA ± 70 mA (**For HPA245-005, -006, -007, -008, -009, -010, -011, -012 only**).
Observe $\rightarrow$ D4 on, D5 off, D6 on.
5. Disable the output of Load #2.
6. Disable the output of PS#1 and remove PS #1 from J3

2.4.7 CFE and Charge IC Chipset Test Setup

1. Connect the output of power supply #1 to J1 (DC+, DC-).
2. Connect a voltage meter across J1 (DC+, DC-).
3. JMP1: ON, JMP2: ON, JMP3: OFF, JMP4: ON, JMP5: ON, JMP6: ON, JMP7: OFF, JMP8: ON.
4. After the preceding steps, the test setup for HPA245 (bq2430x/1x/8x DSG EVM) is shown in [Figure 3](#).

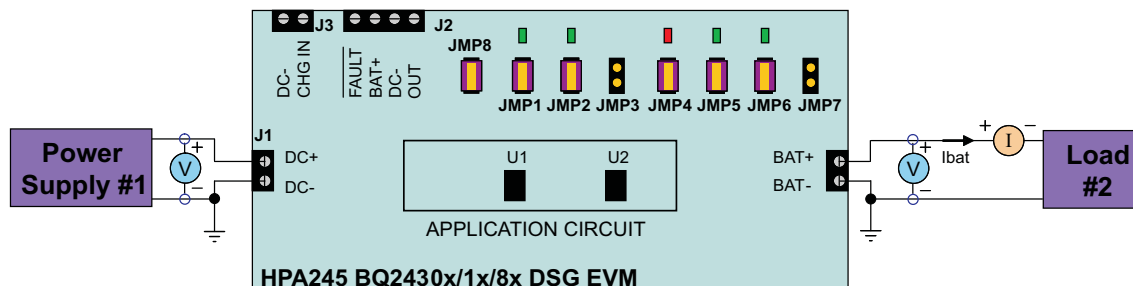


Figure 3. Chipset Test Setup for HPA245 (bq2430x/1x/8x DSG EVM)

2.4.8 CFE and Charge IC Chipset Test

1. Enable output of Load #2.
2. Enable output of PS#1.
Measure $\rightarrow$ Ibat = 200 mA ± 20 mA (**For HPA245-001, -002, -003, -004, -013 only**).

Measure → $I_{bat} = 700 \text{ mA} \pm 70 \text{ mA}$ (**For HPA245-005, -006, -007, -008, -009, -010, -011, -012 only**).

Observe → D2 on, D3 on, D4 on, D5 off, D6 on.

3 PCB Layout Guideline

1. It is critical that the exposed power pad on the backside of the bq2430x/1x/8x package be soldered to the PCB ground. Ensure that sufficient thermal vias are right underneath the IC, connecting to the ground plane on the other layers.
2. The high-current charge paths into IN and from OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
3. Decoupling capacitors for IN and OUT pins should be placed on the board and the interconnections to the IC made as short as possible.
4. Resistors for ILIM and VLIM must be placed close to the corresponding IC pins and the interconnections to the IC made as short as possible.

4 Bill of Materials, Board Layout, and Schematics

4.1 Bill of Materials — bq24300/02/04/10/14/16

b q 2 4 3 0 0 - 0 0 0 1	b q 2 4 3 0 0 - 0 0 0 2	b q 2 4 3 0 0 - 0 0 0 3	b q 2 4 3 0 0 - 0 0 0 4	b q 2 4 3 0 0 - 0 0 0 5	b q 2 4 3 0 0 - 0 0 0 6	b q 2 4 3 0 0 - 0 0 0 7	b q 2 4 3 0 0 - 0 0 0 8	RefDes	Value	Description	Size	Part Number	MFR
1	1	1	1	0	0	0	0	C1	1 μ F	Capacitor, Ceramic, 35-V, X7R, 10%	805	Std	Std
1	1	1	1	1	1	1	1	C2	1 μ F	Capacitor, Ceramic, 35-V, X7R, 10%	805	Std	Std
3	3	3	3	3	3	3	3	C3–C5	1 μ F	Capacitor, Ceramic, 16-V, X7R, 10%	805	Std	Std
1	1	1	1	1	1	1	1	D1	BZT52C5V1S	Diode, Zener, 200mW, 5.1V	SOD-323	BZT52C5V1S	General
4	4	4	4	4	4	4	4	D2, D3, D5, D6	LTST-C190GKT	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	603	LTST-C190GKT	Liteon
1	1	1	1	1	1	1	1	D4	LTST-C190CKT	Diode, LED, Red, 1.8-V, 20-mA, 20-mcd	603	LTST-C190CKT	Liteon
3	3	3	3	3	3	3	3	J1–J4	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 in	ED1514	OST
1	1	1	1	1	1	1	1	J2	ED1516	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25 in	ED1516	OST
8	8	8	8	8	8	8	8	JMP1–JMP8	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 in x 2	PTC36SAAN	Sullins
8	8	8	8	8	8	8	8	JMP1–JMP8	929950-00	Shorting jumpers, 2-pin, 100mil spacing		929950-00	3M/ESD
1	1	1	1	0	0	0	0	Q1	Si2343DS	MOSFET, Pch, –30 V, 4 A, 53 m Ω	SOT23	Si2343DS	Vishay
1	1	1	1	0	0	0	0	R1	100k	Resistor, Chip, 1/16W, 5%	603	Std	Std
0	0	0	0	1	1	1	1	R2	0	Resistor, Chip, 1/8W, 5%	1206	Std	Std
1	1	1	1	1	1	1	1	R3	20k	Resistor, Chip, 1/16W, 5%	603	Std	Std
0	0	0	1	0	0	0	0	R4	113k	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	0	0	0	1	1	1	1	R5	24.9k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	0	1	1	1	1	1	1	R6	100k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	1	1	1	1	1	1	1	R7	6.2k	Resistor, Chip, 1/16-W, 5%	603	Std	Std
1	1	1	1	1	1	1	1	R9	20k	Resistor, Chip, 1/16-W, 5%	603	Std	Std
5	5	5	5	5	5	5	5	R8, R11–R14	1.5k	Resistor, Chip, 1/16-W, 5%	603	Std	Std
0	0	0	0	1	1	1	1	R10	1.13k	Resistor, Chip, 1/16-W, 1%	603	Std	Std
1	1	1	1	0	0	0	0	R10	4.02k	Resistor, Chip, 1/16-W, 1%	603	Std	Std
0	0	0	0	1	1	0	0	R15	137k	Resistor, Chip, 1/16-W, 1%	603	Std	Std
0	0	0	0	1	1	1	1	R16	100k	Resistor, Chip, 1/16-W, 5%	603	Std	Std
1	0	0	0	0	0	0	0	U1	bq24300DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24300DSG	TI
0	1	0	0	0	0	0	0	U1	bq24302DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24302DSG	TI
0	0	1	0	0	0	0	0	U1	bq24304DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24304DSG	TI
0	0	0	1	0	0	0	0	U1	bq24308DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24308DSG	TI
0	0	0	0	1	0	0	0	U1	bq24310DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24310DSG	TI
0	0	0	0	0	1	0	0	U1	bq24312DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24312DSG	TI
0	0	0	0	0	0	1	0	U1	bq24314DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24314DSG	TI
0	0	0	0	0	0	0	1	U1	bq24316DSG	IC, Li+ Charger Front-End Protection	DSG8	bq24316DSG	TI
1	1	1	1	1	1	1	1	U2	bq24080DRC	IC, Single Chip, Li Ion/Li POL, Charger	DRC10	bq24080DRC	TI
1	1	1	1	1	1	1	1	—	HPA245	PCB, 1.2 In x 3 In x 0.031 In		PCB	Any

Notes:

- Number 0 in left side columns means do not use this component.
- OPEN in value column means do not use this component.
- Std in part number column means standard manufacturer's part number
- Std in MFR column means standard manufacturer

4.2 Bill of Materials — bq24380/1/14A/15/05

b q 2 4 3 8 0 - 0 0 9	b q 2 4 3 8 0 - 0 0 9	b q 2 4 3 8 0 - 0 0 9	b q 2 4 3 8 0 - 0 0 9	b q 2 4 3 8 0 - 0 0 9	RefDes	Value	Description	Size	Part Number	MFR
0	0	0	0	1	C1	1 μ F	Capacitor, Ceramic, 35-V, X7R, 10%	805	Std	Std
1	1	1	1	1	C2	1 μ F	Capacitor, Ceramic, 35-V, X7R, 10%	805	Std	Std
3	3	3	3	3	C3–C5	1 μ F	Capacitor, Ceramic, 16-V, X7R, 5%	805	Std	Std
1	1	1	1	1	D1	BZT52C5V1S	Diode, Zener, 200mW, 5.1V	SOD-323	BZT52C5V1S	General
4	4	4	4	4	D2,D3,D5,D6	LTST-C190GKT	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	603	LTST-C190GKT	Liteon
1	1	1	1	1	D4	LTST-C190CKT	Diode, LED, Red, 1.8-V, 20-mA, 20-mcd	603	LTST-C190CKT	Liteon
3	3	3	3	3	J1, J3, J4	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 × 0.25 inch	ED1514	OST
1	1	1	1	1	J2	ED1516	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 × 0.25 inch	ED1516	OST
8	8	8	8	8	JMP1–JMP8	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 inch × 2	PTC36SAAN	Sullins
8	8	8	8	8	JMP1–JMP8	929950-00	Shorting jumpers, 2-pin, 100mil spacing		929950-00	3M/ESD
0	0	0	0	1	Q1	Si2343DS	MOSFET, Pch, –30 V, 4 A, 53 m Ω	SOT23	Si2343DS	Vishay
0	0	0	0	1	R1	100k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	1	1	1	0	R2	0	Resistor, Chip, 1/16W, 5%	1206	Std	Std
1	1	1	1	1	R3	20k	Resistor, Chip, 1/16W, 5%	603	Std	Std
0	0	0	0	0	R4	113k	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	0	1	1	0	R5	24.9k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	1	1	R6	100k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	1	1	1	1	R7	6.2k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	1	1	1	1	R9	20k	Resistor, Chip, 1/16W, 5%	603	Std	Std
5	5	5	5	5	R8, R11–R14	1.5k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	1	1	1	0	R10	1.13k	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	0	0	0	1	R10	4.02k	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	0	0	0	0	R15	137k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	1	1	1	0	R16	100k	Resistor, Chip, 1/16W, 5%	603	Std	Std
1	0	0	0	0	U1	BQ24380DSG	IC, Li+ Charger Front-End Protection	DSG8	BQ24380DSG	TI
0	1	0	0	0	U1	BQ24381DSG	IC, Li+ Charger Front-End Protection	DSG8	BQ24381DSG	TI
0	0	1	0	0	U1	BQ24314ADSG	IC, Li+ Charger Front-End Protection	DSG8	BQ24314ADSG	TI
0	0	0	1	0	U1	BQ24315DSG	IC, Li+ Charger Front-End Protection	DSG8	BQ24315DSG	TI
0	0	0	0	1	U1	BQ24305DSG	IC, Li+ Charger Front-End Protection	DSG8	BQ24305DSG	TI
1	1	1	1	1	—	HPA245	PCB, 1.2 In × 3 In × 0.031 In		PCB	Any
Notes: 1. Number 0 in left side columns means do not use this component. 2. OPEN in value column means do not use this component. 3. Std in part number column means standard manufacturer's part number 4. Std in MFR column means standard manufacturer .										

4.3 Board Layout

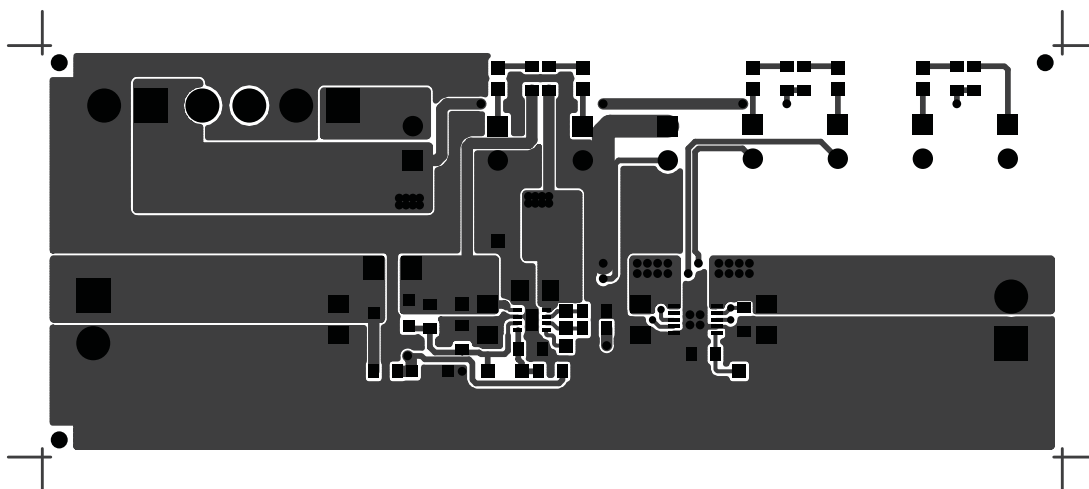


Figure 4. Top Layer

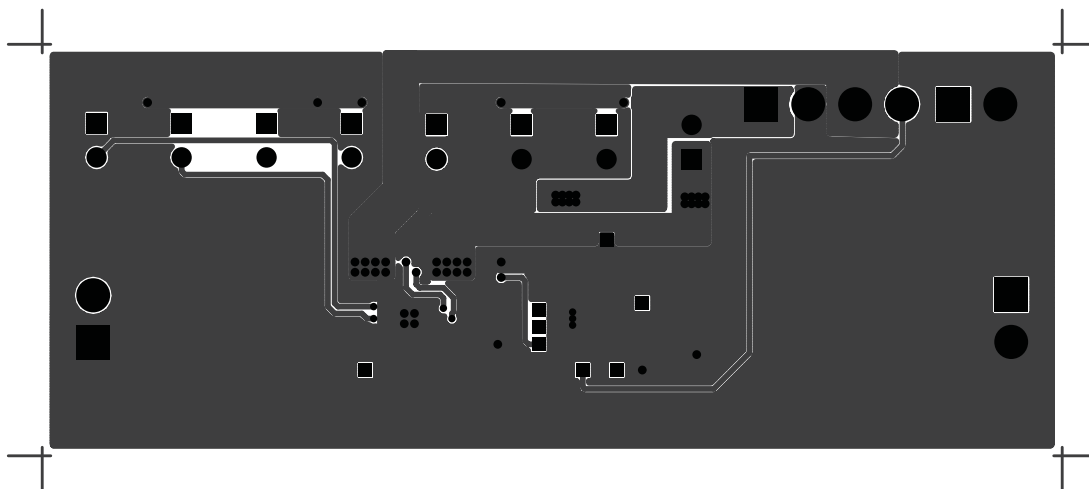


Figure 5. Bottom Layer

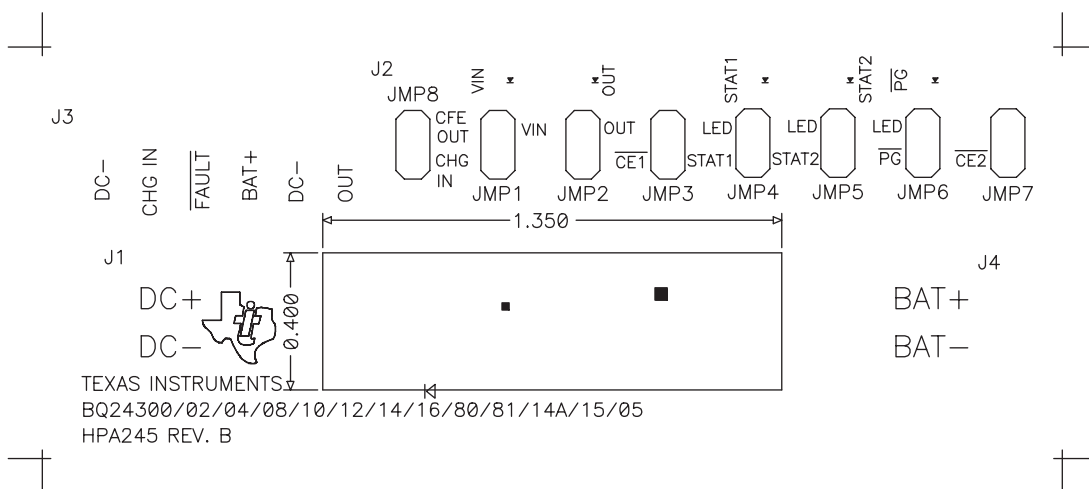


Figure 6. Top Silkscreen

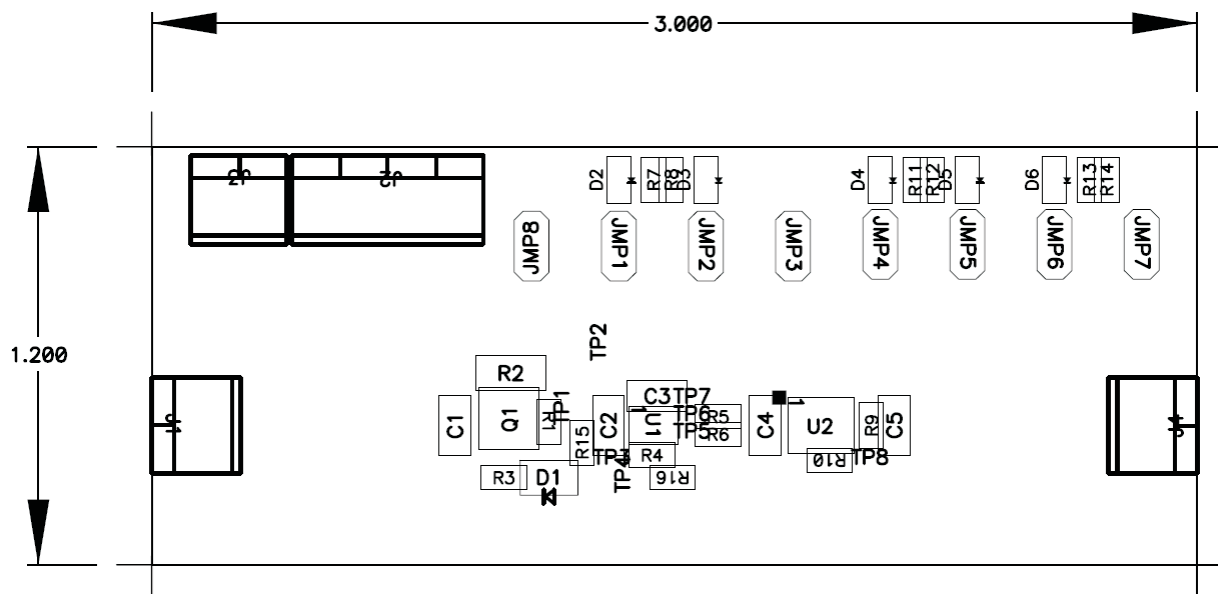
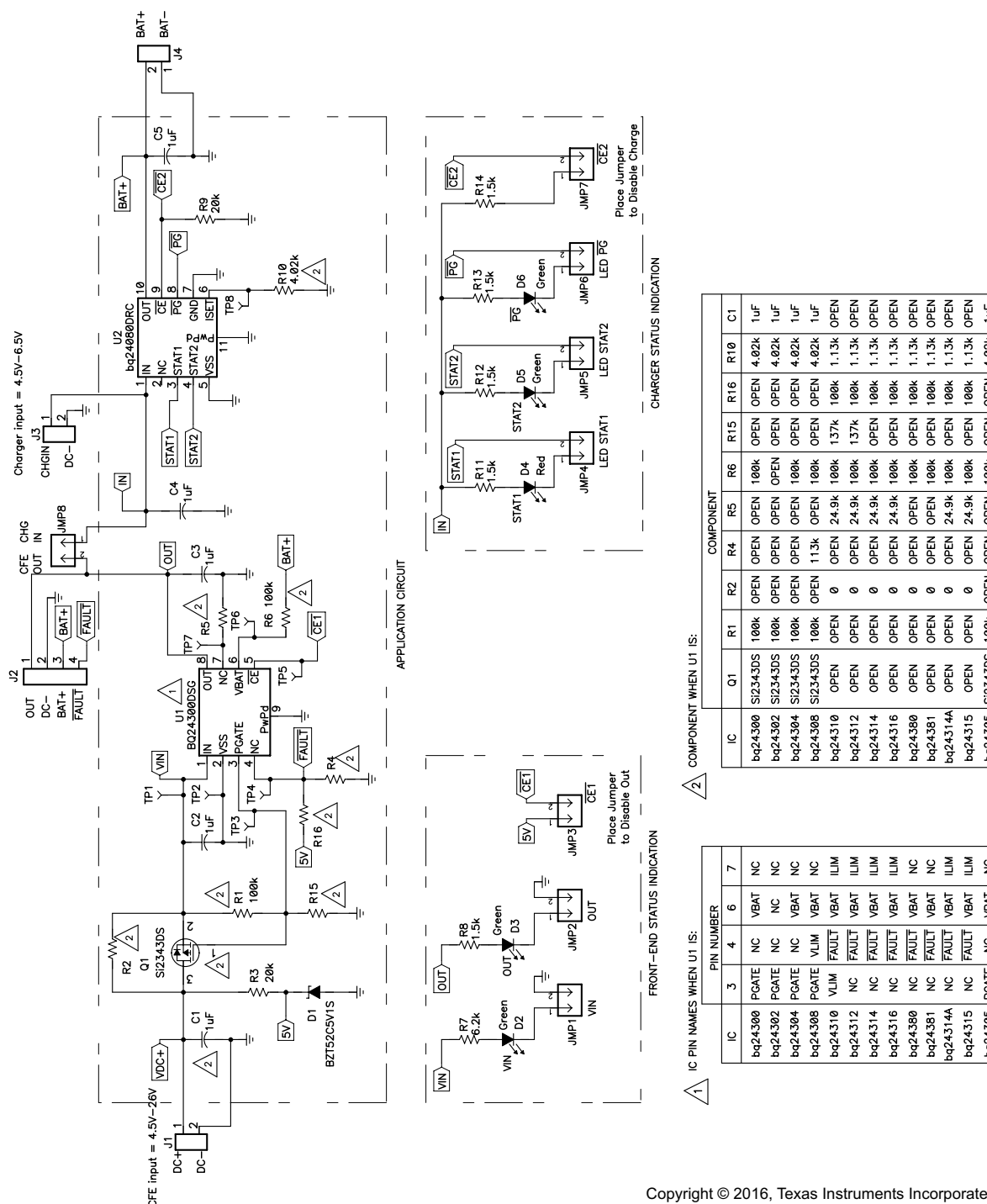


Figure 7. Top Assembly

4.4 Schematics

The bq2430x/1x/8x DSG EVM schematic follows.



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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (April 2008) to B Revision

Page

- Changed pin name for pin 3 in the IC pin names when U1 is: table of the schematics for the bq24312 from 'VLM' to 'NC'.....

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CAUTION

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

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Concernant les EVMs avec appareils radio:

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Concernant les EVMs avec antennes détachables

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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