



14-Bit, 105MSPS Analog-To-Digital Converter

FEATURES

- 14-Bit Resolution
- 105MSPS Sample Rate
- High SNR: 72dBFS at 100MHz f_{IN}
- High SFDR: 86dBc at 100MHz f_{IN}
- 2.3V_{PP} Differential Input Voltage
- Internal Voltage Reference
- 3.3V Single-Supply Voltage
- Analog Power Dissipation: 571mW
- Serial Programming Interface
- TQFP-64 PowerPAD™ Package
- Pin-Compatible With:
 - ADS5500 (14-Bit, 125MSPS)
 - ADS5542 (14-Bit, 80MSPS)
 - ADS5520 (12-Bit, 125MSPS)
 - ADS5521 (12-Bit, 105MSPS)
 - ADS5522 (12-Bit, 80MSPS)
- Recommended Op Amps:
 - OPA695, OPA847, THS3202, THS3201, THS4503, THS4509, THS9001

APPLICATIONS

- Wireless Communication
 - Communication Receivers
 - Base Station Infrastructure
- Test and Measurement Instrumentation
- Single and Multichannel Digital Receivers
- Communication Instrumentation
 - Radar, Infrared
- Video and Imaging
- Medical Equipment
- Military Equipment

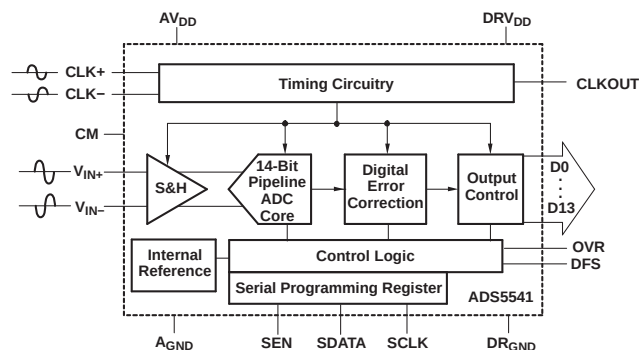
DESCRIPTION

The ADS5541 is a high-performance, 14-bit, 105MSPS analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in a small space, the ADS5541 has excellent analog power dissipation of 571mW at 3.3V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. The parallel CMOS compatible outputs ensure seamless interfacing with common logic.

The ADS5541 is available in a TQFP-64 PowerPAD package over the industrial temperature range.

ADS5500 PRODUCT FAMILY

	80MSPS	105MSPS	125MSPS
12-Bit	ADS5522	ADS5521	ADS5542
14-Bit	ADS5542	ADS5541	ADS5500



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD ⁽²⁾	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5541	HTQFP-64 PowerPAD	PAP	–40°C to +85°C	ADS5541I	ADS5541IPAP	Tray, 160
					ADS5541IPAPR	Tape and Reel, 1000

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Thermal pad size: 3.5mm × 3.5mm (min), 4mm × 4mm (max). $\theta_{JA} = 21.47^{\circ}\text{C/W}$ and $\theta_{JC} = 2.99^{\circ}\text{C/W}$, when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard, four-layer, 3in × 3in PCB.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		ADS5541	UNIT
Supply Voltage	AV_{DD} to A_{GND} , DRV_{DD} to DR_{GND}	–0.3 to 3.7	V
	A_{GND} to DR_{GND}	±0.1	V
Analog input to A_{GND} ⁽²⁾⁽³⁾		–0.3 to minimum ($AV_{DD} + 0.3$, +3.6)	V
Logic input to DR_{GND}		–0.3 to DRV_{DD}	V
Digital data output to DR_{GND}		–0.3 to DRV_{DD}	V
Operating temperature range		–40 to 85	°C
Junction temperature		105	°C
Storage temperature range		–65 to 150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) If the input signal can exceed 3.6V, then a resistor greater than or equal to 25Ω should be added in series with each of the analog input pins to support input voltages up to 3.8V. For input voltages above 3.8V, the device can only handle transients and the duty cycle of the overshoot should be limited to less than 5% for inputs up to 3.9V.
- (3) The overshoot duty cycle can be defined as the ratio of the total time of overshoot to the total intended device lifetime, expressed as a percentage. The total time of overshoot is the integrated time of all overshoot occurrences over the lifetime of the device.

RECOMMENDED OPERATING CONDITIONS

		ADS5541			UNIT
		MIN	TYP	MAX	
Supplies					
Analog supply voltage, AV _{DD}		3	3.3	3.6	V
Output driver supply voltage, DRV _{DD}		3	3.3	3.6	V
Analog Input					
Differential input range		2.3			V _{PP}
Input common-mode voltage, V _{CM} ⁽¹⁾		1.45	1.55	1.65	V
Digital Output					
Maximum output load		10			pF
Clock Input					
ADCLK input sample rate (sine wave) 1/t _C	DLL ON	60	105		MSPS
	DLL OFF	2	80		
Clock amplitude, sine wave, differential ⁽²⁾		1	3	V _{PP}	
Clock duty cycle ⁽³⁾		50%			
Open free-air temperature range		−40	85		°C

(1) Input common-mode should be connected to CM.

(2) See Figure 49 for more information.

(3) See Figure 48 for more information.

ELECTRICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, min and max specified over the full temperature range of -40°C to $+85^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and -1dBFS differential input, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5541			UNIT
		MIN	TYP	MAX	
Resolution			14		Bits
Analog Inputs					
Differential input range			2.3		V_{PP}
Differential input impedance	See Figure 39		6.6		$k\Omega$
Differential input capacitance	See Figure 39		4		pF
Analog input common-mode current (per input)			250		μA
Analog input bandwidth	Source impedance = 50Ω		750		MHz
Voltage overload recovery time			4		Clock cycles
Internal Reference Voltages					
Reference bottom voltage, V_{REFM}			0.95		V
Reference top voltage, V_{REFP}			2.1		V
Reference error		–4	± 0.9	4	%
Common-mode voltage output, V_{CM}		1.5	1.55	1.6	V
Dynamic DC Characteristics and Accuracy					
No missing codes			Tested		
Differential nonlinearity error, DNL	$f_{IN} = 55\text{ MHz}$	–0.9	± 0.25	1.1	LSB
Integral nonlinearity error, INL	$f_{IN} = 55\text{ MHz}$	–5	± 2.5	5	LSB
Offset error		–11	± 1.5	11	mV
Offset temperature coefficient			0.02		$\text{mV}/^\circ\text{C}$
DC power-supply rejection ratio, DC PSRR	$\Delta\text{offset error}/\Delta AV_{DD}$ from $AV_{DD} = 3\text{ V}$ to $AV_{DD} = 3.6\text{ V}$		0.25		mV/V
Gain error ⁽¹⁾		–2	± 0.3	2	%FS
Gain temperature coefficient			–0.02		$\Delta\%/^\circ\text{C}$

(1) Gain error is specified by design and characterization; it is not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, min and max specified over the full temperature range of -40°C to $+85^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and -1dBFS differential input, unless otherwise noted.

PARAMETER	CONDITIONS		ADS5541			UNIT
			MIN	TYP	MAX	
Dynamic AC Characteristics						
Signal-to-noise ratio, SNR	f _{IN} = 10MHz		73.6		dBFS	
	f _{IN} = 55MHz	+25°C to +85°C	71.7	72.7		
		Full temperature range		70.5		71.9
	f _{IN} = 70MHz		72.5			
	f _{IN} = 100MHz		72			
	f _{IN} = 150MHz		71			
	f _{IN} = 220MHz		69			
RMS idle channel noise	Input tied to common-mode		1.03		LSB	
Spurious-free dynamic range, SFDR	f _{IN} = 10MHz		84		dBc	
	f _{IN} = 55MHz	+25°C	78.3	86		
		Full temperature range		76.3		85
	f _{IN} = 70MHz		82			
	f _{IN} = 100MHz		86			
	f _{IN} = 150MHz		75			
	f _{IN} = 220MHz		72			
Second-harmonic, HD2	f _{IN} = 10MHz		90		dBc	
	f _{IN} = 55MHz	+25°C	78.3	86		
		Full temperature range		76.3		85
	f _{IN} = 70MHz		82			
	f _{IN} = 100MHz		88			
	f _{IN} = 150MHz		75			
	f _{IN} = 220MHz		72			
Third-harmonic, HD3	f _{IN} = 10MHz		84		dBc	
	f _{IN} = 55MHz	+25°C	78.3	89		
		Full temperature range		76.3		88
	f _{IN} = 70MHz		82			
	f _{IN} = 100MHz		86			
	f _{IN} = 150MHz		80			
	f _{IN} = 220MHz		78			
Worst-harmonic/spur (other than HD2 and HD3)	f _{IN} = 55MHz		87		dBc	
Signal-to-noise + distortion, SINAD	f _{IN} = 10MHz		72.6		dBFS	
	f _{IN} = 55MHz	+25°C	70.7	72		
		Full temperature range		69.5		71
	f _{IN} = 70MHz		71.8			
	f _{IN} = 100MHz		71.2			
	f _{IN} = 150MHz		70			
	f _{IN} = 220MHz		67			
Total harmonic distortion, THD	f _{IN} = 10MHz		80		dBc	
	f _{IN} = 55MHz	+25°C	76.5	83		
		Full temperature range		74.5		82
	f _{IN} = 70MHz		79			
	f _{IN} = 100MHz		84			
	f _{IN} = 150MHz		74			
	f _{IN} = 220MHz		70.5			
Effective number of bits, ENOB	f _{IN} = 55MHz		11.7		Bits	

ELECTRICAL CHARACTERISTICS (continued)

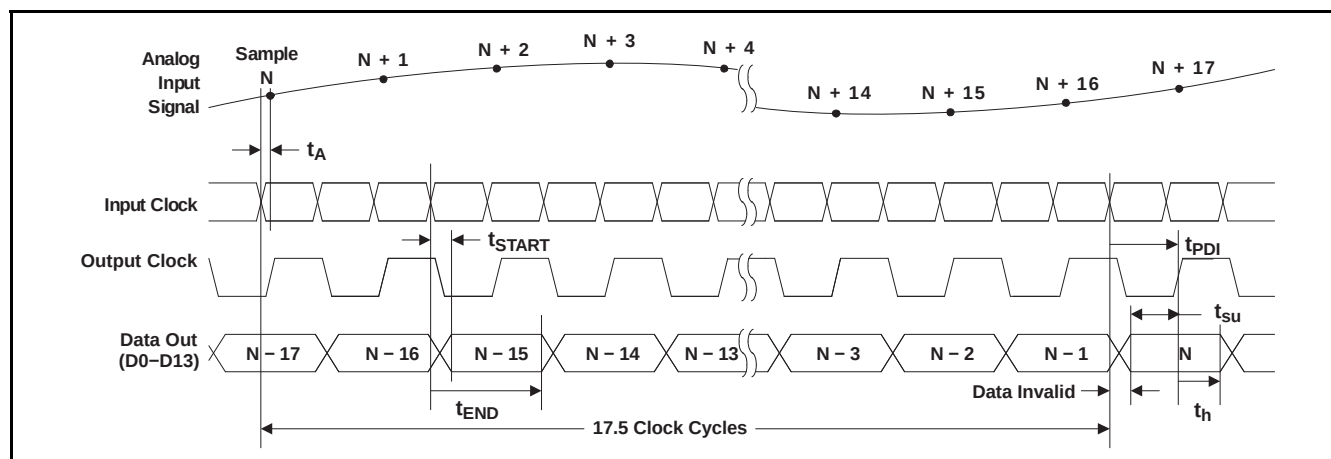
At $T_A = +25^\circ\text{C}$, min and max specified over the full temperature range of -40°C to $+85^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and -1dBFS differential input, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5541			UNIT
		MIN	TYP	MAX	
Dynamic AC Characteristics (continued)					
Two-tone intermodulation distortion, IMD	f = 10.1MHz, 15.1MHz (−7dBFS each tone)	94			dBFS
	f = 50.1MHz, 55.1MHz (−7dBFS each tone)	96			
	f = 150.1MHz, 155.1MHz (−7dBFS each tone)	84.7			
Power Supply					
Total supply current, I _{CC}	f _{IN} = 55MHz	224 250			mA
Analog supply current, I _{AVDD}	f _{IN} = 55MHz	173 185			mA
Output buffer supply current, I _{DRVDD}	f _{IN} = 55MHz	51 65			mA
Power dissipation	Analog only	571 611			mW
	Output buffer power with 10pF load on digital output to ground	168 215			
Standby power	With Clocks running	180 250			mW

DIGITAL CHARACTERISTICS

Valid over full temperature range of $T_{MIN} = -40^\circ\text{C}$ to $T_{MAX} = +85^\circ\text{C}$, and $AV_{DD} = DRV_{DD} = 3.3\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5541			UNIT
		MIN	TYP	MAX	
Digital Inputs					
V _{IH}	High-level input voltage	2.4			V
V _{IL}	Low-level input voltage	0.8			V
I _{IH}	High-level input current	10			μA
I _{IL}	Low-level input current	10			μA
Input current for RESET		−20			μA
Input capacitance		4			pF
Digital Outputs					
V _{OL}	Low-level output voltage	C _{LOAD} = 10pF	0.3	0.4	V
V _{OH}	High-level output voltage	C _{LOAD} = 10pF	2.8	3	V
Output capacitance			3		pF



NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

Figure 1. Timing Diagram

TIMING CHARACTERISTICS⁽¹⁾⁽²⁾

At $T_A = +25^{\circ}\text{C}$, min and max specified over the full temperature range of -40°C to $+85^{\circ}\text{C}$, sampling rate = 105MSPS, 50% clock duty cycle, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER		DESCRIPTION	ADS5541			UNIT
			MIN	TYP	MAX	
Switching Specification						
t _A	Aperture delay	Input CLK falling edge to data sampling point	1			ns
	Aperture jitter (uncertainty)	Uncertainty in sampling instant	300			fs
t _{SU}	Data setup time	Data valid ⁽³⁾ to 50% of CLKOUT rising edge	2.2	2.8	ns	
t _H	Data hold time	50% of CLKOUT rising edge to data becoming invalid ⁽³⁾	2.2	2.5	ns	
t _{START} ⁽⁴⁾⁽⁵⁾	Input clock to output data valid start	Input clock rising edge to data valid start delay	1.9	2.8	ns	
t _{END} ⁽⁴⁾⁽⁵⁾	Input clock to output data valid end	Input clock rising edge to data valid end delay	5.8	7.3	ns	
t _{JIT}	Output clock jitter	Uncertainty in CLKOUT rising edge, peak-to-peak	175	250	ps	
t _{RISE}	Output clock rise time	Rise time of CLKOUT from 20% to 80% of DRV _{DD}	2	2.2	ns	
t _{FALL}	Output clock fall time	Fall time of CLKOUT from 80% to 20% of DRV _{DD}	1.7	1.8	ns	
t _{PDI}	Input clock to output clock delay	Input clock rising edge, zero crossing, to output clock rising edge 50%	4	4.7	5.5	ns
t _R	Data rise time	Data rise time measured from 20% to 80% of DRV _{DD}	4.4	5.1	ns	
t _F	Data fall time	Data fall time measured from 80% to 20% of DRV _{DD}	3.3	3.8	ns	
	Output enable(OE) to data output delay	Time required for outputs to have stable timings with regard to input clock ⁽⁶⁾ after OE is activated	1000			Clock cycles
	Wakeup time	Time to valid data after coming out of software power down and stopping and restarting the clock	1000			Clock cycles
	Latency	Time for a sample to propagate to the ADC outputs	17.5			Clock cycles

- (1) Timing parameters are ensured by design and characterization and not tested in production.
- (2) See [Table 5](#) through [Table 8](#) in the [Application Information](#) section for timing information at additional sampling frequencies.
- (3) Data valid refers to 2V for LOGIC high and 0.8V for LOGIC low.
- (4) See the [Output Information](#) section for details on using the input clock for data capture.
- (5) These specifications apply when the CLKOUT polarity is set to rising edge (according to [Table 3](#)). Add 1/2 clock period for the valid number for a falling edge CLKOUT polarity.
- (6) Data outputs are available within a clock from assertion of OE; however, it takes 1000 clock cycles to ensure stable timing with respect to input clock.

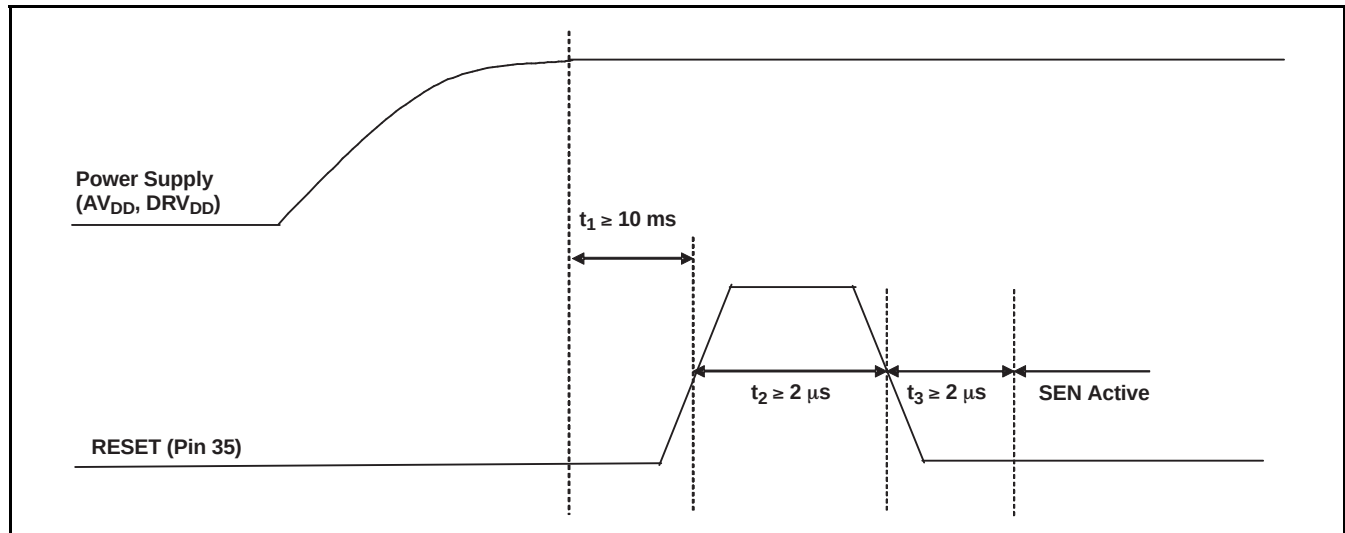


Figure 2. Reset Timing Diagram

RESET TIMING CHARACTERISTICS

Typical values given at $T_A = +25^\circ\text{C}$, min and max specified over the full temperature range of -40°C to $+85^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER		DESCRIPTION	ADS5541			UNIT
			MIN	TYP	MAX	
Switching Specification						
t ₁	Power-on delay	Delay from power-on of AV _{DD} and DRV _{DD} to RESET pulse	10			ms
t ₂	Reset pulse width	Pulse width of active RESET signal	2			μs
t ₃	Register write delay	Delay from RESET disable to SEN active	2			μs
	Power-up time	Delay from power-up of AV _{DD} and DRV _{DD} to output stable		40		ms

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The ADS5541 has a three-wire serial interface. The device latches the serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at the falling edge.
- Minimum width of data stream for a valid loading is 16 clocks.
- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiples of 16-bit words within a single active SEN pulse.
- The first 4-bit nibble is the address of the register while the last 12 bits are the register contents.

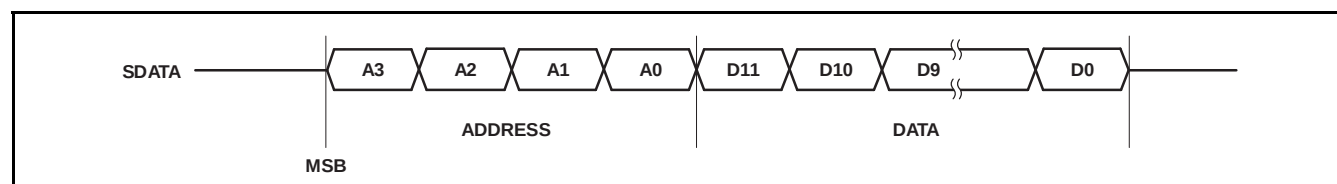


Figure 3. DATA Communication is 2-Byte, MSB First

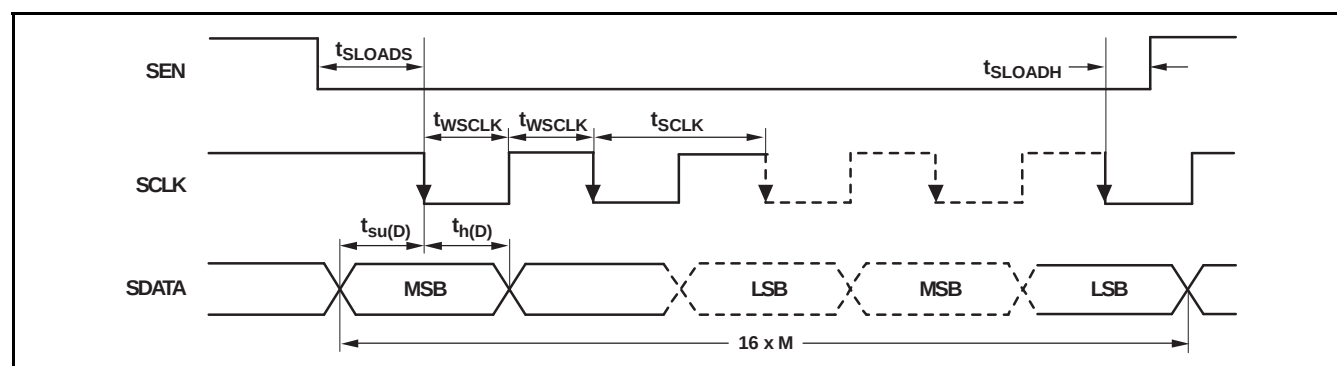


Figure 4. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface Timing Characteristics

SYMBOL	PARAMETER	ADS5541			UNIT
		MIN ⁽¹⁾	TYP ⁽¹⁾	MAX ⁽¹⁾	
t_{SCLK}	SCLK period	50			ns
t_{WSCLK}	SCLK duty cycle	25	50	75	%
t_{SLOADS}	SEN to SCLK setup time	8			ns
t_{SLOADH}	SCLK to SEN hold time	6			ns
$t_{SY(D)}$	Data setup time	8			ns
$t_{H(D)}$	Data hold time	6			ns

(1) Values are characterized, but not production tested.

Table 2. Serial Register Table⁽¹⁾

A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION	
														DLL CTRL	Clock DLL		
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Internal DLL is on; recommended for 60MSPS to 105MSPS clock speeds.	
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	Internal DLL is off; recommended for 2MSPS to 80MSPS clock speeds.	
				TP<1>	TP<0>											Test Mode	
1	1	1	0	0	0	0	0	0	0	0	0	0	0	X	0	Normal mode of operation	
1	1	1	0	0	0	1	0	0	0	0	0	0	0	X	0	All outputs forced to 0	
1	1	1	0	0	1	0	0	0	0	0	0	0	0	X	0	All outputs forced to 1	
1	1	1	0	0	1	1	0	0	0	0	0	0	0	X	0	Each output bit toggles between 0 and 1. ⁽²⁾⁽³⁾	
				PDN											Power Down		
1	1	1	1	0	0	0	0	0	0	0	0	0	0	X	0	Normal mode of operation	
1	1	1	1	1	0	0	0	0	0	0	0	0	0	X	0	Device is put in power-down (low-current) mode.	

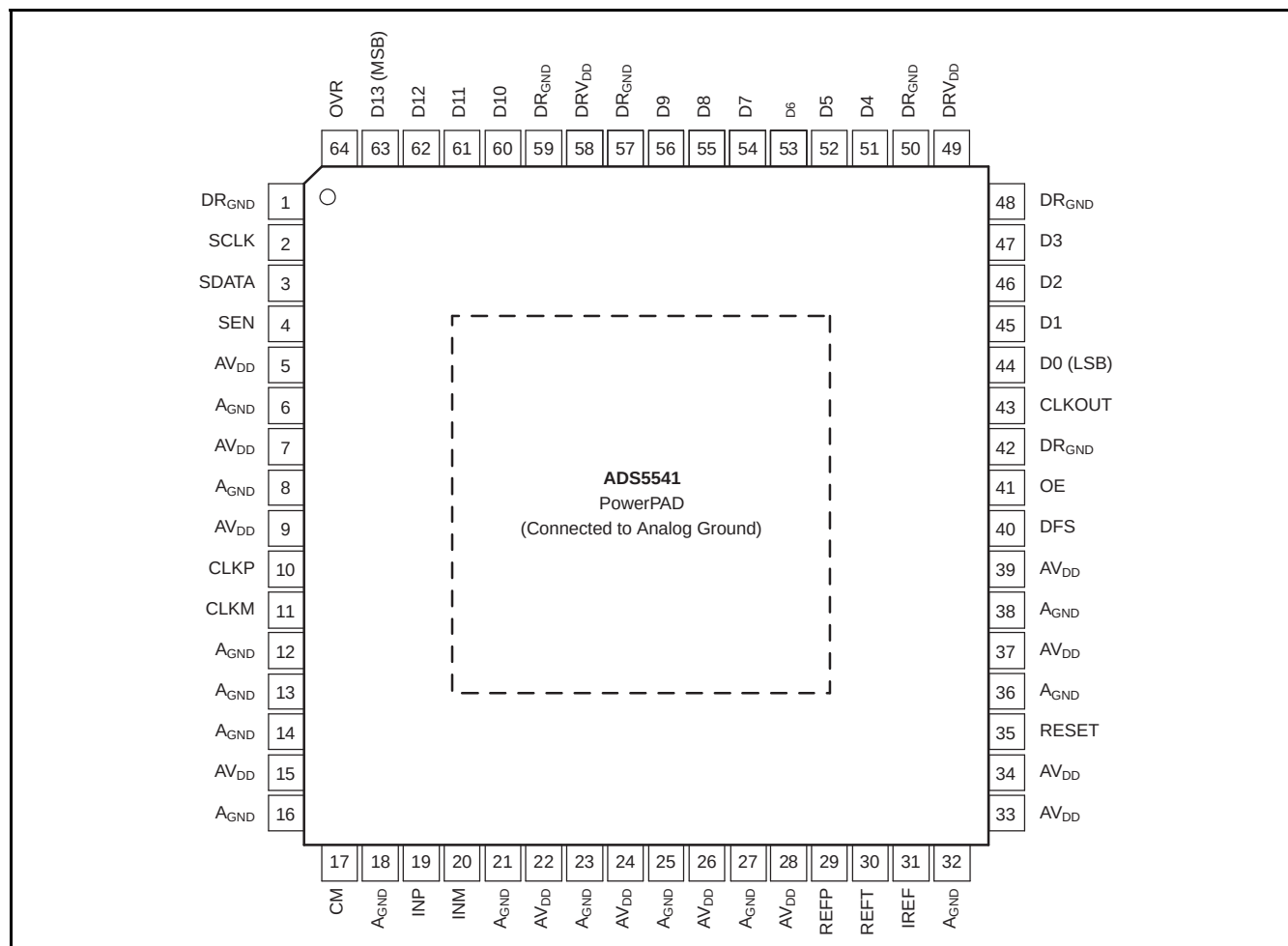
(1) The register contents default to the appropriate setting for normal operation up on RESET.

(2) The patterns given are applicable to the straight offset binary output format. If two's complement output format is selected, the test mode outputs will be the binary two's complement equivalent of these patterns as described in the [Output Information](#) section.

(3) While each bit toggles between 1 and 0 in this mode, there is no assured phase relationship between the data bits D0–D13. For example, when D0 is a 1, D1 is not assured to be a 0, and vice-versa.

Table 3. Data Format Select (DFS) Table

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{2}{12} \times AV_{DD}$	Straight Binary	Data valid on rising edge
$\frac{4}{12} \times AV_{DD} < V_{DFS} < \frac{5}{12} \times AV_{DD}$	Two's Complement	Data valid on rising edge
$\frac{7}{12} \times AV_{DD} < V_{DFS} < \frac{8}{12} \times AV_{DD}$	Straight Binary	Data valid on falling edge
$V_{DFS} > \frac{10}{12} \times AV_{DD}$	Two's Complement	Data valid on falling edge

PIN CONFIGURATION**PAP PACKAGE
(TOP VIEW)**

PIN CONFIGURATION (continued)**PIN ASSIGNMENTS ⁽¹⁾**

TERMINAL		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AV _{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
A _{GND}	6, 8, 12–14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground (PowerPAD must be connected to analog ground).
DRV _{DD}	49, 58	2	I	Output driver power supply
DR _{GND}	1, 42, 48, 50, 57, 59	6	I	Output driver ground
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive); 1μF capacitor in series with a 1Ω resistor to GND.
REFM	30	1	O	Reference voltage (negative); 1μF capacitor in series with a 1Ω resistor to GND.
IREF	31	1	I	Current set; 56kΩ resistor to GND; do not connect capacitors.
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high); Internal 200kΩ resistor to AV _{DD} . ⁽²⁾
OE	41	1	I	Output enable (active high) ⁽³⁾
DFS	40	1	I	Data format and clock out polarity select ⁽⁴⁾⁽³⁾
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select ⁽³⁾
SDATA	3	1	I	Serial interface data ⁽³⁾
SCLK	2	1	I	Serial interface clock ⁽³⁾
D0 (LSB)–D13 (MSB)	44–47, 51–56, 60–63	12	O	Parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data

(1) PowerPAD is connected to analog ground.

(2) If RESET pin is unused, it must be tied to AGND and serial interface should be used to reset the device. See the serial programming interface section for details.

(3) Pins OE, DFS, SEN, SDATA, and SCLK have internal clamping diodes to the DRV_{DD} supply. Any external circuit driving these pins must also run off the same supply voltage as DRV_{DD}.

(4) [Table 3](#) defines the voltage levels for each mode selectable via the DFS pin.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3dB with respect to the low frequency value.

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL)

The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error does not account for variations in the internal reference voltages (see the [Electrical Characteristics](#) section for limits on the variation of V_{REFP} and V_{REFM}).

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX} . It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference ($T_{MAX} - T_{MIN}$).

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first eight harmonics.

$$SNR = 10\log_{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to Full-Scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$\text{THD} = 10 \log_{10} \frac{P_S}{P_D} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR)

The DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

Reference Error

The reference error is the variation of the actual reference voltage ($V_{REFP} - V_{REFM}$) from its ideal value. The reference error is typically given as a percentage.

Voltage Overload Recovery Time

The voltage overload recovery time is defined as the time required for the ADC to recover to within 1% of the full-scale range in response to an input voltage overload of 10% beyond the full-scale range.

AC Power-Supply Rejection Ratio (AC PSRR)

The ratio of output spectral power at a given frequency with respect to the injected ac-power on AV_{DD} at that frequency. The rejected ac-input amplitude should be limited to less than 100mV_{PP} . The PSRR is typically given in units of dB.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{pp}$ differential clock, and -1dBFS differential input, unless otherwise noted.

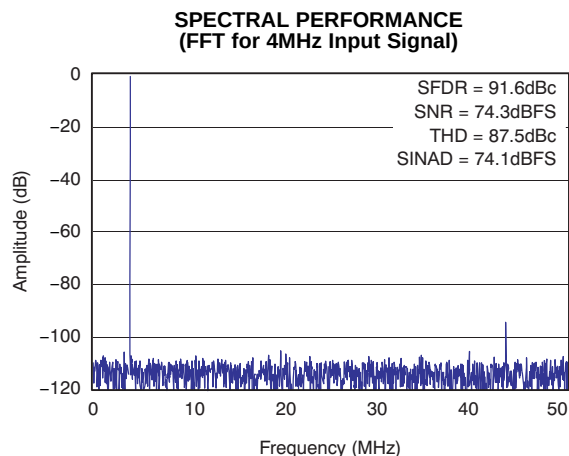


Figure 5.

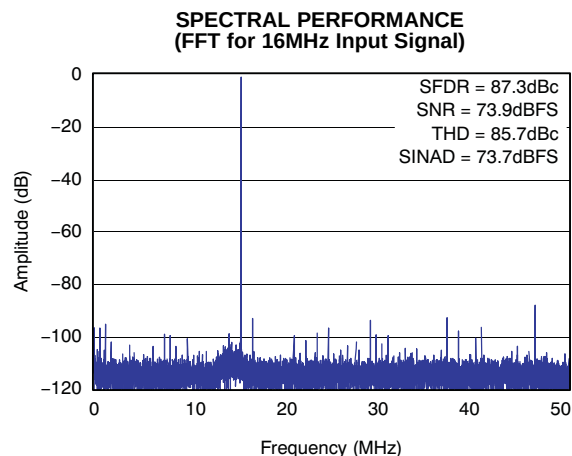


Figure 6.

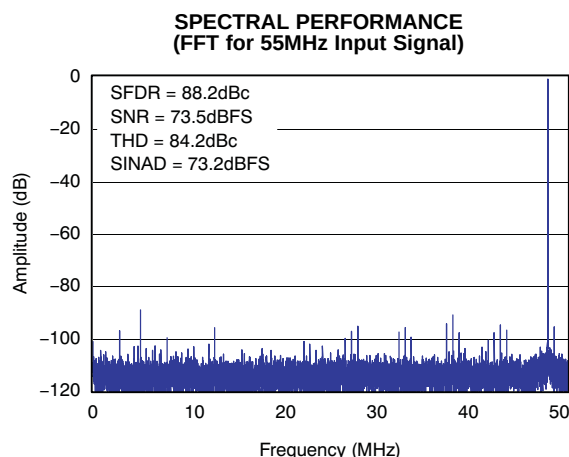


Figure 7.

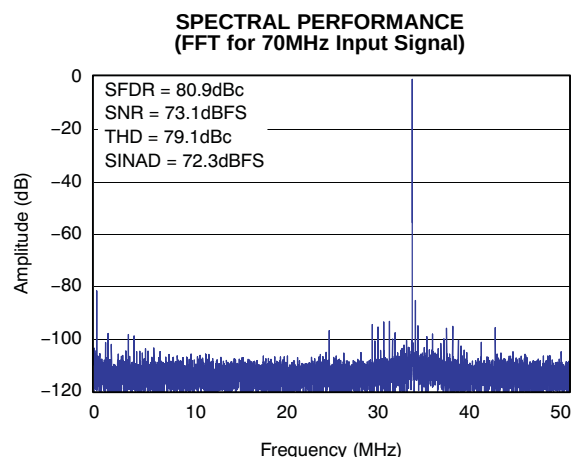


Figure 8.

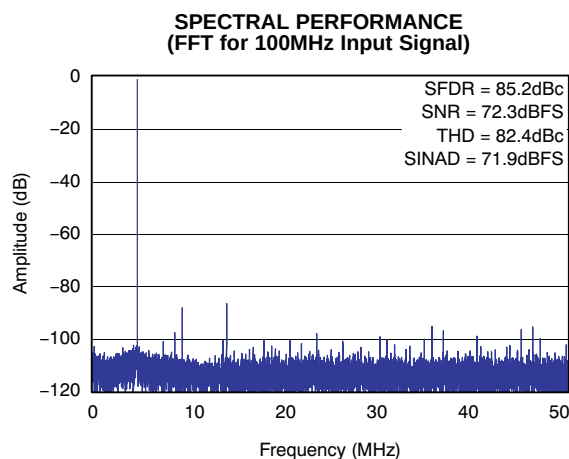


Figure 9.

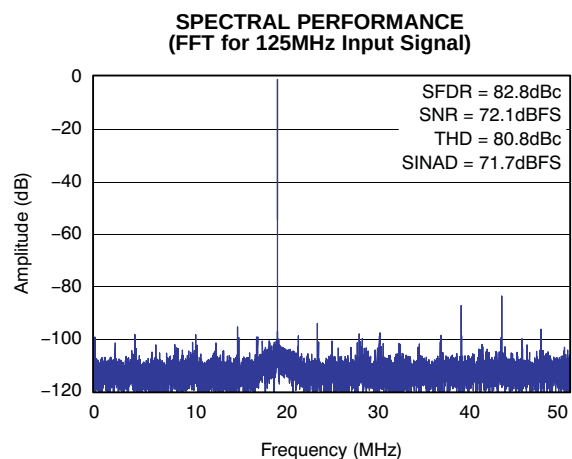


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{pp}$ differential clock, and -1dBFS differential input, unless otherwise noted.

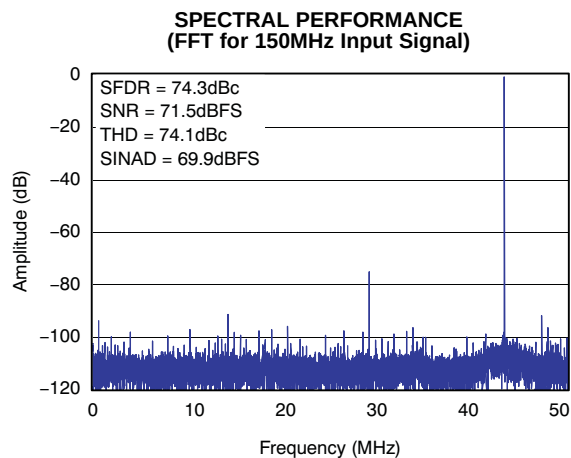


Figure 11.

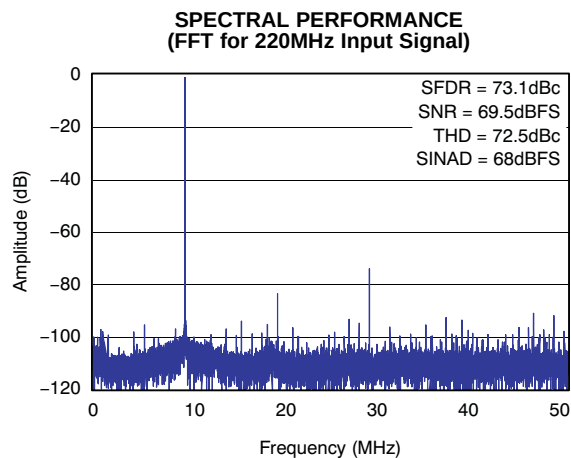


Figure 12.

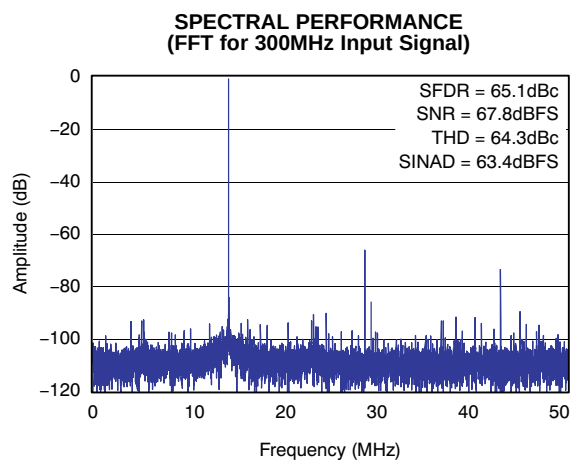


Figure 13.

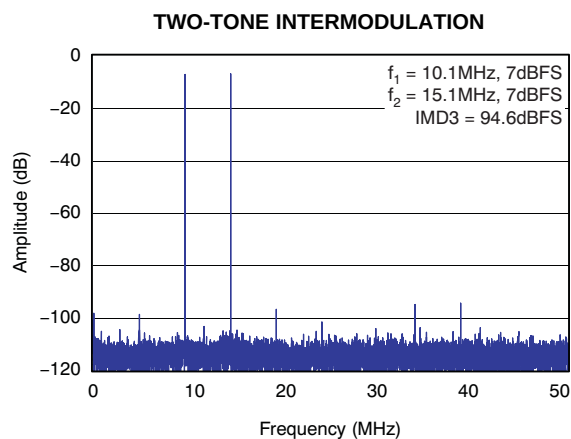


Figure 14.

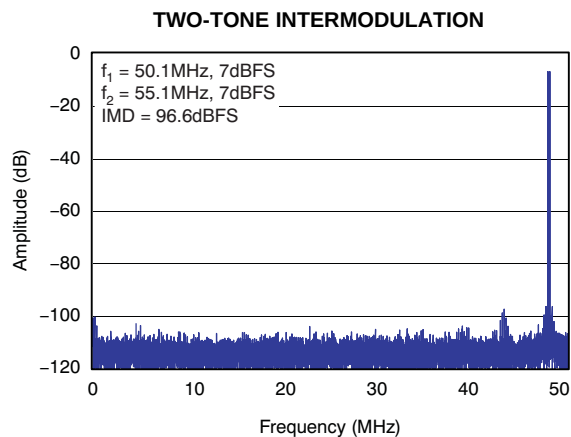


Figure 15.

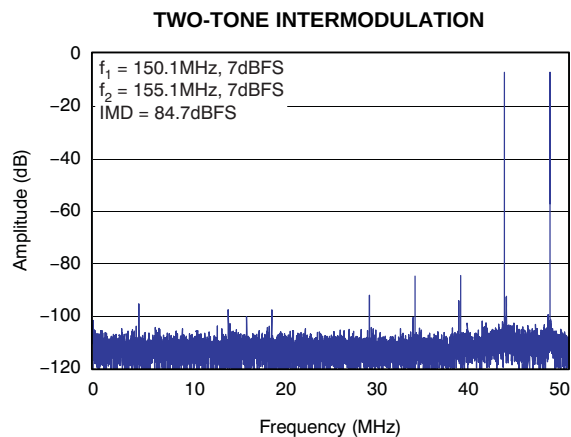
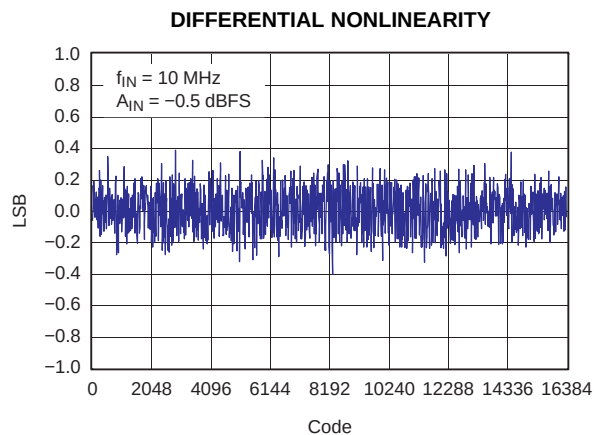
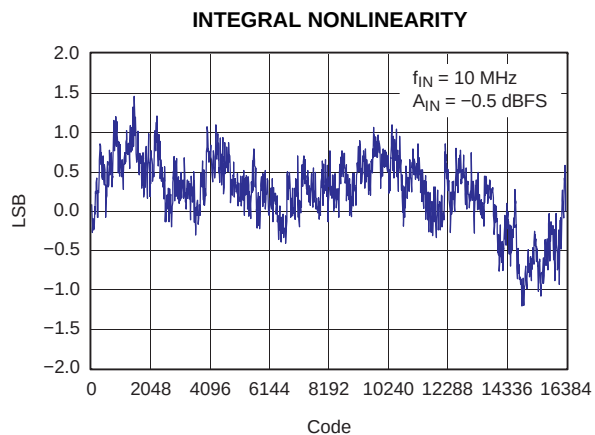
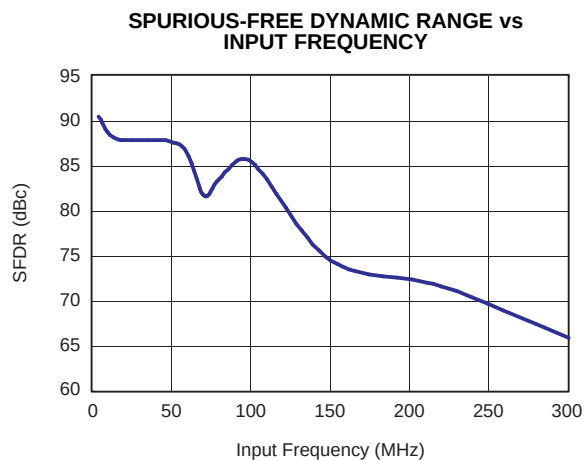
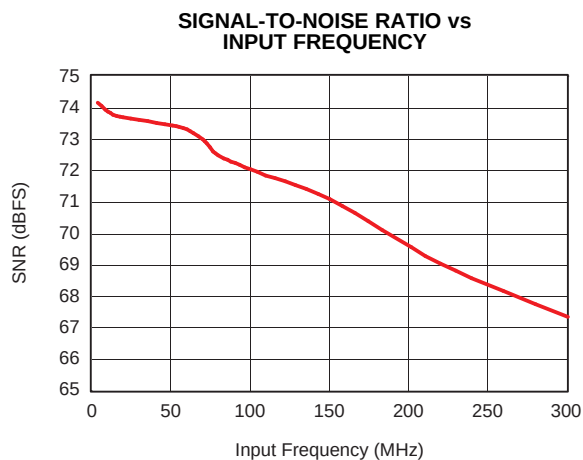
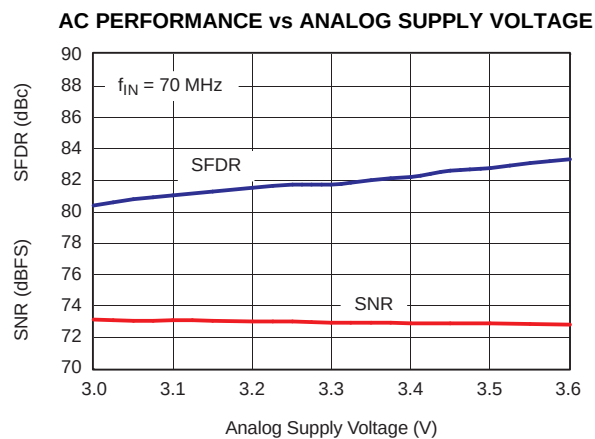
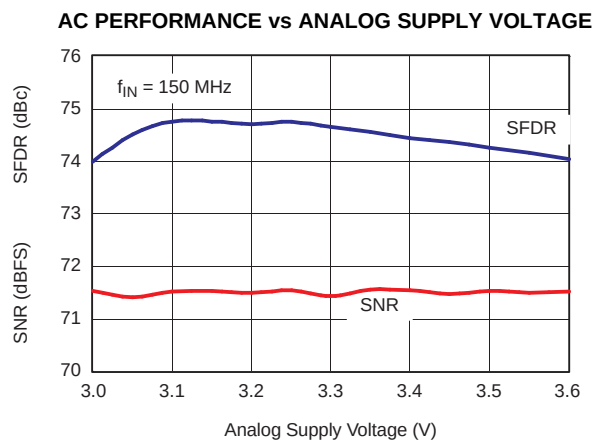


Figure 16.

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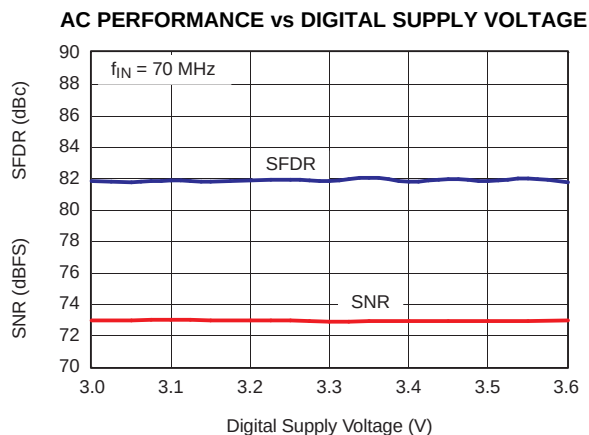
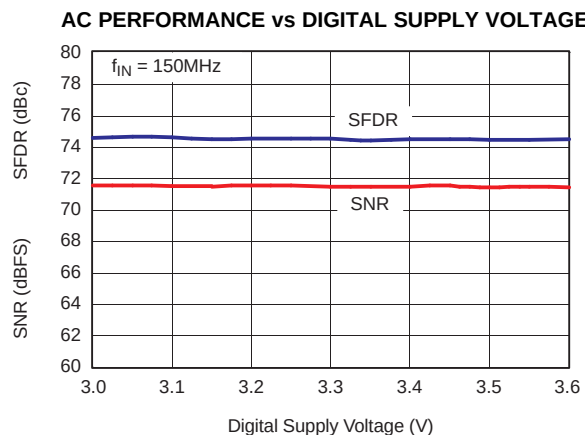
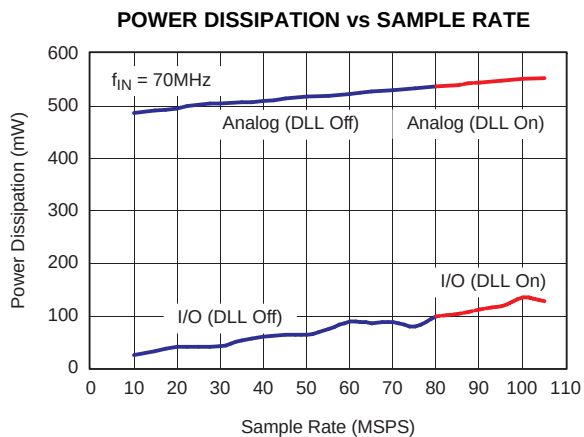
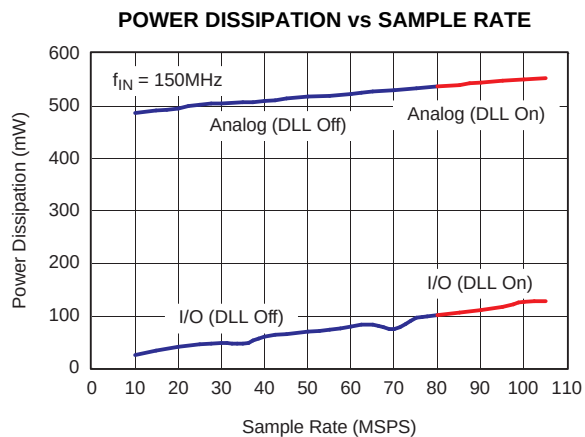
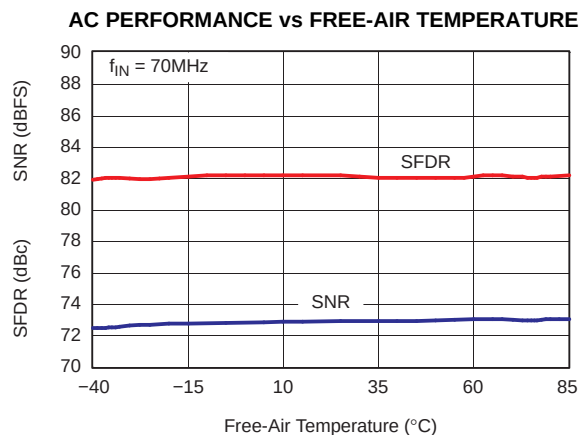
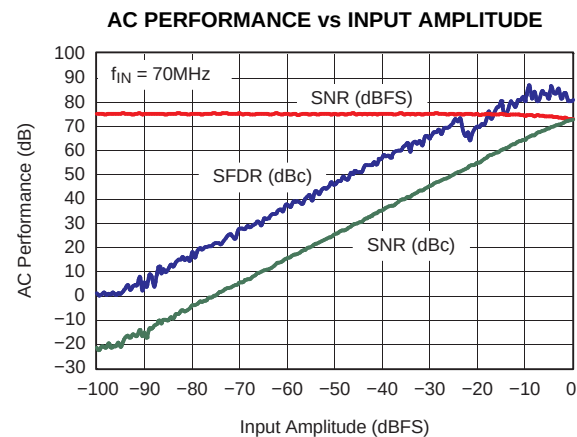
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and -1dBFS differential input, unless otherwise noted.

**Figure 17.****Figure 18.****Figure 19.****Figure 20.****Figure 21.****Figure 22.**

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{pp}$ differential clock, and -1dBFS differential input, unless otherwise noted.

**Figure 23.****Figure 24.****Figure 25.****Figure 26.****Figure 27.****Figure 28.**

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and -1dBFS differential input, unless otherwise noted.

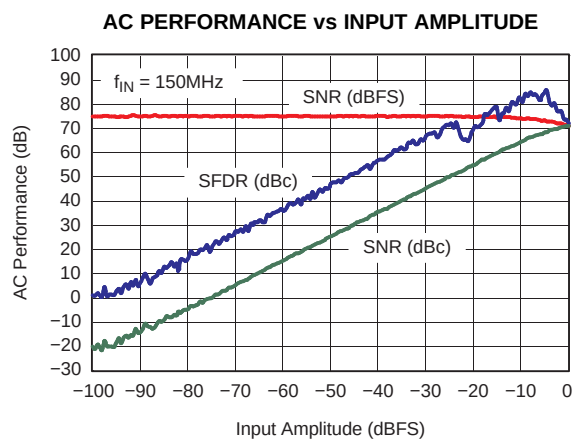


Figure 29.

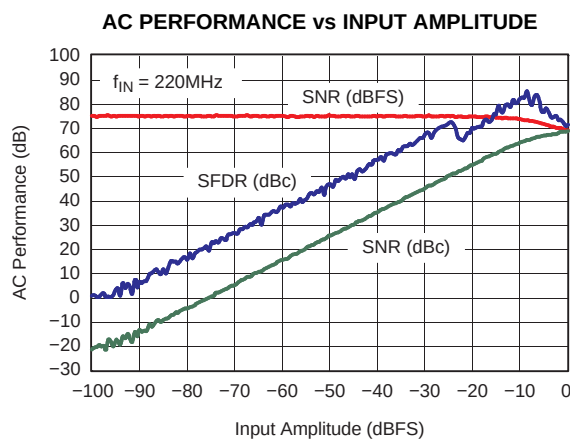


Figure 30.

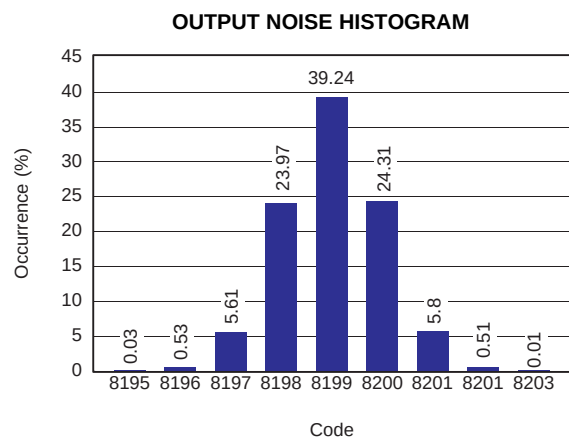


Figure 31.

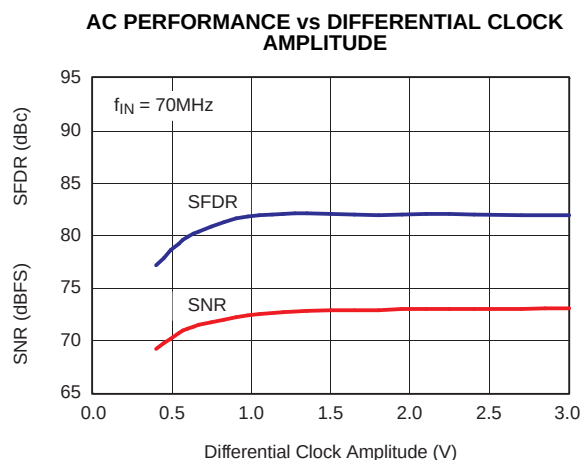


Figure 32.

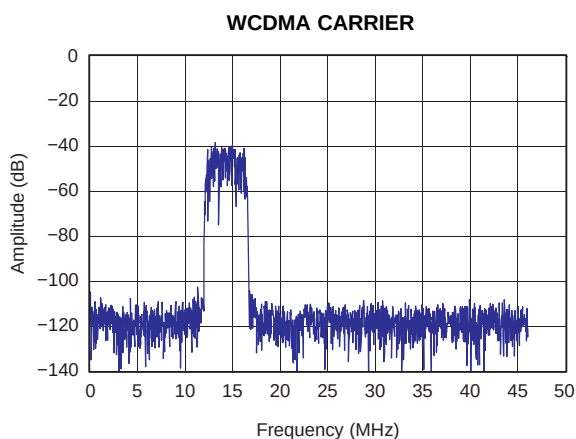


Figure 33.

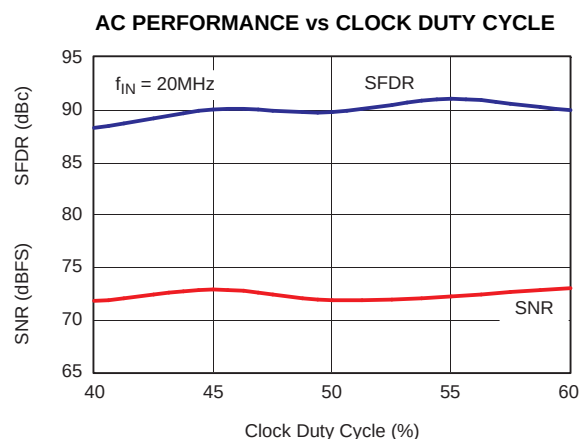


Figure 34.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{pp}$ differential clock, and -1dBFS differential input, unless otherwise noted.

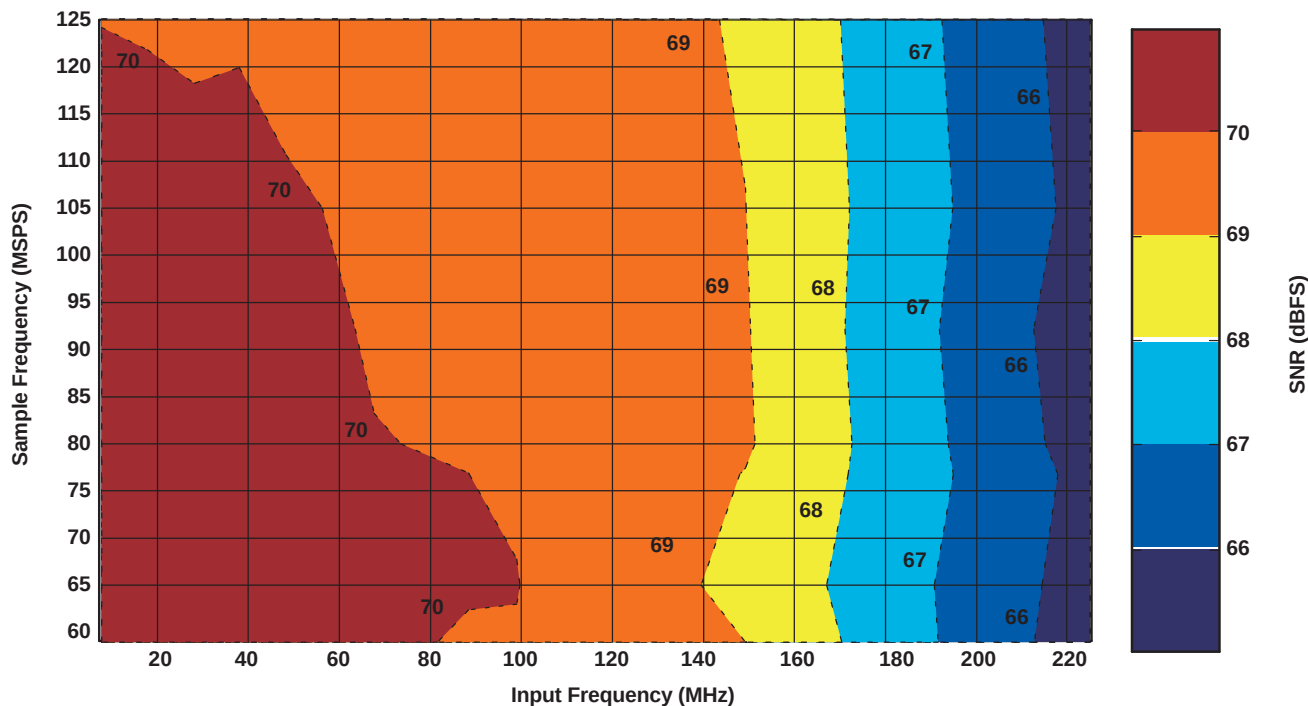


Figure 35. SIGNAL-TO-NOISE RATIO (SNR) (DLL On)

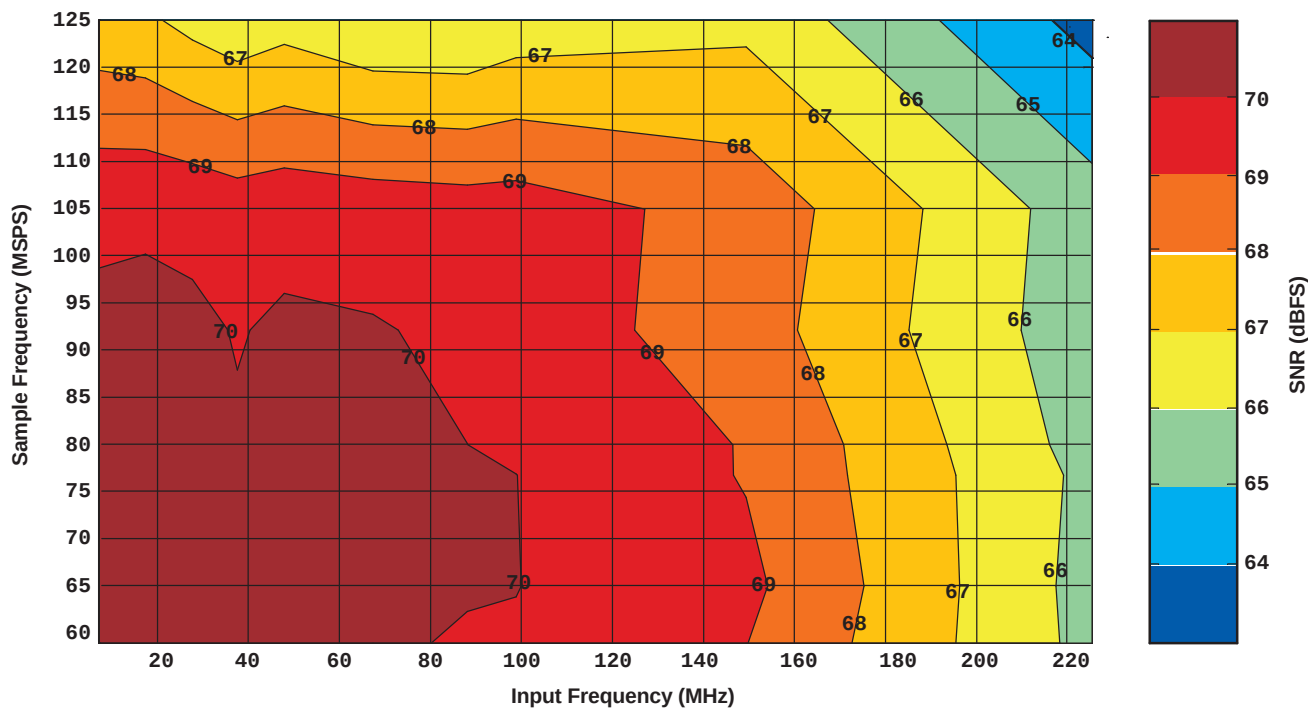


Figure 36. SIGNAL-TO-NOISE RATIO (SNR) (DLL Off)

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and -1dBFS differential input, unless otherwise noted.

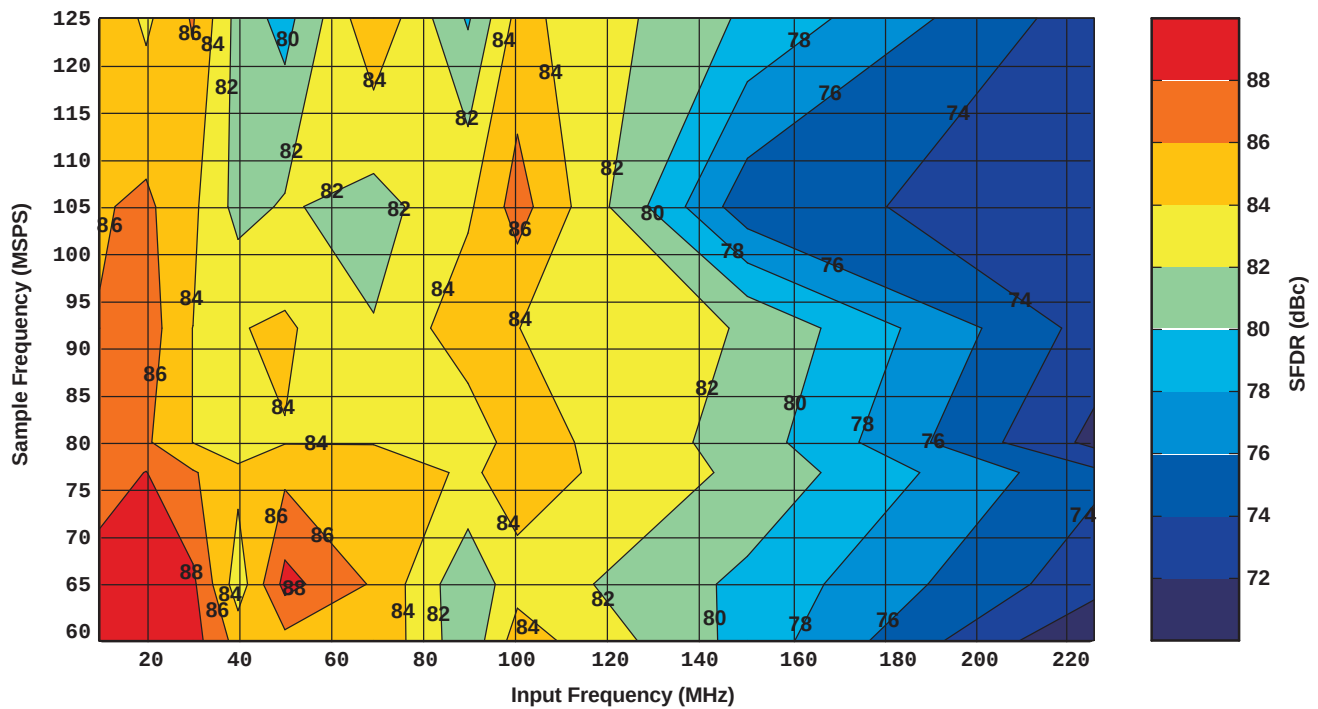


Figure 37. SPURIOUS-FREE DYNAMIC RANGE (SFDR) (DLL On)

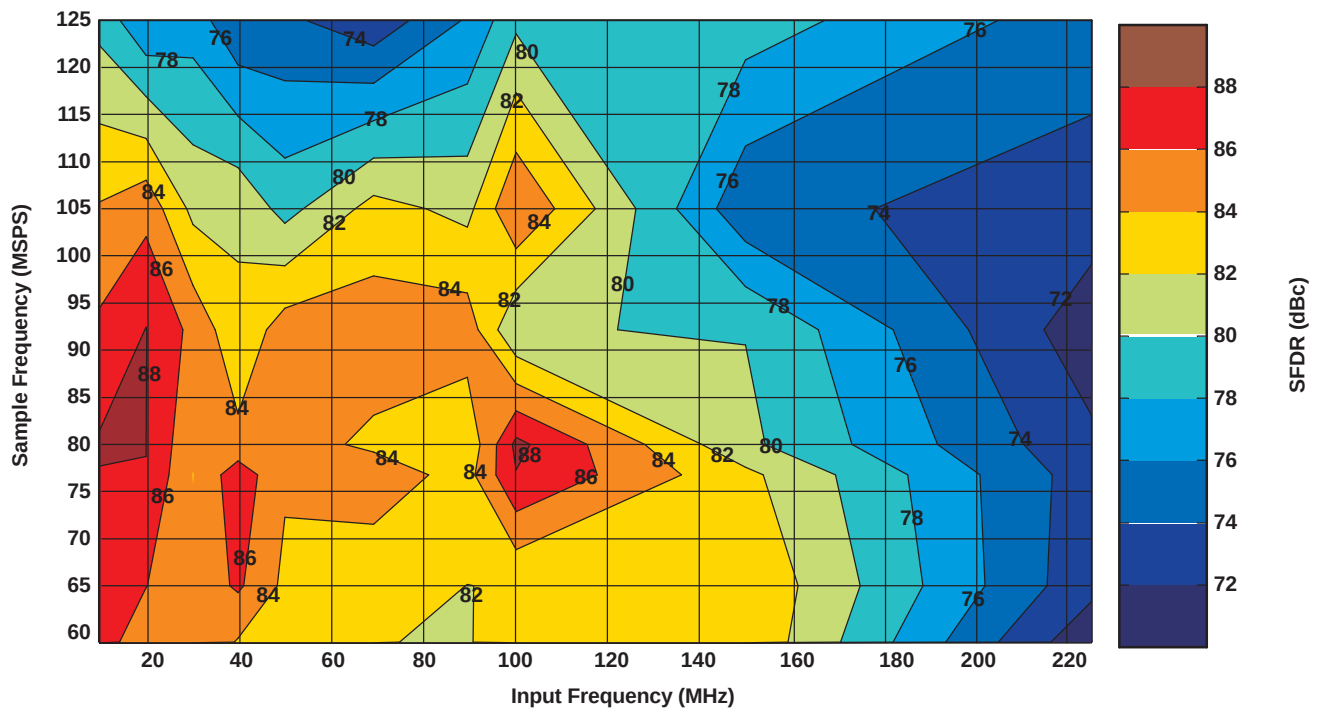


Figure 38. SPURIOUS-FREE DYNAMIC RANGE (SFDR) (DLL Off)

This differential input topology produces a high level of ac performance for high sampling rates. It also results in a very high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5541 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swing symmetrically between $CM + 0.575V$ and $CM - 0.575V$. This means that each input is driven with a signal of up to $CM \pm 0.575V$, so that each input has a maximum differential signal of $1.15V_{PP}$ for a total differential input signal swing of $2.3V_{PP}$. The maximum swing is determined by the two reference voltages, the top reference (REFP, pin 29) and the bottom reference (REFM, pin 30).

The ADS5541 gives optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 40 illustrates one possible configuration using an RF transformer.

The single-ended signal is fed to the primary winding of an RF transformer. Placing a 25Ω resistor in series with INP and INM is recommended to dampen ringing because of ADC kickback. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5541 is connected to the center-tap of the secondary winding. To ensure a steady low-noise V_{CM} reference, best performance is attained when the CM output (pin 17) is filtered to ground with a 10Ω series resistor and parallel $0.1\mu F$ and $0.001\mu F$ low-inductance capacitors as illustrated in Figure 39.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of $500\mu A$ ($250\mu A$ per input) at 105MSPS. Equation 5 describes the dependency of the common-mode current and the sampling frequency:

$$\frac{500\mu A \times f_s \text{ (in MSPS)}}{105 \text{ MSPS}} \quad (5)$$

Where:

$$f_s > 2 \text{ MSPS.}$$

This equation helps to design the output capability and impedance of the driving circuit accordingly.

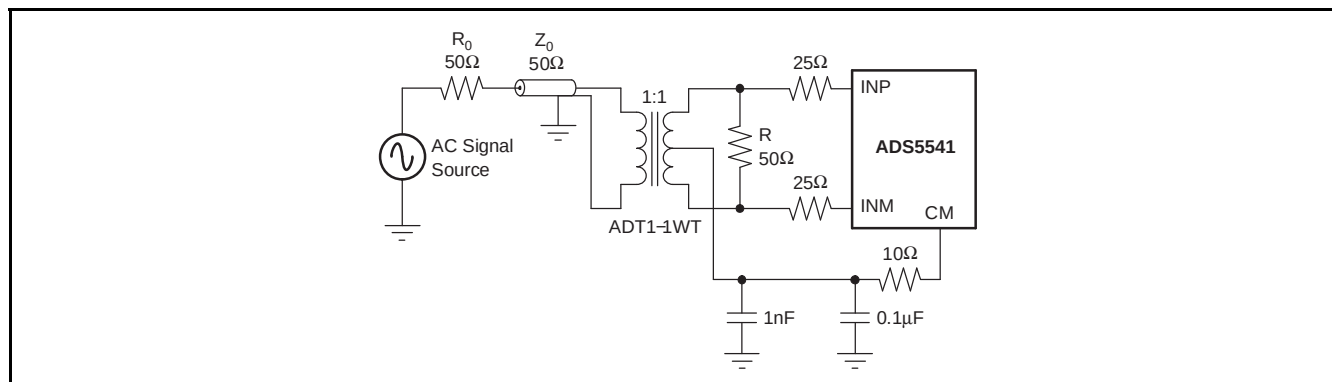


Figure 40. Transformer Input to Convert Single-Ended Signal to Differential Signal

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5541. Texas Instruments offers a wide selection of single-ended operational amplifiers (including the [THS3201](#), [THS3202](#), [OPA847](#), and [OPA695](#)) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instruments [THS9001](#), can also be used with an RF transformer for high input frequency applications. The THS4503 is a recommended differential input/output amplifier. [Table 4](#) lists the recommended amplifiers.

When using single-ended operational amplifiers (such as the [THS3201](#), [THS3202](#), [OPA847](#), or [OPA695](#)) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5520. These three amplifier circuits minimize even-order harmonics. For high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5541 directly, as shown in [Figure 40](#), or with the addition of the filter circuit shown in [Figure 41](#).

[Figure 41](#) illustrates how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5541 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5541 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring dc-coupling of the input. Flexible in their configurations (see [Figure 42](#)), such amplifiers can be used for single-ended-to-differential conversion signal amplification.

Table 4. Recommended Amplifiers to Drive the Input of the ADS5520

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER
DC to 20MHz	THS4503	Differential In/Out Amp	No
DC to 50MHz	OPA847	Operational Amp	Yes
10MHz to 120MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100MHz	THS9001	RF Gain Block	Yes

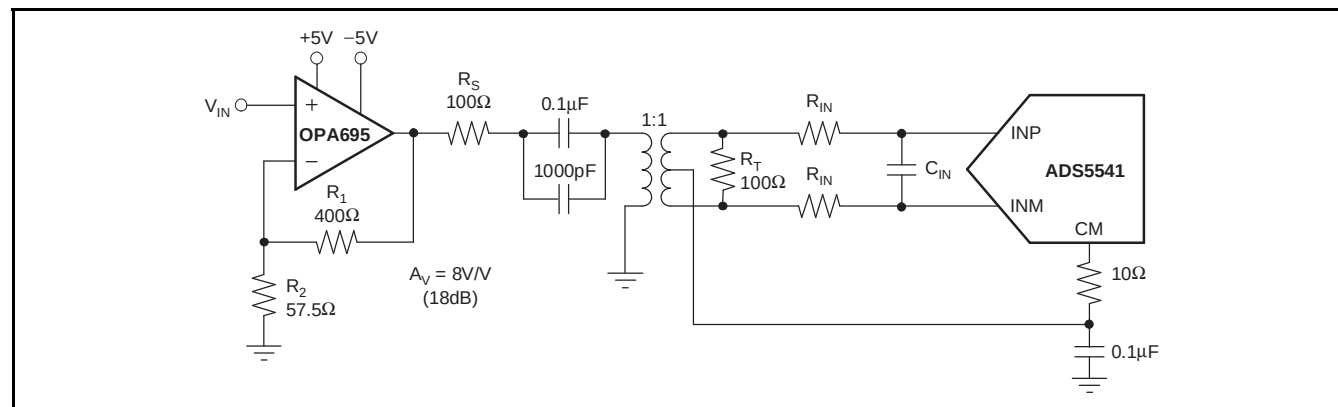


Figure 41. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

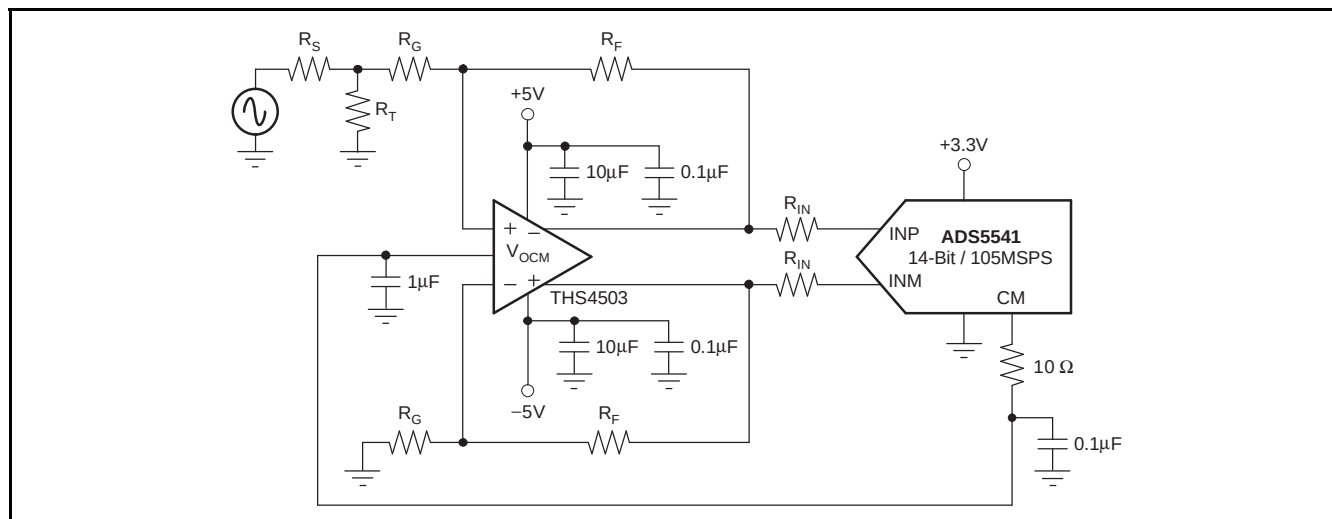


Figure 42. Using the THS4503 with the ADS5520

POWER-SUPPLY SEQUENCE

The preferred mode of power-supply sequencing is to power up AV_{DD} first, followed by DRV_{DD} . Raising both supplies simultaneously is also a valid power-supply sequence. In the event that DRV_{DD} powers up before AV_{DD} in the system, AV_{DD} must power up within 10ms of DRV_{DD} . Optionally, it is recommended to put a 2kΩ resistor from REFP (pin 29) to AV_{DD} as shown in Figure 43. This configuration helps to make the device more robust to power supply ramp-up timings.

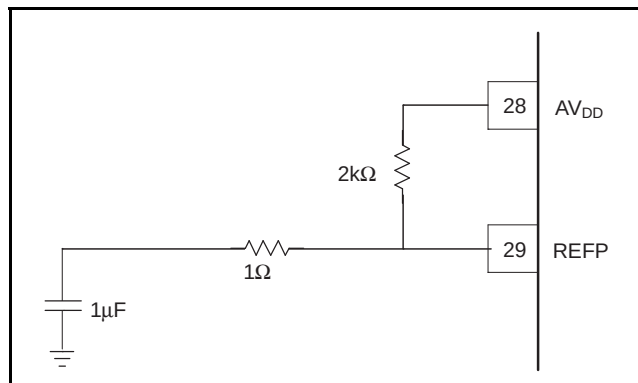


Figure 43.

POWER-DOWN

The device enters power-down in one of two ways: either by reducing the clock speed or by setting the PDN bit via the serial programming interface. Using the reduced clock speed, power-down may be initiated for clock frequency below 2MSPS. The exact frequency at which the power-down occurs varies from device to device.

Using the serial interface PDN bit to power down the device places the outputs in a high-impedance state and only the internal reference remains on to reduce the power-up time. The power-down mode reduces power dissipation to approximately 180mW.

REFERENCE CIRCUIT

The ADS5541 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1µF decoupling capacitor (the 1Ω resistor shown in Figure 44 is optional). In addition, an external 56kΩ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC, as shown in Figure 44. No capacitor should be connected between pin 31 and ground; only the 56kΩ resistor should be used.

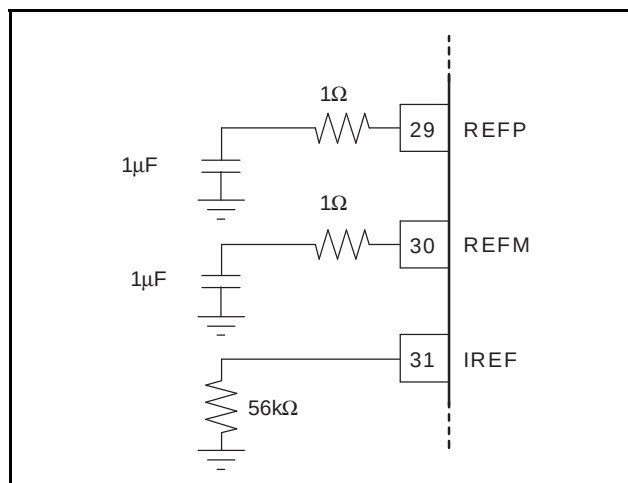


Figure 44. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5541 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal $5\text{k}\Omega$ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17), as shown in Figure 45.

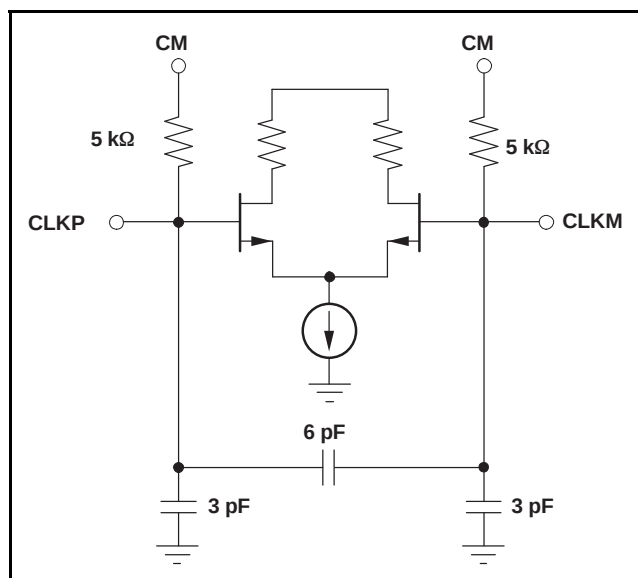


Figure 45. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a $0.01\mu\text{F}$ capacitor, while CLKP is ac-coupled with a $0.01\mu\text{F}$ capacitor to the clock source, as shown in Figure 46.

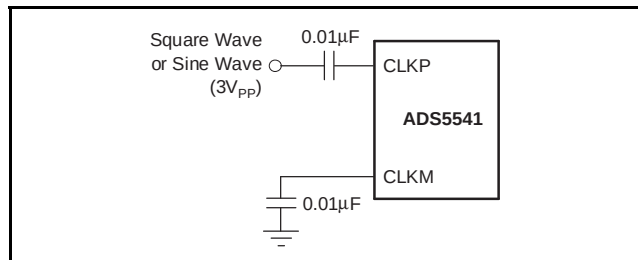


Figure 46. AC-Coupled, Single-Ended Clock Input

The ADS5541 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with $0.01\mu\text{F}$ capacitors, as shown in Figure 47.

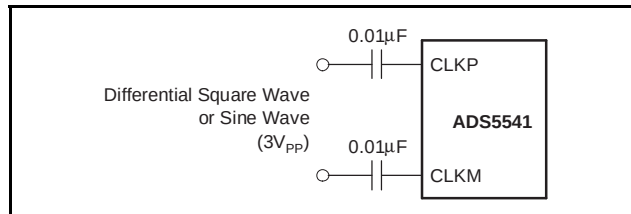


Figure 47. AC-Coupled, Differential Clock Input

For high-input frequency sampling, it is recommended to use a clock source with low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 48 shows the performance variation of the ADC versus clock duty cycle.

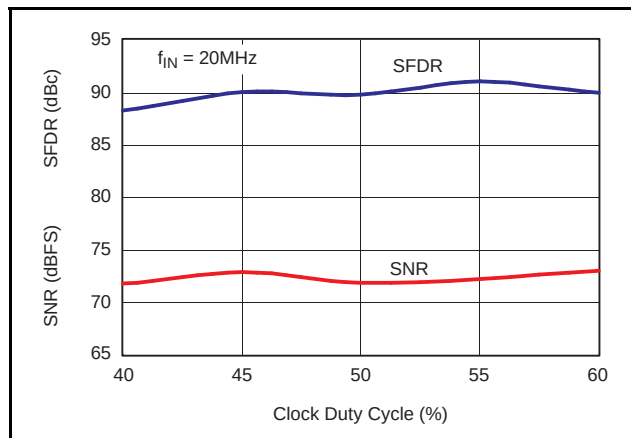


Figure 48. AC Performance vs Clock Duty Cycle

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter further improves as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 49 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, see the ADS5541EVM User's Guide (SLWU010), available for download from www.ti.com.

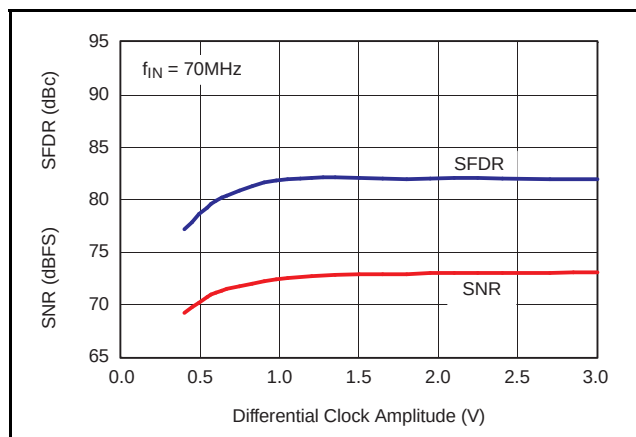


Figure 49. AC Performance vs Clock Amplitude

INTERNAL DLL

In order to achieve the fastest possible sampling rates with the ADS5541, the device uses an internal delay locked loop (DLL). The effective delay range of the DLL limits its use to sampling rates above 60MSPS. In order to operate the device below 60MSPS, the internal DLL must be shut off using the DLL OFF mode described in the [Serial Programming Interface](#) section. The [Typical Characteristics](#) show the performance obtained in both modes of operation: DLL ON (default) and DLL OFF. In either

of the two modes, the device enters power-down mode if no clock or a slow clock is provided. The limit of the clock frequency where the device functions properly with default settings is ensured to be over 2MHz.

OUTPUT INFORMATION

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals '1' when the output reaches the full-scale limits.

Two different output formats (straight offset binary or two's complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to put the outputs into a high-impedance state.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0x3FFF in straight offset binary output format, and 0x1FFF in two's complement output format. For a negative input overdrive, the output code is 0x0000 in straight offset binary output format, and 0x2000 in two's complement output format. These outputs to an overdrive signal are ensured through design and characterization

The output circuitry of the ADS5541, by design, minimizes the noise produced by the data switching transients, and, in particular, its coupling to the ADC analog circuitry. Output D4 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1. Care should be taken to ensure that all output lines (including CLKOUT) have nearly the same load as D4 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. Placing external resistors in series with the outputs is **not** recommended.

The timing characteristics of the digital outputs change for sampling rates below the 105MSPS maximum sampling frequency. Table 5 and Table 6 show the setup, hold, and input clocks to output data delays, and rise and fall times for different sampling frequencies with the DLL on and off, respectively.

Table 7 and Table 8 show the values of various timing parameters for lower sampling frequencies, both with DLL on and off.

To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay, t_d , that results in the desired setup or hold time. Use either of the following equations to calculate the value of t_d .

$$\text{Desired setup time} = t_D - t_{\text{START}}$$

$$\text{Desired hold time} = t_{\text{END}} - t_D$$

Table 5. Timing Characteristics at Additional Sampling Frequencies (DLL ON)

f_s (MSPS)	t_{SU} (ns)			t_{H} (ns)			t_{START} (ns)			t_{END} (ns)			t_{R} (ns)			t_{F} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	2.8	3.7		2.8	3.3			0.5	1.7	5.3	7.9			5.8	6.6		4.4	5.3
65	3.8	4.6		3.6	4.1			-0.5	0.8	5.3	8.5			6.7	7.2		5.5	6.4

Table 6. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)

f_s (MSPS)	t_{SU} (ns)			t_{H} (ns)			t_{START} (ns)			t_{END} (ns)			t_{R} (ns)			t_{F} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	3.2	4.2		1.8	3			3.8	5	8.4	11			5.8	6.6		4.4	5.3
65	4.3	5.7		2	3			2.8	4.5	8.3	11.8			6.6	7.2		5.5	6.4
40	8.5	11		2.6	3.5			-1	1.5	8.9	14.5			7.5	8		7.3	7.8
20	17	25.7		2.5	4.7			-9.8	2	9.5	21.6			7.5	8		7.6	8
10	27	51		4	6.5			-30	-3	11.5	31							
2	284	370		8	19			185	320	515	576			50	82		75	150

Table 7. Timing Characteristics at Additional Sampling Frequencies (DLL ON)

f_s (MSPS)	CLKOUT t_{RISE} (ns)			CLKOUT t_{FALL} (ns)			CLKOUT Jitter, Peak-to-Peak t_{JIT} (ps)			Input-to-Output Clock Delay t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80		2.5	2.8		2.1	2.3		210	315	3.7	4.3	5.1
65		3.1	3.5		2.6	2.9		260	380	3.5	4.1	4.8

Table 8. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)

f_s (MSPS)	CLKOUT t_{RISE} (ns)			CLKOUT t_{FALL} (ns)			CLKOUT Jitter, Peak-to-Peak t_{JIT} (ps)			Input-to-Output Clock Delay t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80		2.5	2.8		2.1	2.3		210	315	7.1	8	8.9
65		3.1	3.5		2.6	2.9		260	380	7.8	8.5	9.4
40		4.8	5.3		4	4.4		445	650	9.5	10.4	11.4
20		8.3	9.5		7.6	8.2		800	1200	13	15.5	18
2		31	52		36	65		2610	4400	537	551	567

SERIAL PROGRAMMING INTERFACE

The ADS5541 has internal registers for the programming of some of the modes described in the previous sections. The registers should be reset after power-up by applying a 2 μ s (minimum) high pulse on RESET (pin 35); this pulse also resets the entire ADC and sets the data outputs to low. This pin has a 200k Ω internal pullup resistor to AV_{DD}. The programming is done through a three-wire interface.

Table 2 shows the different modes and the bit values to be written to the register to enable them.

Note that some of these modes may modify the standard operation of the device and possibly vary the performance with respect to the typical data shown in this data sheet.

Applying a RESET signal is absolutely essential to set the internal registers to the default states for normal operation. If the hardware RESET function is not used in the system, the RESET pin must be tied to ground, and it is necessary to write the default values to the internal registers through the serial programming interface. The registers must be written in the following order.

Write 9000h (Address 9, Data 000)
 Write A000h (Address A, Data 000)
 Write B000h (Address B, Data 000)
 Write C000h (Address C, Data 000)
 Write D000h (Address D, Data 000)
 Write E000h (Address E, Data 804)
 Write 0000h (Address 0, Data 000)
 Write 1000h (Address 1, Data 000)
 Write F000h (Address F, Data 000)

NOTE: This procedure is only required if a RESET pulse is not provided to the device.

PowerPAD PACKAGE

The PowerPAD package is a thermally-enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the lead

frame die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the *Mechanical Data* section. The recommended thermal pad dimension is 8mm $\times$ 8mm.
2. Place a 5-by-5 array of thermal vias in the thermal pad area. These holes should be 13mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the application brief [SLMA004B](#) (*PowerPAD Made Easy*) or technical brief [SLMA002](#) (*PowerPAD Thermally Enhanced Package*).

Changes from B Revision (March 2006) to C Revision	Page
• Added MIN and MAX values for offset error and gain error, footnote for gain error.	3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5541IPAP	Active	Production	HTQFP (PAP) 64	160 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5541I
ADS5541IPAP.A	Active	Production	HTQFP (PAP) 64	160 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5541I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

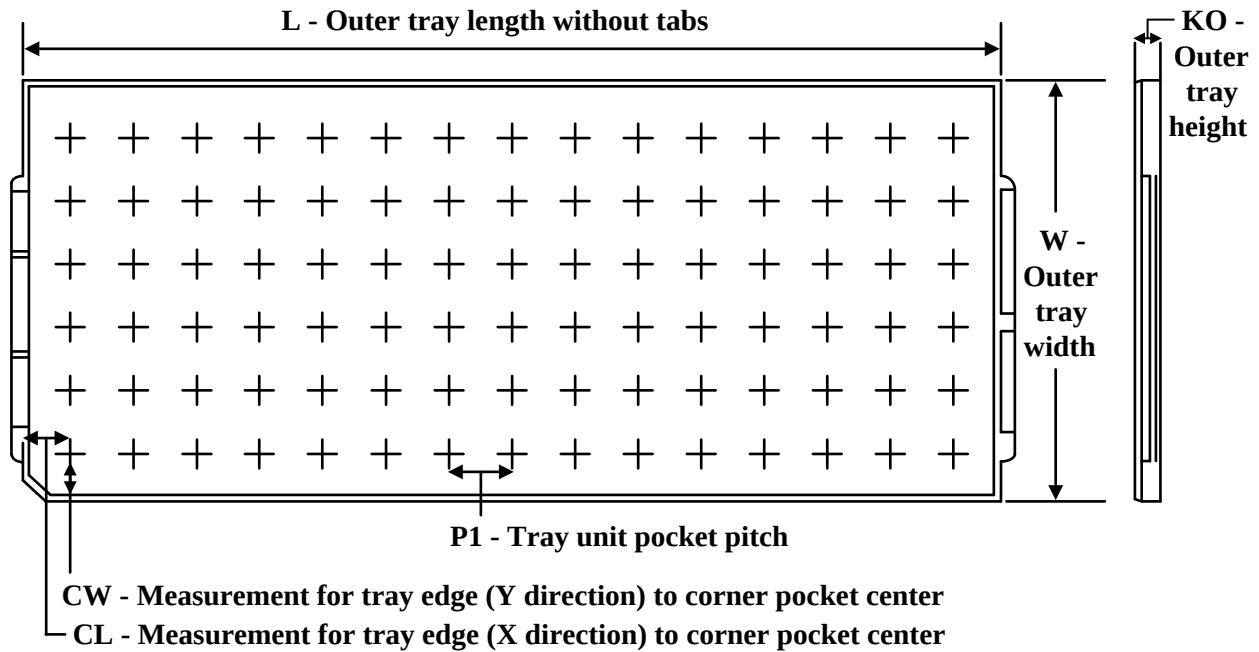
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
ADS5541IPAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS5541IPAP.A	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

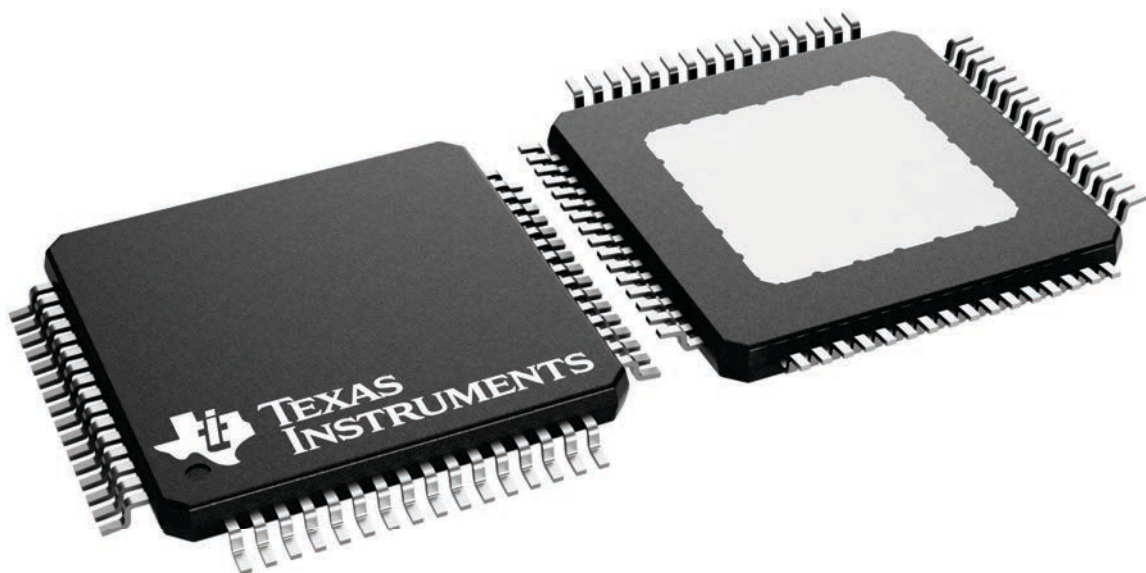
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

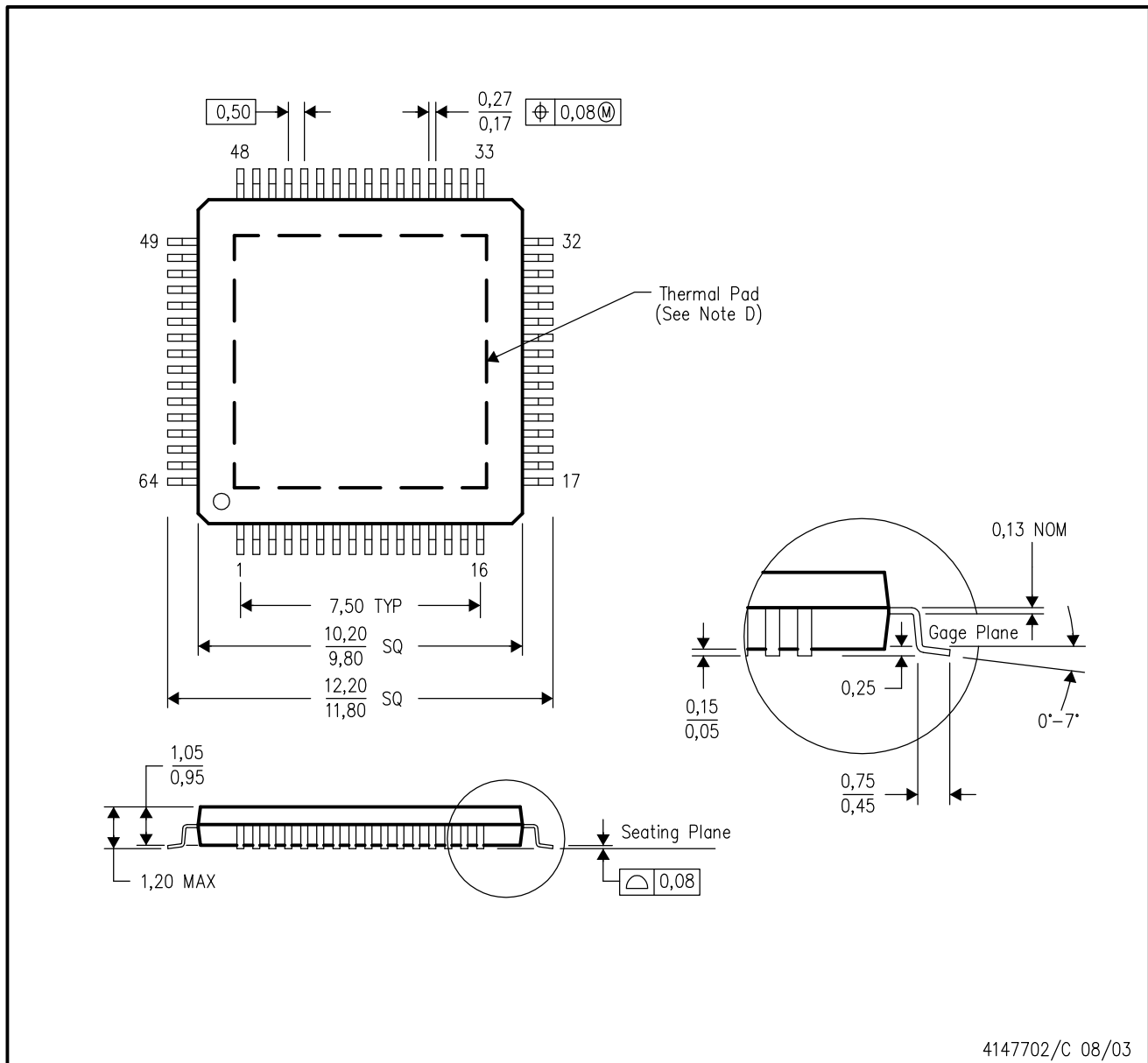
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PAP (S-PQFP-G64)

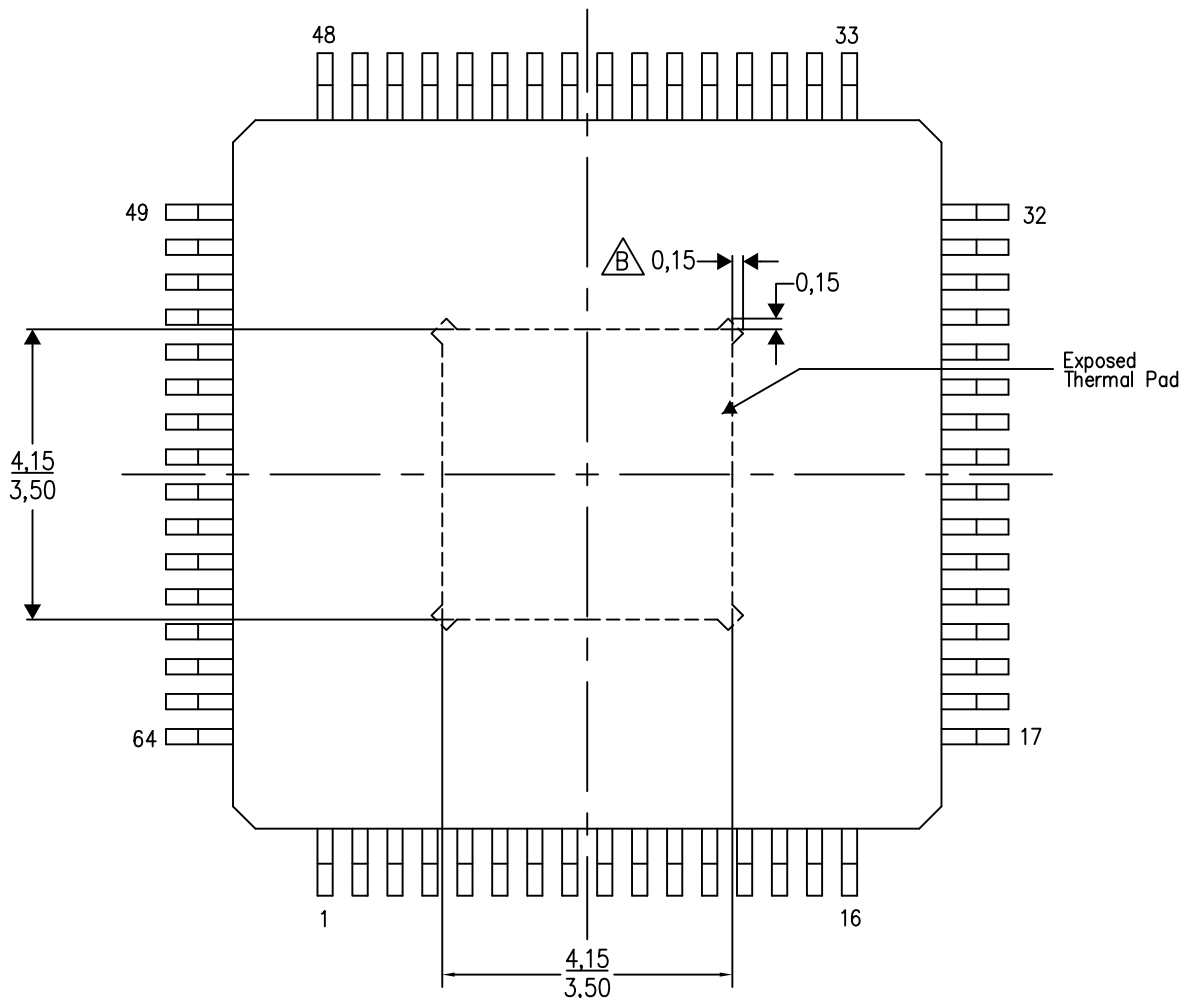
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206326-2/P 05/14

NOTES: A. All linear dimensions are in millimeters

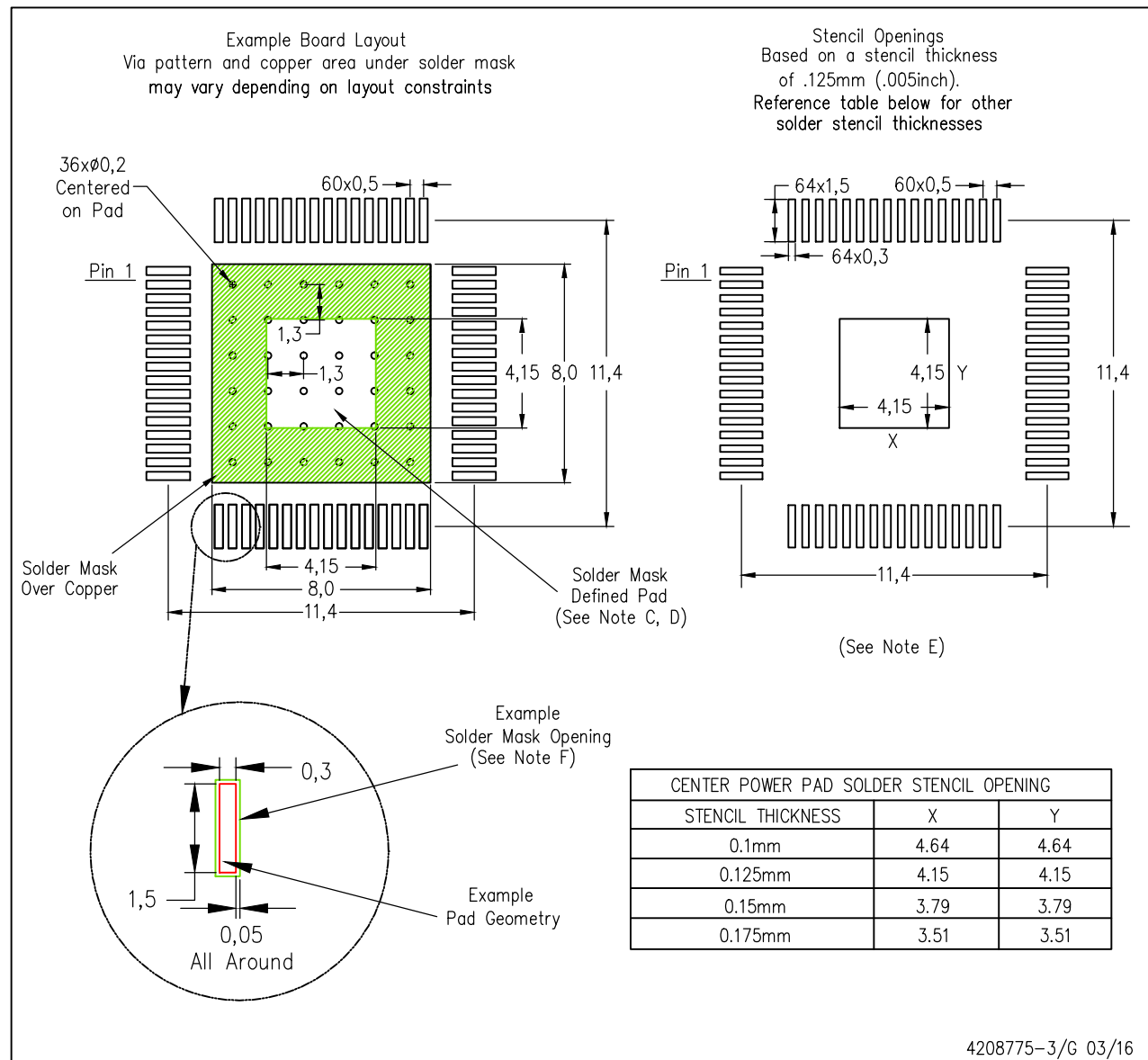
 Tie strap features may not be present.

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LAND PATTERN DATA

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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