

FEATURES

- Readback Capability for all DACs
- On-Chip Latches for All DACs
- Linearity Grades to $\pm 1/8$ LSB
- Single Supply Voltage (5 Volt)
- DACs Matched to 1%
- Four Quadrant Multiplication
- Microprocessor TTL/CMOS Compatible
- Latch-Up Free
- Dual Version: MP7529B

APPLICATIONS

- Microprocessor Controlled Gain and Attenuation Circuits
- Microprocessor Controlled/Programmable Power Supplies
- Hardware Redundant Applications Requiring Data Readback

GENERAL DESCRIPTION

The MP7628 is a quad 8-bit Digital-to-Analog Converter designed using a decoded DAC architecture featuring excellent DAC-to-DAC matching and guaranteed monotonicity.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

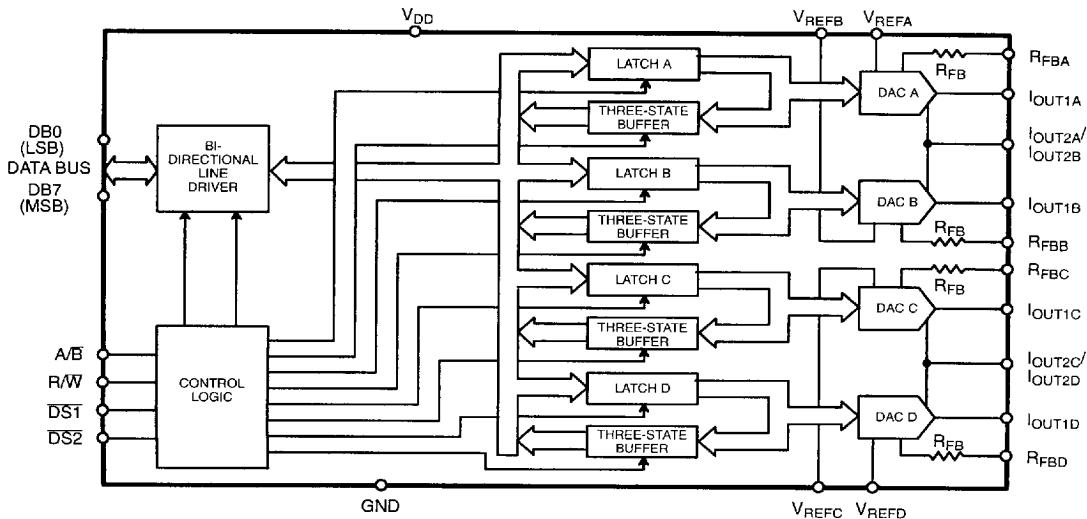
The readback function allows the user to poll or read the data latches, eliminating the need for storing information in RAM. In the event the microprocessor power supply is interrupted, it can poll the DACs to establish the last known system state.

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Data is transferred into any of the four DAC data latches via common 8-bit TTL/CMOS compatible input port. Control inputs DST, DS2 and A/B determine which DAC is to be loaded. The MP7628's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors.

The device operates at +5 V power supply and dissipates less than 5mW.

All DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

SIMPLIFIED BLOCK DIAGRAM


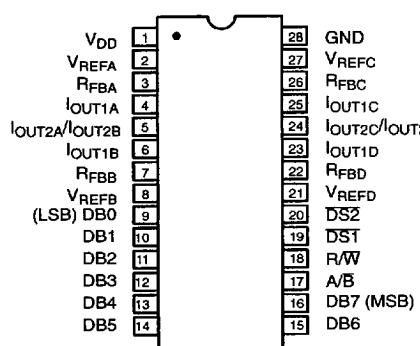
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP7628JN	$\pm 1/2$	$\pm 1/2$	± 1.8
Plastic Dip	-40 to +85°C	MP7628KN	$\pm 1/4$	$\pm 1/4$	± 0.9
SOIC	-40 to +85°C	MP7628JS	$\pm 1/2$	$\pm 1/2$	± 1.8
SOIC	-40 to +85°C	MP7628KS	$\pm 1/4$	$\pm 1/4$	± 0.9
PLCC	-40 to +85°C	MP7628JP	$\pm 1/2$	$\pm 1/2$	± 1.8
PLCC	-40 to +85°C	MP7628KP	$\pm 1/4$	$\pm 1/4$	± 0.9
Ceramic Dip	-40 to +85°C	MP7628AD	$\pm 1/2$	$\pm 1/2$	± 1.8
Ceramic Dip	-40 to +85°C	MP7628BD	$\pm 1/4$	$\pm 1/4$	± 0.9
Ceramic Dip	-55 to +125°C	MP7628SD*	$\pm 1/2$	$\pm 1/2$	± 1.8
Ceramic Dip	-55 to +125°C	MP7628TD*	$\pm 1/4$	$\pm 1/4$	± 0.9

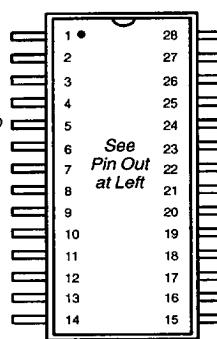
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

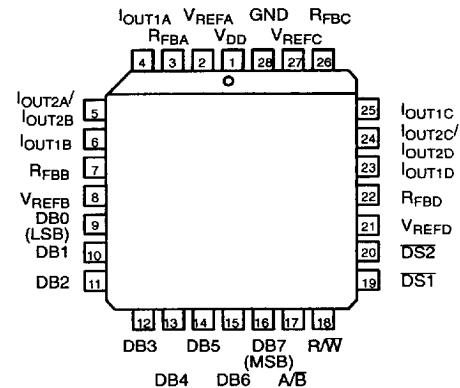
See Packaging Section for
Package Dimensions



28 Pin CDIP, PDIP (0.600")
D28, N28



28 Pin SOIC (Jedec, 0.300")
S28



28 Pin PLCC
P28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V _{DD}	Power Supply
2	V _{REFA}	Reference Voltage for DAC A
3	R _{FBA}	Feedback Resistor for DAC A
4	I _{OUT1A}	Current Output 1 DAC A
5	I _{OUT2A/OUT2B}	Current Output 2 DAC A/DAC B
6	I _{OUT1B}	Current Output 1 DAC B
7	R _{FBB}	Feedback Resistor for DAC B
8	V _{REFB}	Reference Voltage for DAC B
9	DB0	Data Input Bit 0 (LSB)
10	DB1	Data Input Bit 1
11	DB2	Data Input Bit 2
12	DB3	Data Input Bit 3
13	DB4	Data Input Bit 4
14	DB5	Data Input Bit 5
15	DB6	Data Input Bit 6
16	DB7	Data Input Bit 7 (MSB)
17	A/B	DAC Selection
18	R/W	Read/Write
19	DS1	Control 1
20	DS2	Control 2
21	V _{REFD}	Reference Voltage for DAC D
22	R _{FBD}	Feedback Resistor for DAC D
23	I _{OUT1D}	Current Output 1 DAC D
24	I _{OUT2C/OUT2D}	Current Output 2 DAC C/DAC D
25	I _{OUT1C}	Current Output 1 DAC C
26	R _{FBC}	Feedback Resistor for DAC C
27	V _{REFC}	Reference Voltage for DAC C
28	GND	Ground

MP7628

EXAR

ELECTRICAL CHARACTERISTICS ($V_{DD} = +5$ V, $V_{REF} = +10$ V unless otherwise noted)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
STATIC PERFORMANCE¹								
Resolution (All Grades)	N	8			8		Bits	FSR = Full Scale Range
Integral Non-Linearity (Relative Accuracy) J, A, S K, B, T	INL		$\pm 1/2$ $\pm 1/4$		$\pm 1/2$ $\pm 1/4$		LSB	End Point Linearity Spec.
Differential Non-Linearity J, A, S K, B, T	DNL		$\pm 1/2$ $\pm 1/4$		$\pm 1/2$ $\pm 1/4$		LSB	All grades monotonic over full temperature range.
Gain Error J, A, S K, B, T	GE		± 1.5 ± 0.8		± 1.8 ± 0.9		% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Gain Temperature Coefficient ²	TC _{GE}				± 2		ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		± 200		± 400		ppm/%	ΔGain/Δ V_{DD} $\Delta V_{DD} = \pm 5\%$ Digital Inputs = V_{INH}
Output Leakage Current (all)	I _{OUT1}		± 50		± 200		nA	Digital Inputs = V_{INL}
REFERENCE INPUT								
Voltage Range ² Input Resistance	R _{IN}	12	± 20 28		12	± 20 28	V kΩ	
DIGITAL INPUTS³								
Logic Thresholds V_{INH} V_{INL}		2.4		0.8	2.4		V V	
Input Leakage Current	I _{LKG}		3	± 1		± 10	μA pF	
Input Capacitance ²	C _{IN}							
DATA BUS OUTPUTS								
Output Capacitance ² Input Leakage Current	C _{OUT} I _{LKG}		7	± 1		± 10	pF μA	
ANALOG OUTPUTS								
Propagation Delay ²		500			750		ns	From digital input to 90% of final analog output current
Output Capacitance ²	C _{OUT}		120				pF	DAC Inputs all 1's
Glitch Energy ²	C _{OUT}	160	80		440		pF nVs	DAC Inputs all 0's Typical for code transition from all 0's to all 1's

ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
POWER SUPPLY⁵								
Functional Voltage Range ² Supply Current	V _{DD} I _{DD}	4.5	5.5	50	4.5	5.5	V μA	All digital inputs = 0 V or all = 5 V
SWITCHING CHARACTERISTICS^{2, 4}								
Data Write Time Write Strobe Req. Data Hold Time Data Read Time 3-state Hold Time Read Strobe Req.	t _W t _{DSW} t _{DHLD} t _R t _{TSHD} t _{DSR}	320 200 40 480 240 320			400 250 50 600 300 400		ns ns ns ns ns ns	

NOTES:

- 1 Full Scale Range (FSR) is 10V for unipolar mode.
- 2 Guaranteed but not production tested.
- 3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 See timing diagrams.
- 5 Specified values guarantee functionality. Refer to other parameters for accuracy.

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Specifications are subject to change without notice

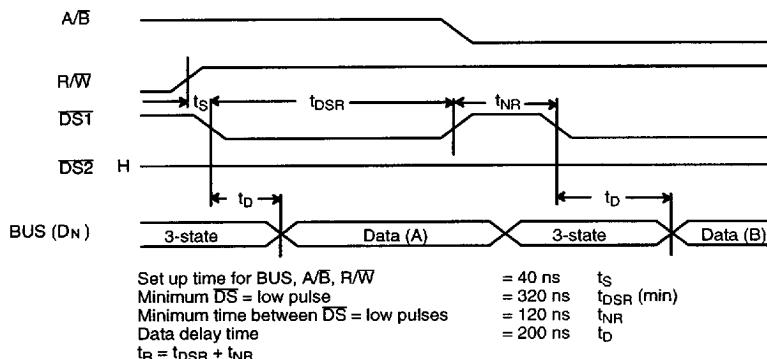
ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2}

V _{DD} to GND	+7 V	Storage Temperature	-65°C to +150°C
Digital Input Voltage to GND (2)	GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds)	+300°C
I _{OUT1} , I _{OUT2} to GND (2)	GND -0.5 to V _{DD} +0.5 V	Package Power Dissipation Rating to 75°C	
V _{REF} to GND	±25 V	CDIP, PDIP, SOIC, PLCC	1050mW
V _{RFB} to GND	±25 V	Derates above 75°C	14mW/°C

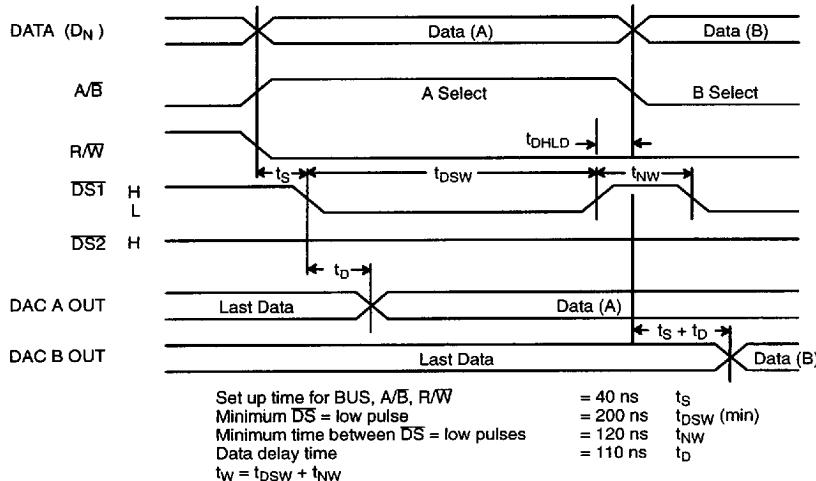
NOTES:

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

TIMING DIAGRAM READ CYCLE



TIMING DIAGRAM WRITE CYCLE



MODE SELECTION TABLE

DS1	DS2	A/B	R/W	MODE	DAC
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A & C
L	L	L	L	WRITE	B & D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = LOW STATE
 H = HIGH STATE
 X = DON'T CARE

INTERFACE LOGIC INFORMATION

DAC Selection: All DAC latches share a common 8-bit input port. The control inputs \overline{DS} , $\overline{DS2}$, A/B select which DAC can accept data from the input port.

Mode Selection: Inputs \overline{DS} and R/W control the operating mode of the selected DAC. *See Mode Selection Table on the previous page.*

Write Mode: When \overline{DS} and R/W are both low the selected DAC is in the write mode. The input data latches of the selected

DAC are transparent and its analog output responds to activity on DB0-DB7.

Hold Mode: The selected DAC latch retains the data which was present on DB0-DB7 just prior to \overline{DS} and R/W assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When \overline{DS} is low and R/W is high, the selected DAC is in the read mode and the data held in the appropriate latch is outputted to the data bus.

APPLICATION NOTES

Refer to Section 8 for Applications Information