

SN74ALVC162268

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES051 – AUGUST 1995

- B-Port Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments **Widebus™** Family
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALVC162268 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus. This device is designed specifically for low-voltage (3.3-V) V_{CC} operation; it is tested at 2.5-V, 2.7-V, and 3.3-V V_{CC} .

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

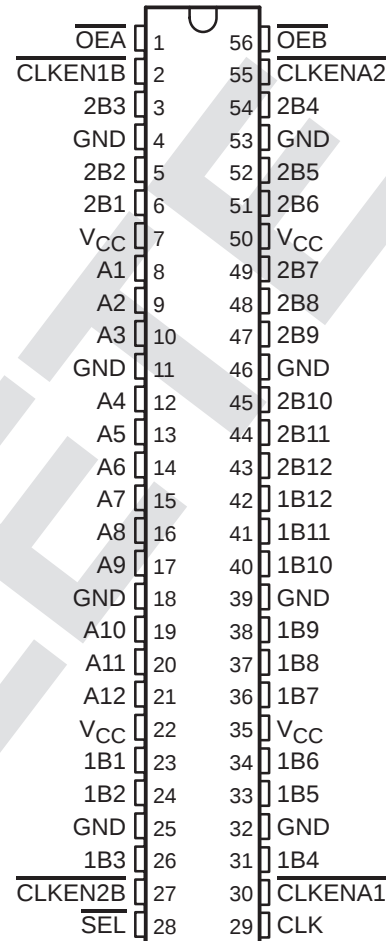
For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB}$). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include 26- Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC162268 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

SN74ALVC162268

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES051 – AUGUST 1995

Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B ₀ [†]	2B ₀ [†]
L	X	↑	L	L [†]	X
L	X	↑	H	H [†]	X
X	L	↑	L	X	L
X	L	↑	H	X	H

[†] Two CLK edges are needed to propagate data.

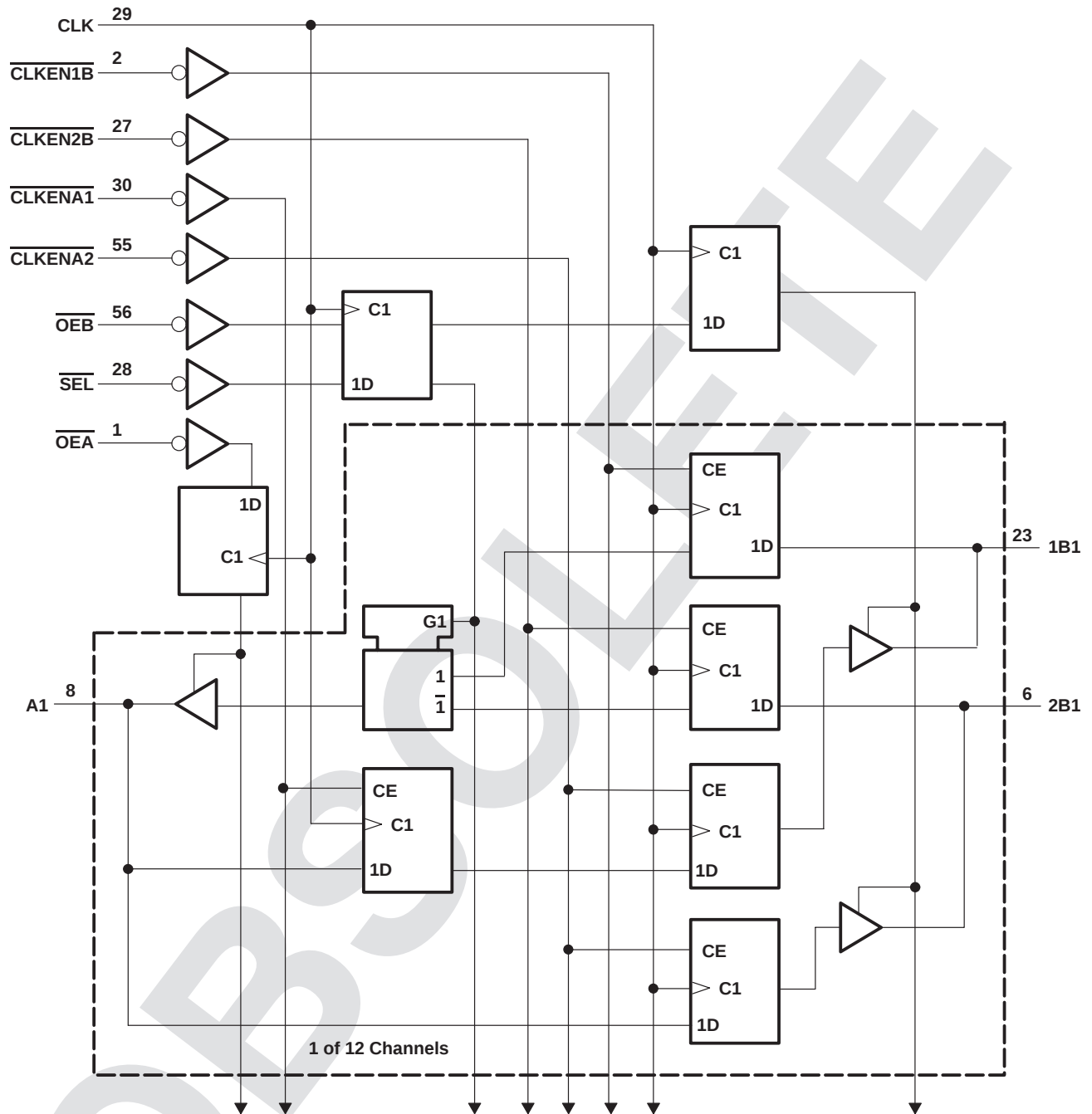
[‡] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS						OUTPUT A
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	
H	X	X	H	X	X	A ₀ [‡]
X	H	X	L	X	X	A ₀ [‡]
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



SN74ALVC162268

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES051 – AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive-voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current on the B port	V _{CC} = 2.3 V		−6	mA
		V _{CC} = 2.7 V		−8	
		V _{CC} = 3 V		−12	
I _{OL}	Low-level output current on the B port	V _{CC} = 2.3 V		6	mA
		V _{CC} = 2.7 V		8	
		V _{CC} = 3 V		12	
I _{OH}	High-level output current on the A port	V _{CC} = 2.3 V		−12	mA
		V _{CC} = 2.7 V		−12	
		V _{CC} = 3 V		−24	
I _{OL}	Low-level output current on the A port	V _{CC} = 2.3 V		12	mA
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVC162268
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS
SCES051 – AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	T _A = –40°C to 85°C			UNIT
				MIN	TYP [‡]	MAX	
V _{OH} (B port)	I _{OH} = –100 μA		MIN to MAX	V _{CC} –0.2			V
	I _{OH} = –4 mA, V _{IH} = 1.7 V		2.3 V	1.9			
	I _{OH} = –6 mA	V _{IH} = 1.7 V	2.3 V	1.7			
		V _{IH} = 2 V	3 V	2.4			
	I _{OH} = –8 mA, V _{IH} = 2 V		2.7 V	2			
I _{OH} = –12 mA, V _{IH} = 2 V		3 V	2				
V _{OL} (B port)	I _{OL} = 100 μA		MIN to MAX	0.2			V
	I _{OL} = 4 mA, V _{IL} = 0.7 V		2.3 V	0.4			
	I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V	0.55			
		V _{IL} = 0.8 V	3 V	0.55			
	I _{OL} = 8 mA, V _{IL} = 0.8 V		2.7 V	0.6			
I _{OL} = 12 mA, V _{IL} = 0.8 V		3 V	0.8				
V _{OH} (A port)	I _{OH} = –100 μA		MIN to MAX	V _{CC} –0.2			V
	I _{OH} = –6 mA, V _{IH} = 1.7 V		2.3 V	2			
	I _{OH} = –12 mA	V _{IH} = 1.7 V	2.3 V	1.7			
		V _{IH} = 2 V	2.7 V	2.2			
		V _{IH} = 2 V	3 V	2.4			
I _{OH} = –24 mA, V _{IH} = 2 V		3 V	2				
V _{OL} (A port)	I _{OL} = 100 μA		MIN to MAX	0.2			V
	I _{OL} = 6 mA, V _{IL} = 0.7 V		2.3 V	0.4			
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V	0.7			
		V _{IL} = 0.8 V	2.7 V	0.4			
	I _{OL} = 24 mA, V _{IL} = 0.8 V		3 V	0.55			
I _I		V _I = V _{CC} or GND	3.6 V	±5			μA
I _I (hold)	V _I = 0.7 V		2.3 V	45			μA
	V _I = 1.7 V			–45			
	V _I = 0.8 V		3 V	75			
	V _I = 2 V			–75			
	V _I = 0 to 3.6 V		3.6 V	±500			
I _{OZ} [§]		V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	40			μA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	9			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V.

[§] For I/O ports, the parameter I_{OZ} includes the input-leakage current.

SN74ALVC162268
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES051 – AUGUST 1995

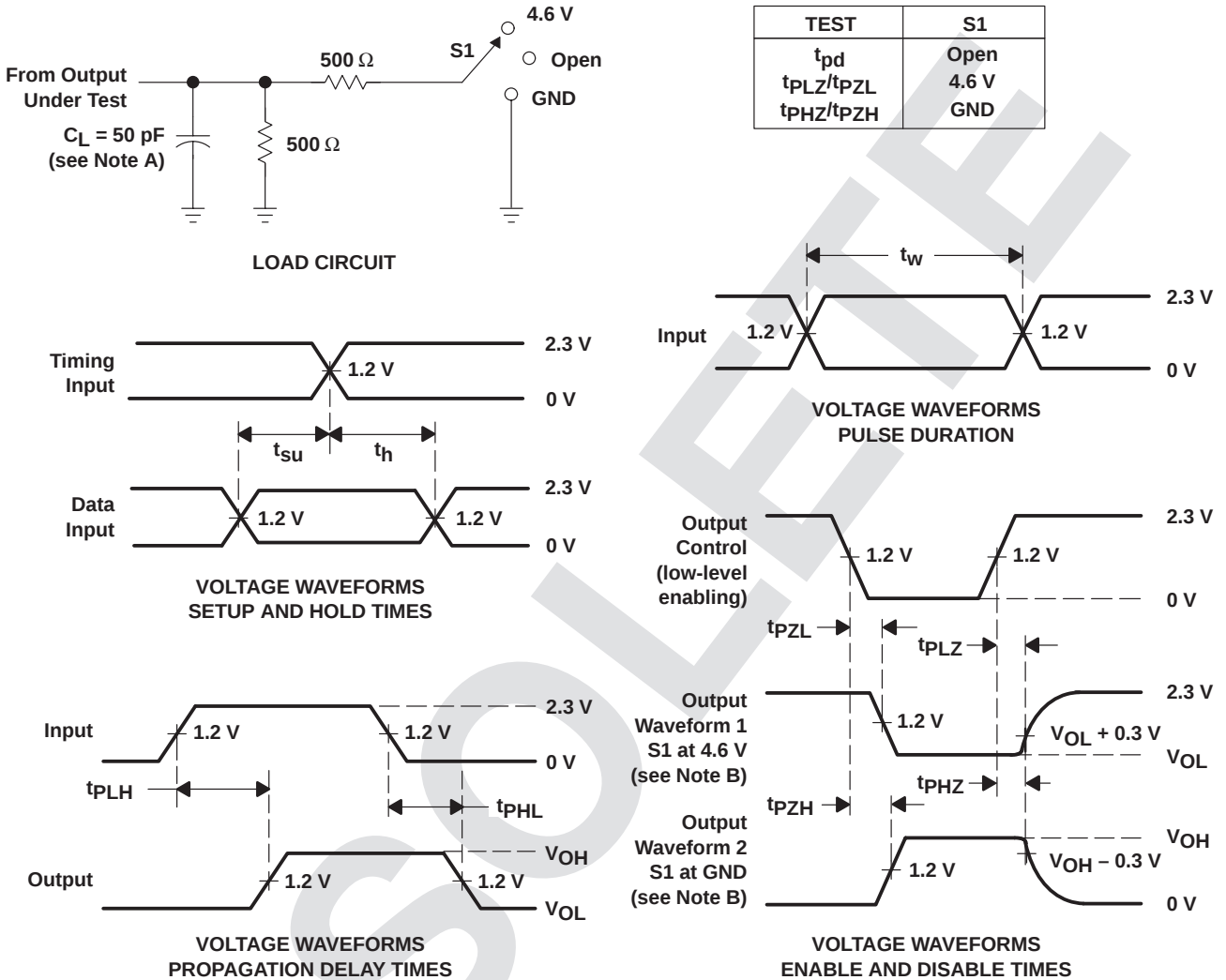
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			120		125		150		MHz
t _w	Pulse duration, CLK High or low			3.3		3.3		3.3		ns
t _{su}	Setup time	A data before CLK↑	High or low	4.5		4		3.4		ns
		B data before CLK↑	High or low	0.8		1.2		1		
		<u>SEL</u> before CLK↑	High or low	1.4		1.6		1.3		
		<u>CLKENA1</u> or <u>CLKENA2</u> before CLK↑	High or low	3.6		3.4		2.8		
		<u>CLKENB1</u> or <u>CLKENB2</u> before CLK↑	High or low	3.2		3		2.5		
		<u>OE</u> before CLK↑	High or low	4.2		3.9		3.2		
t _h	Hold time	A data after CLK↑	High or low	0		0		0.2		ns
		B data after CLK↑	High or low	1.3		1.2		1.3		
		<u>SEL</u> after CLK↑	High or low	1		1		1		
		<u>CLKENA1</u> or <u>CLKENA2</u> after CLK↑	High or low	0.1		0.1		0.4		
		<u>CLKENB1</u> or <u>CLKENB2</u> after CLK↑	High or low	0.1		0		0.5		
		<u>OE</u> after CLK↑	High or low	0		0		0.2		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			120		125		150		ns
t_{pd}	CLK	B	2.1	6.7	5.9		1.8	5.4	ns
t_{pd}	CLK	A (1B)	2.1	6.4	5.4		1.7	4.8	ns
t_{pd}	CLK	A (2B)	2.1	6.4	5.3		1.8	4.8	ns
t_{pd}	CLK	A ($\overline{\text{SEL}}$)	3	7.9	6.5		2.4	5.8	ns
t_{en}	CLK	B	2.8	7.7	6.8		2.6	6.1	ns
t_{dis}	CLK	B	3.5	7.4	6.1		2.5	5.9	ns
t_{en}	CLK	A	2.1	6.7	5.6		1.8	5.1	ns
t_{dis}	CLK	A	2.7	6.7	5.4		2.1	5	ns

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74ALVC162268

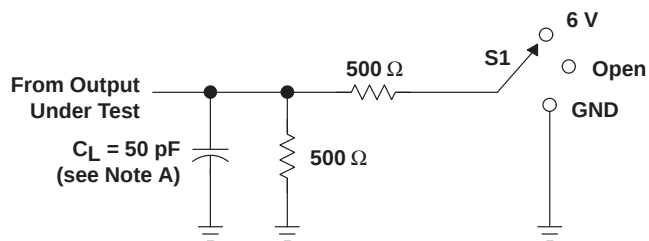
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES051 – AUGUST 1995

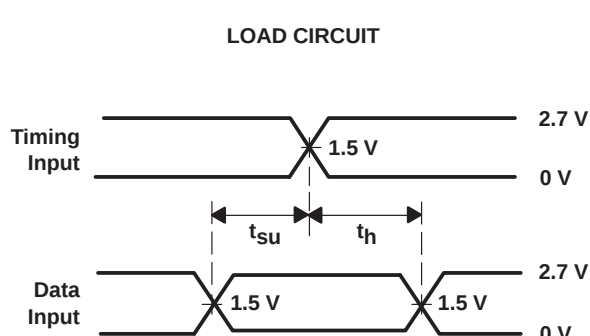
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

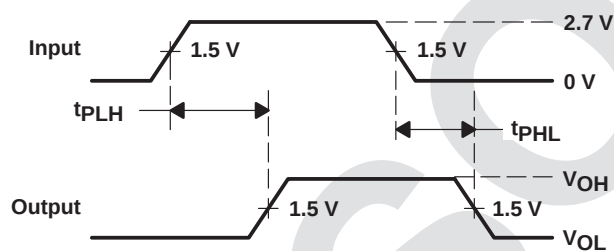


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



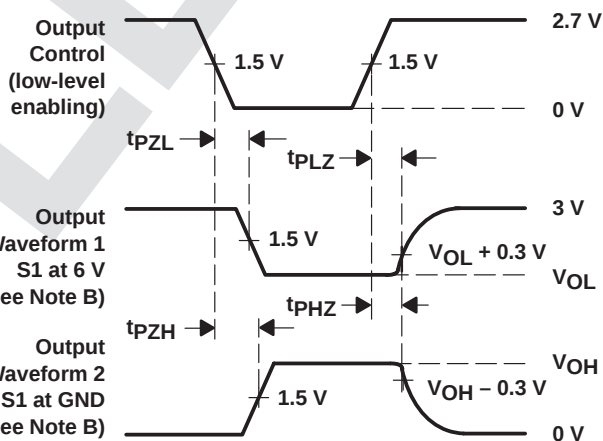
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALVC162268DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
SN74ALVC162268DLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

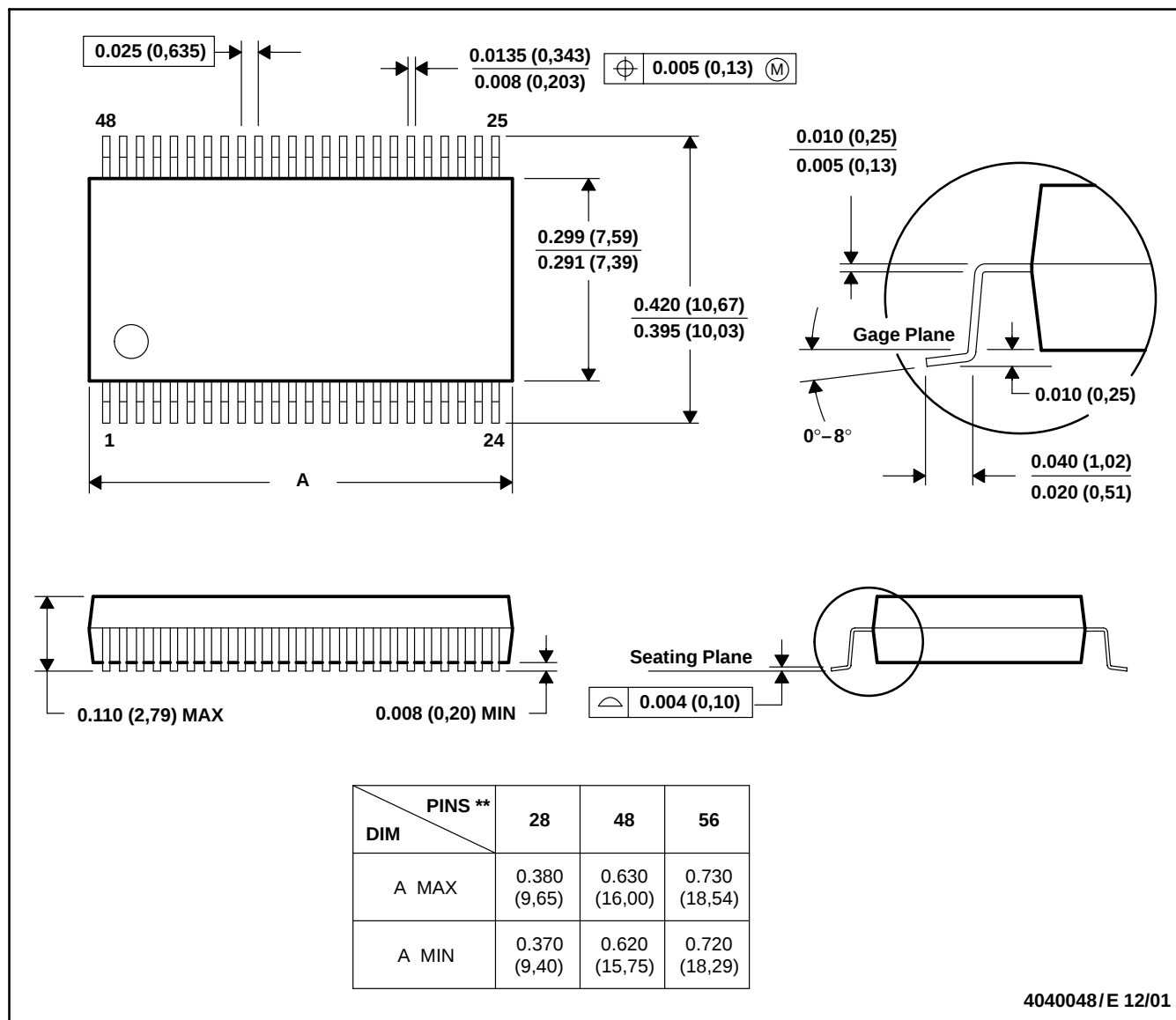
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated