

HIP2101

100V/2A Peak, Low Cost, High Frequency Half Bridge Driver

FN9025

Rev 9.00

November 12, 2015

The HIP2101 is a high frequency, 100V Half Bridge N-Channel power MOSFET driver IC. It is equivalent to the HIP2100 with the added advantage of full TTL/CMOS compatible logic input pins. The low-side and high-side gate drivers are independently controlled and matched to 13ns. This gives users total control over dead-time for specific power circuit topologies. Undervoltage protection on both the low-side and high-side supplies force the outputs low. An on-chip diode eliminates the discrete diode required with other driver ICs. A new level-shifter topology yields the low-power benefits of pulsed operation with the safety of DC operation. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP2101IB (No longer available, recommended replacement: HIP2101IBZ)	-40 to 125	8 Ld SOIC	M8.15
HIP2101IBZ (Note 1)	-40 to 125	8 Ld SOIC (Pb-free)	M8.15
HIP2101EIB (No longer available, recommended replacement: HIP2101EIBZ)	-40 to 125	8 Ld EPOIC	M8.15C
HIP2101EIBZ (Note 1)	-40 to 125	8 Ld EPOIC (Pb-free)	M8.15C
HIP2101IRZ (Note 1)	-40 to 125	16 Ld 5x5 QFN (Pb-free)	L16.5x5
HIP2101IR4Z (Note 1)	-40 to 125	12 Ld 4x4 DFN (Pb-free)	L12.4x4A

NOTES:

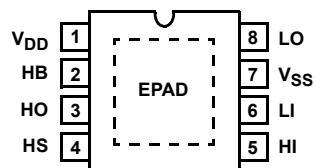
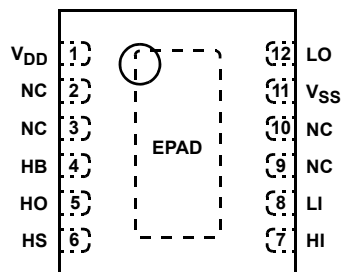
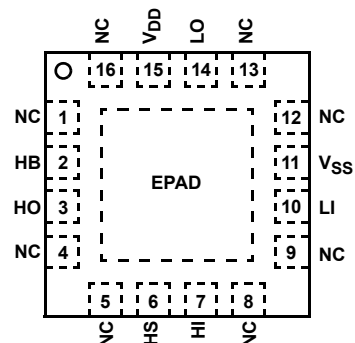
- Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.
- Add "T" suffix for Tape and Reel packing option.

Features

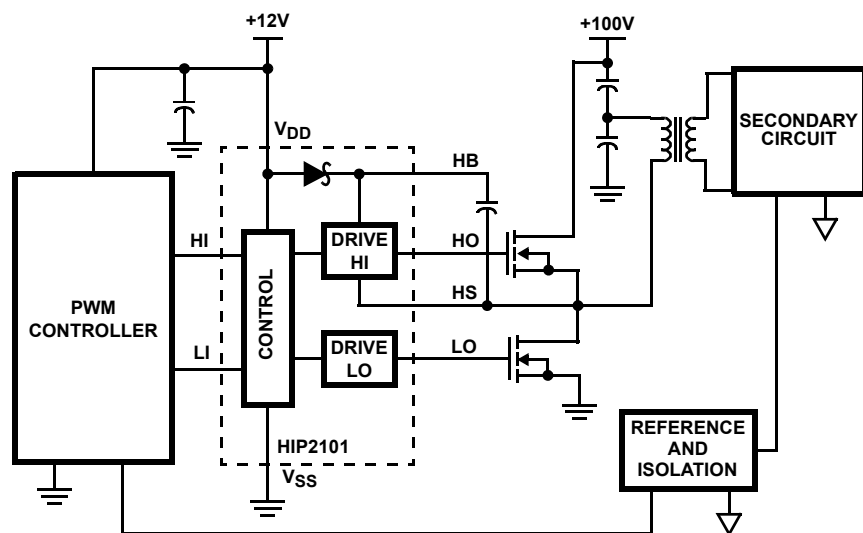
- Drives N-Channel MOSFET Half Bridge
- SOIC, EPOIC, QFN and DFN Package Options
- SOIC, EPOIC and DFN Packages Compliant with 100V Conductor Spacing Guidelines of IPC-2221
- Pb-free Product Available (RoHS Compliant)
- Bootstrap Supply Max Voltage to 114VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times for Multi-MHz Circuits
- Drives 1000pF Load with Rise and Fall Times Typ. 10ns
- TTL/CMOS Input Thresholds Increase Flexibility
- Independent Inputs for Non-Half Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 3Ω Output Driver Resistance
- QFN/DFN Package:
 - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
 - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile

Applications

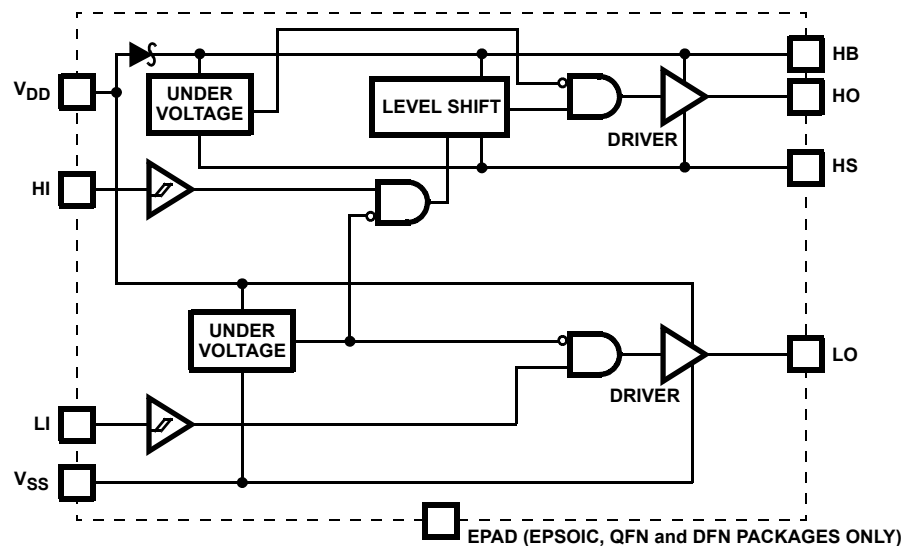
- Telecom Half Bridge Power Supplies
- Avionics DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

Pinouts**HIP2101 (SOIC, EPSOIC)**
TOP VIEW**HIP2101IR4 (DFN)**
TOP VIEW**HIP2101 (QFN)**
TOP VIEW

NOTE: EPAD = Exposed PAD.

Application Block Diagram

Functional Block Diagram



*EPAD = Exposed Pad. The EPAD is electrically isolated from all other pins. For best thermal performance connect the EPAD to the PCB power ground plane.

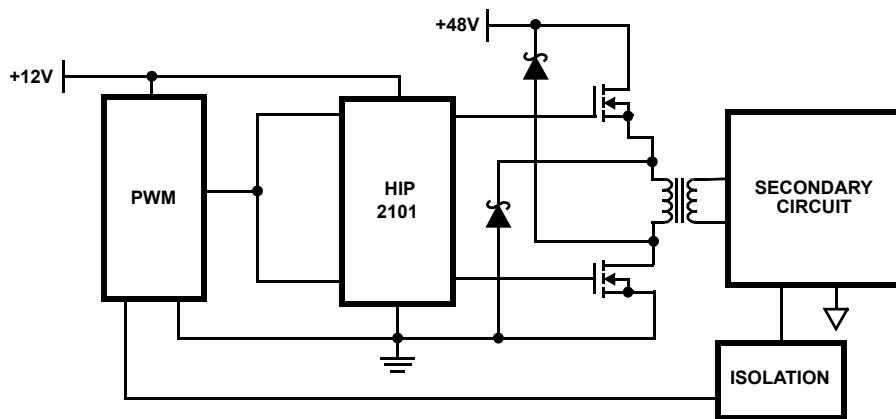


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

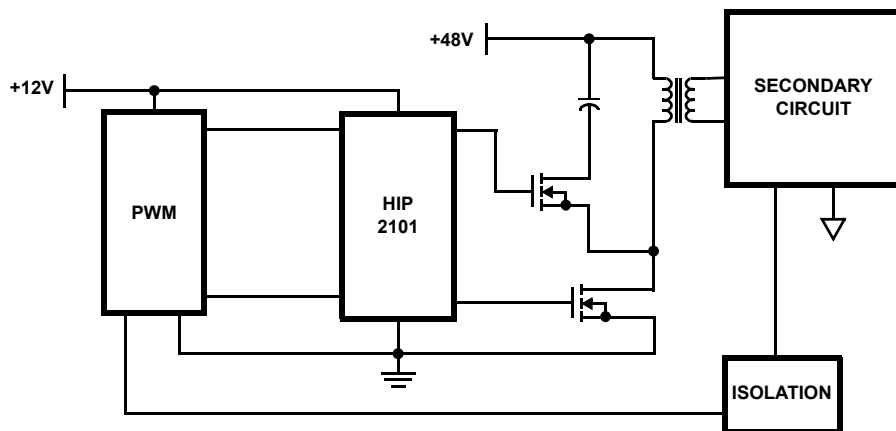


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP

Absolute Maximum Ratings

Supply Voltage, V_{DD} , V_{HB} - V_{HS} (Notes 3, 4) -0.3V to 18V
 LI and HI Voltages (Note 4) -0.3V to 7.0V
 Voltage on LO (Note 4) -0.3V to V_{DD} +0.3V
 Voltage on HO (Note 4) V_{HS} -0.3V to V_{HB} +0.3V
 Voltage on HS (Continuous) (Note 4) -1V to 110V
 Voltage on HB (Note 4) +118V
 Average Current in V_{DD} to HB diode 100mA
 ESD Classification Class 1 (1kV)

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD} +9V to 14.0VDC
 Voltage on HS -1V to 100V
 Voltage on HS (Repetitive Transient) -5V to 105V
 Voltage on HB V_{HS} +8V to V_{HS} +14.0V and V_{DD} -1V to V_{DD} +100V
 HS Slew Rate <50V/ns

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W) θ_{JC} (°C/W)
 SOIC (Note 5) 95 N/A
 EPSON (Note 6) 40 3.0
 QFN (Note 6) 37 6.5
 DFN (Note 6) 40 3.0
 Max Power Dissipation at 25°C in Free Air (SOIC, Note 5) 1.3W
 Max Power Dissipation at 25°C in Free Air (EPSON, Note 6) . . . 3.1W
 Max Power Dissipation at 25°C in Free Air (QFN, Note 6) 3.3W
 Storage Temperature Range -65°C to 150°C
 Junction Temperature Range -55°C to 150°C
 Lead Temperature (Soldering 10s - SOIC Lead Tips Only) . . . 300°C
 For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

NOTES:

- The HIP2101 is capable of derated operation at supply voltages exceeding 14V. Figure 16 shows the high-side voltage derating curve for this mode of operation.
- All voltages referenced to V_{SS} unless otherwise specified.
- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC} , the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	T _J = 25°C			T _J = -40°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS								
V _{DD} Quiescent Current	I _{DD}	LI = HI = 0V	-	0.3	0.45	-	0.6	mA
V _{DD} Operating Current	I _{DDO}	f = 500kHz	-	1.7	3.0	-	3.4	mA
Total HB Quiescent Current	I _{HB}	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	I _{HBO}	f = 500kHz	-	1.5	2.5	-	3	mA
HB to V _{SS} Current, Quiescent	I _{HBS}	V _{HS} = V _{HB} = 114V	-	0.05	1.5	-	10	μA
HB to V _{SS} Current, Operating	I _{HBSO}	f = 500kHz	-	0.7	-	-	-	mA
INPUT PINS								
Low Level Input Voltage Threshold	V _{IL}		0.8	1.65	-	0.8	-	V
High Level Input Voltage Threshold	V _{IH}		-	1.65	2.2	-	2.2	V
Input Pulldown Resistance	R _I		-	200	-	100	500	kΩ
UNDER VOLTAGE PROTECTION								
V _{DD} Rising Threshold	V _{DDR}		7	7.3	7.8	6.5	8	V
V _{DD} Threshold Hysteresis	V _{DDH}		-	0.5	-	-	-	V
HB Rising Threshold	V _{HBR}		6.5	6.9	7.5	6	8	V
HB Threshold Hysteresis	V _{HBH}		-	0.4	-	-	-	V

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	T _J = 25°C			T _J = -40°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
BOOT STRAP DIODE								
Low-Current Forward Voltage	V _{DL}	I _{VDD-HB} = 100μA	-	0.45	0.70	-	0.7	V
High-Current Forward Voltage	V _{DH}	I _{VDD-HB} = 100mA	-	0.7	0.92	-	1	V
Dynamic Resistance	R _D	I _{VDD-HB} = 100mA	-	0.8	1	-	1.5	Ω
LO GATE DRIVER								
Low Level Output Voltage	V _{OLL}	I _{LO} = 100mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V _{OHL}	I _{LO} = -100mA, V _{OHL} = V _{DD} -V _{LO}	-	0.25	0.3	-	0.4	V
Peak Pullup Current	I _{OHL}	V _{LO} = 0V	-	2	-	-	-	A
Peak Pulldown Current	I _{OLL}	V _{LO} = 12V	-	2	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V _{OLH}	I _{HO} = 100mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V _{OHH}	I _{HO} = -100mA, V _{OHH} = V _{HB} -V _{HO}	-	0.25	0.3	-	0.4	V
Peak Pullup Current	I _{OHH}	V _{HO} = 0V	-	2	-	-	-	A
Peak Pulldown Current	I _{OLH}	V _{HO} = 12V	-	2	-	-	-	A

Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ C$			$T_J = -40^\circ C \text{ TO } 125^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	25	43	-	56	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	25	43	-	56	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	25	43	-	56	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	25	43	-	56	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	t_{MON}		-	2	13	-	16	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	t_{MOFF}		-	2	13	-	16	ns
Either Output Rise/Fall Time	t_{RC}, t_{FC}	$C_L = 1000pF$	-	10	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V)	t_R, t_F	$C_L = 0.1\mu F$	-	0.5	0.6	-	0.8	us
Either Output Rise Time Driving DMOS	t_{RD}	$C_L = IRFR120$	-	20	-	-	-	ns
Either Output Fall Time Driving DMOS	t_{FD}	$C_L = IRFR120$	-	10	-	-	-	ns
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

Pin Descriptions

SYMBOL	DESCRIPTION
V _{DD}	Positive Supply to lower gate drivers. De-couple this pin to V _{SS} . Bootstrap diode connected to HB.
HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
HO	High-Side Output. Connect to gate of High-Side power MOSFET.
HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	High-Side input.
LI	Low-Side input.
V _{SS}	Chip negative supply, generally will be ground.
LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.
EPAD	Exposed pad. Connect to ground or float. The EPAD is electrically isolated from all other pins.

Timing Diagrams

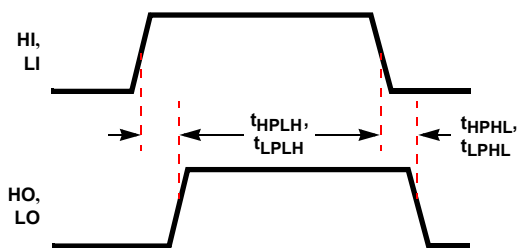


FIGURE 3.

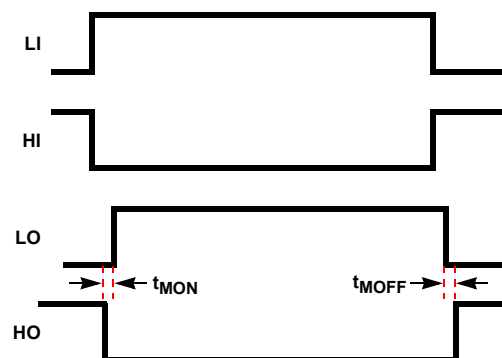


FIGURE 4.

Typical Performance Curves

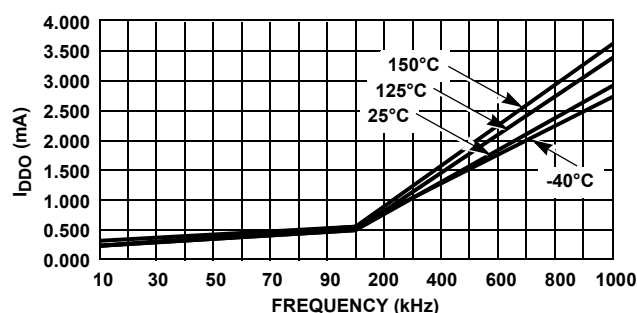


FIGURE 5A.

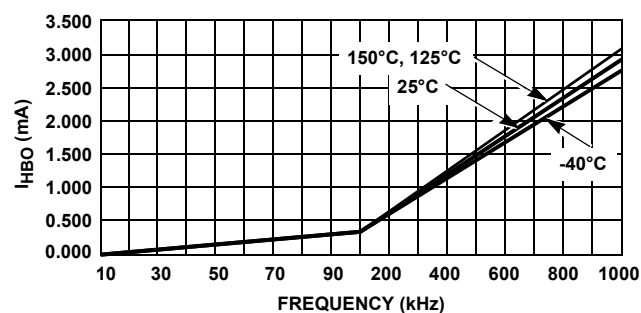


FIGURE 5B.

FIGURE 5. OPERATING CURRENT vs FREQUENCY

Typical Performance Curves (Continued)

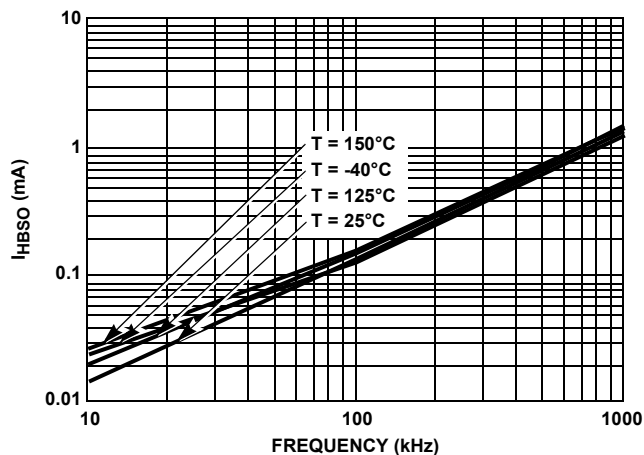


FIGURE 6. HB TO VSS OPERATING CURRENT vs FREQUENCY

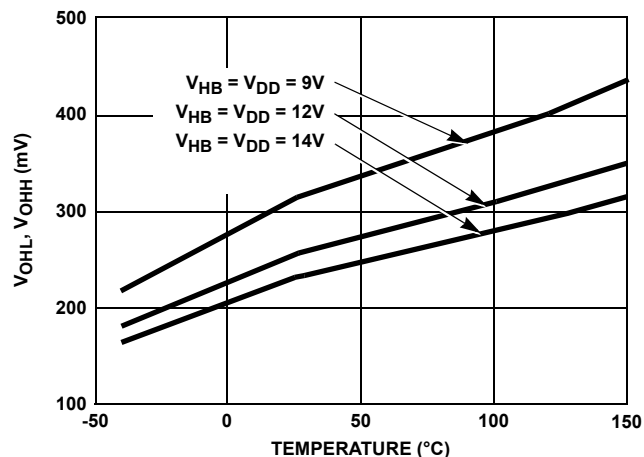


FIGURE 7. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

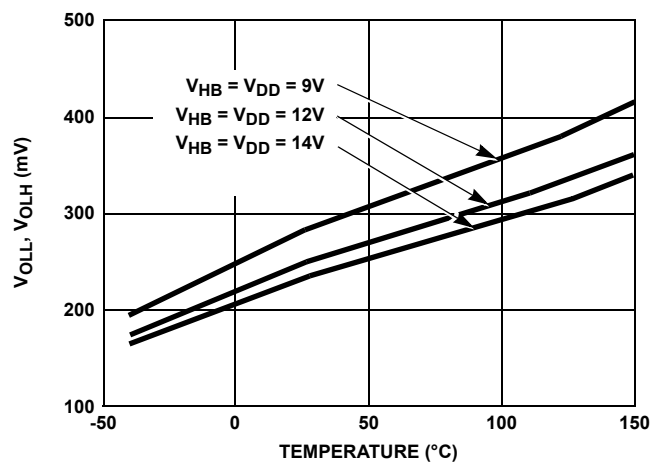


FIGURE 8. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

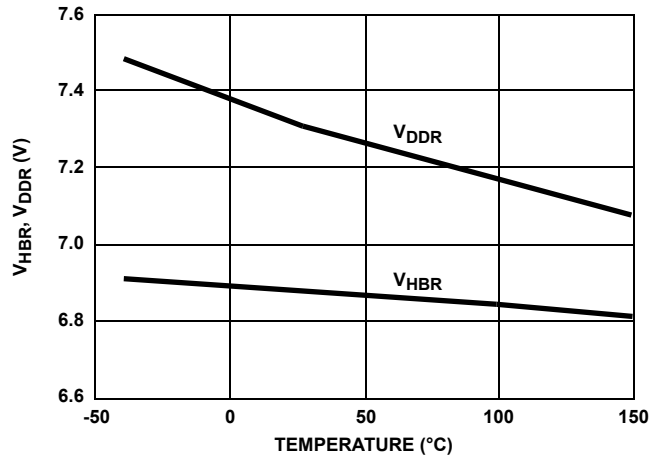


FIGURE 9. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

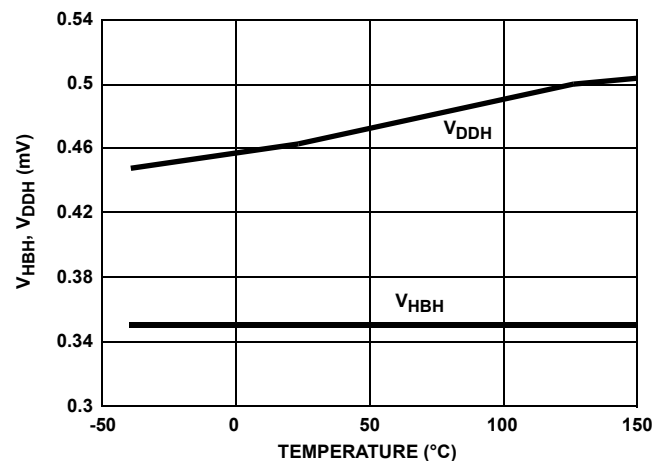


FIGURE 10. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

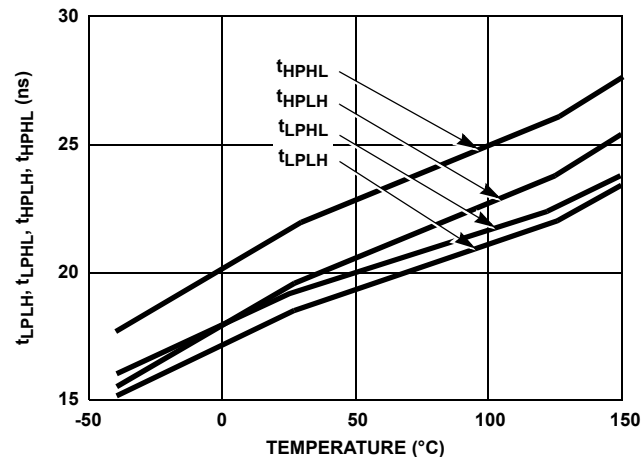


FIGURE 11. PROPAGATION DELAYS vs TEMPERATURE

Typical Performance Curves (Continued)

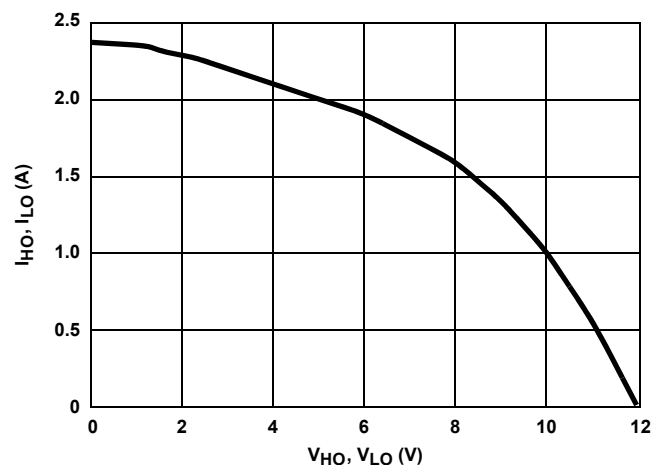


FIGURE 12. PEAK PULLUP CURRENT vs OUTPUT VOLTAGE

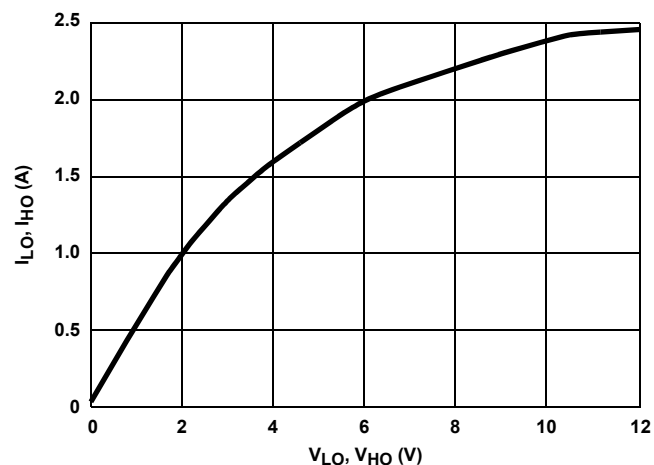


FIGURE 13. PEAK PULLDOWN CURRENT vs OUTPUT VOLTAGE

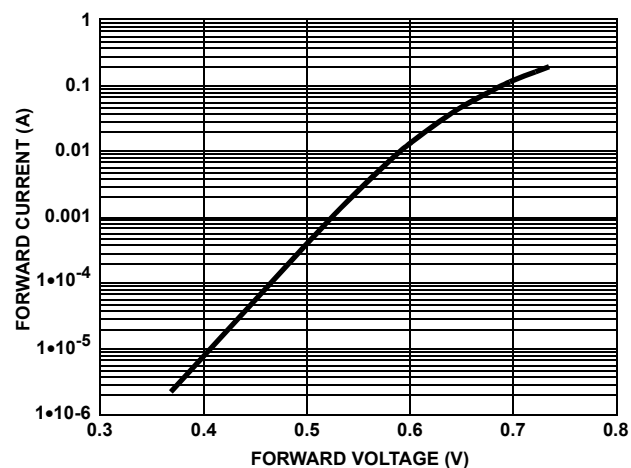


FIGURE 14. BOOTSTRAP DIODE I-V CHARACTERISTICS

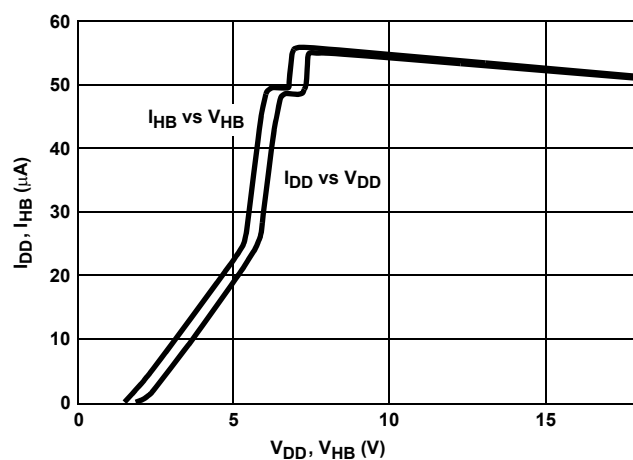
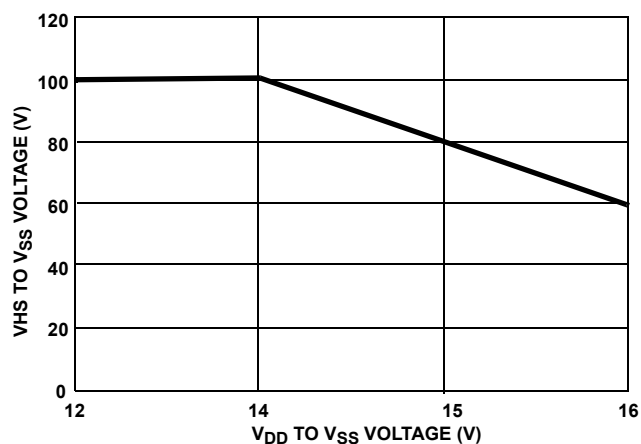


FIGURE 15. QUIESCENT CURRENT vs VOLTAGE

FIGURE 16. VHS VOLTAGE vs V_{DD} VOLTAGE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
November 12, 2015	FN9025.9	<ul style="list-style-type: none"> - Updated Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. - Updated POD L12.4X4A to latest revision changes are as follow: <ul style="list-style-type: none"> Updated to new POD format by removing table listing dimensions and moving dimensions onto drawing. Added Typical Recommended Land Pattern. Bottom View changed "3.2 REF" TO "2.5 REF" Typical Recommended Land Pattern changed "3.80" to "3.75" From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). - Updated POD M8.15 to latest revision changes are as follow: <ul style="list-style-type: none"> Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. Changed in Typical Recommended Land Pattern the following: <ul style="list-style-type: none"> 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 "1982" to "1994" - Updated POD M8.15C to most current version. Removed "u" symbol from drawing (overlaps the "a" on Side View).

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

© Copyright Intersil Americas LLC 2004-2015. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

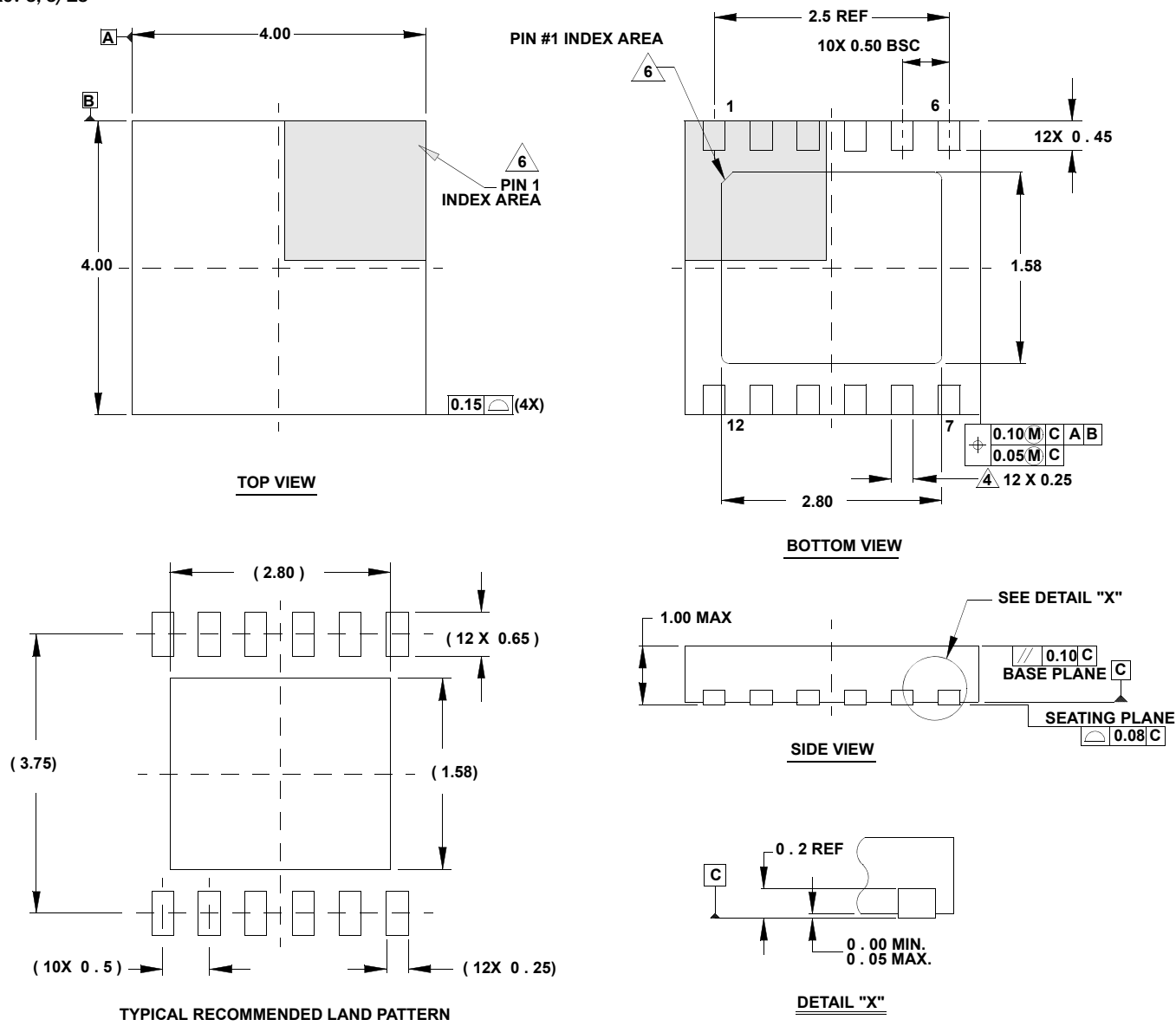
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

L12.4x4A

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

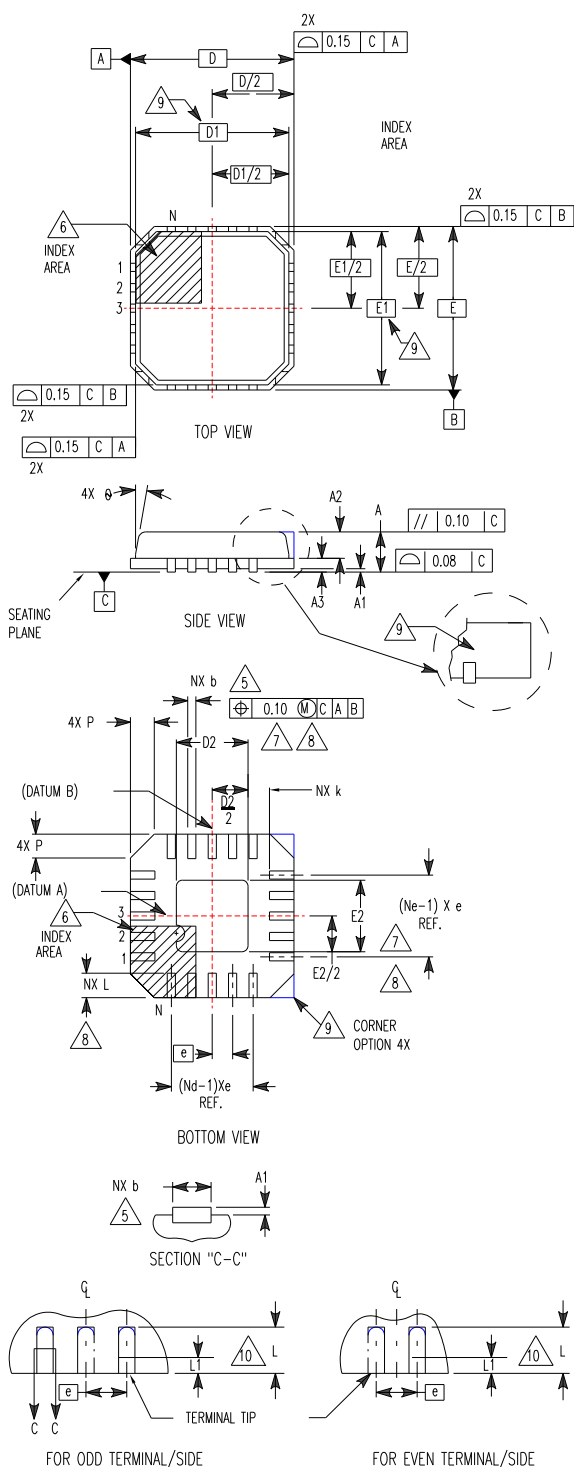
Rev 3, 3/15



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5

**16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220VHBB ISSUE C)**

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.28	0.33	0.40	5, 8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	2.55	2.70	2.85	7, 8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	2.55	2.70	2.85	7, 8
e	0.80 BSC			-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N	16			2
Nd	4			3
Ne	4	4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 2 10/02

NOTES:

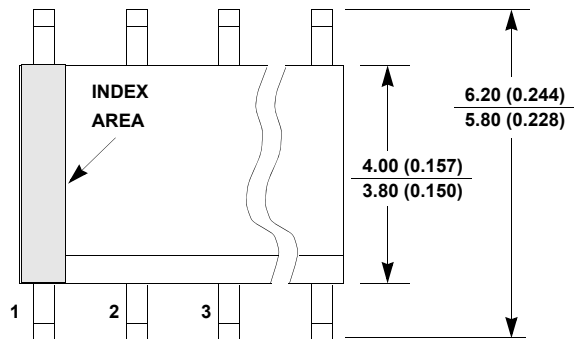
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Package Outline Drawing

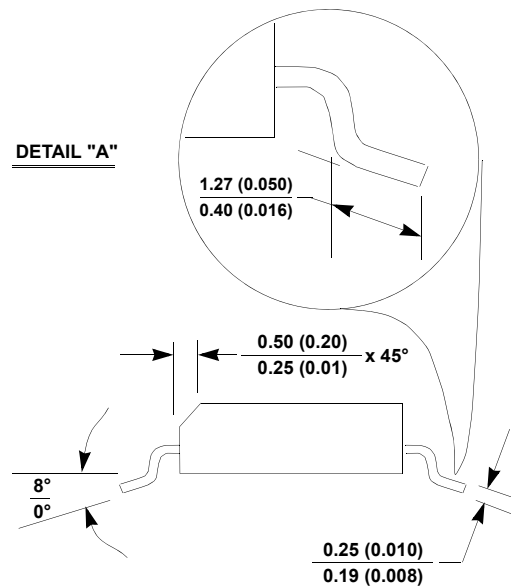
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

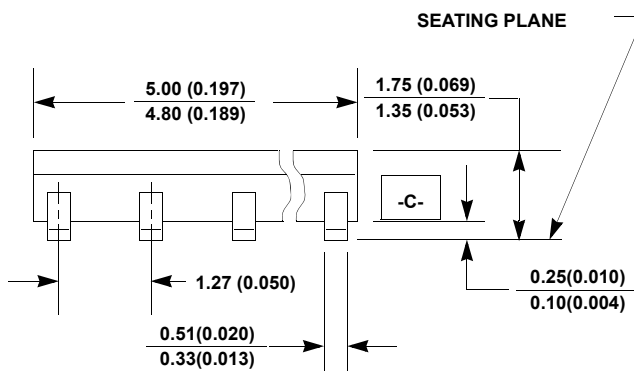
Rev 4, 1/12



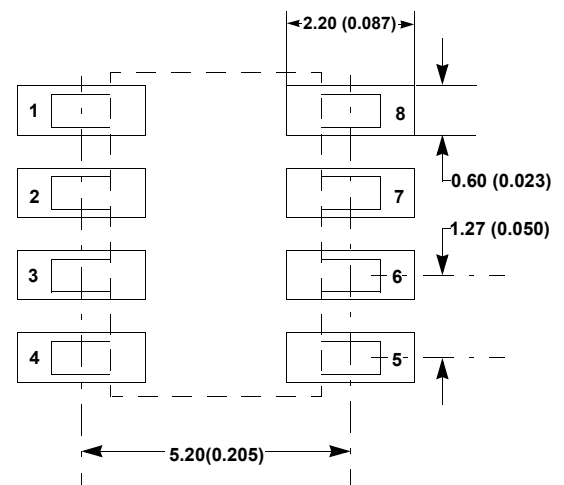
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

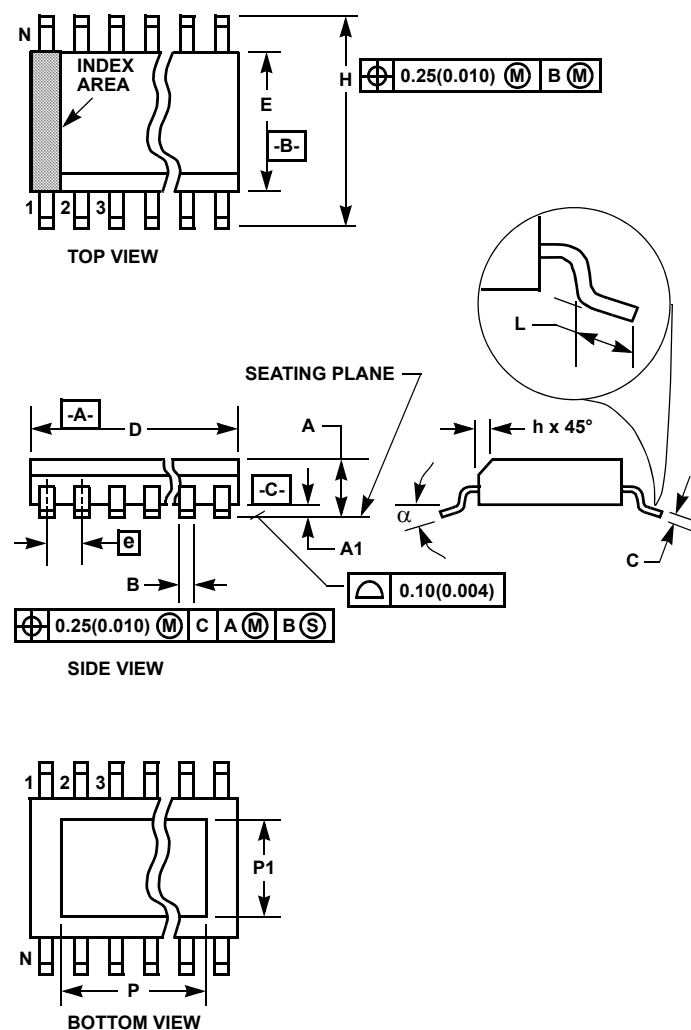


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Small Outline Exposed Pad Plastic Packages (EPSOIC)



M8.15C

8 LEAD NARROW BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.43	1.68	-
A1	0.001	0.005	0.03	0.13	-
B	0.0138	0.0192	0.35	0.49	9
C	0.0075	0.0098	0.19	0.25	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.811	3.99	4
e	0.050 BSC		1.27 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	8		8		7
α	0°	8°	0°	8°	-
P	-	0.126	-	3.200	11
P1	-	0.099	-	2.514	11

Rev. 1 6/05

NOTES:

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
- Dimensions "P" and "P1" are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.