



STP6NS25

N-CHANNEL 250V - 0.9Ω - 6A TO-220

MESH OVERLAY™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP6NS25	250 V	< 1.1 Ω	6 A

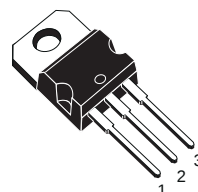
- TYPICAL R_{DS(on)} = 0.9 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performance. The new patented STrip layout coupled with the Company's proprietary edge termination structure, makes it suitable in converters for lighting applications.

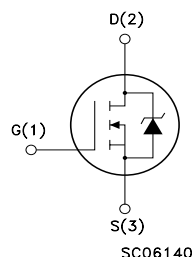
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-DC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	250	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	250	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	6	A
I _D	Drain Current (continuous) at T _C = 100°C	4	A
I _{DM} (•)	Drain Current (pulsed)	24	A
P _{TOT}	Total Dissipation at T _C = 25°C	70	W
	Derating Factor	0.56	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 6A, di/dt ≤ 300 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{jMAX}

STP6NS25

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.79	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	4	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	75	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	250			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 2 A		0.9	1.1	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 2A	1	3.5		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		355		pF
C _{oss}	Output Capacitance			64		pF
C _{rss}	Reverse Transfer Capacitance			30		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 125\text{ V}$, $I_D = 3\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		12		ns
t_r	Rise Time			18		ns
Q_g	Total Gate Charge	$V_{DD} = 200\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 10\text{ V}$		19	27	nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			7.5		nC

SWITCHING OFF

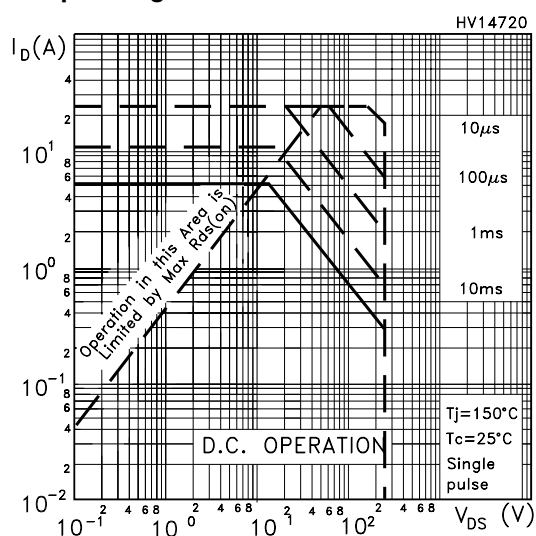
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 125\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		70		ns
t_f	Fall Time			10		ns
$t_{r(off)}$	Off-voltage Rise Time	$V_{clamp} = 200\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		13		ns
t_f	Fall Time			10		ns
t_c	Cross-over Time			21		ns

SOURCE DRAIN DIODE

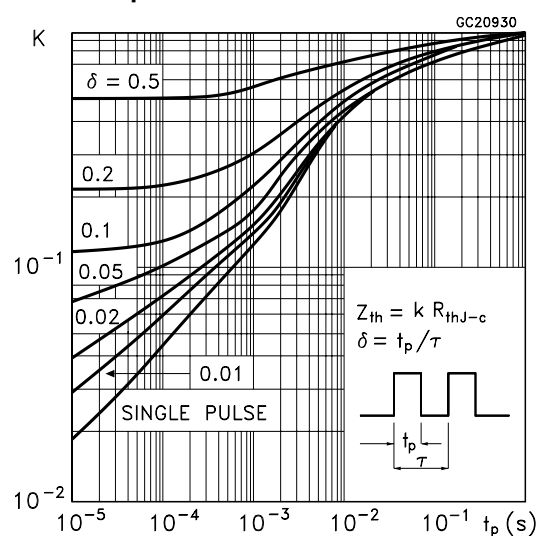
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				6	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				24	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$, $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		124		ns
Q_{rr}	Reverse Recovery Charge			0.5		μC
I_{RRM}	Reverse Recovery Current			7		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

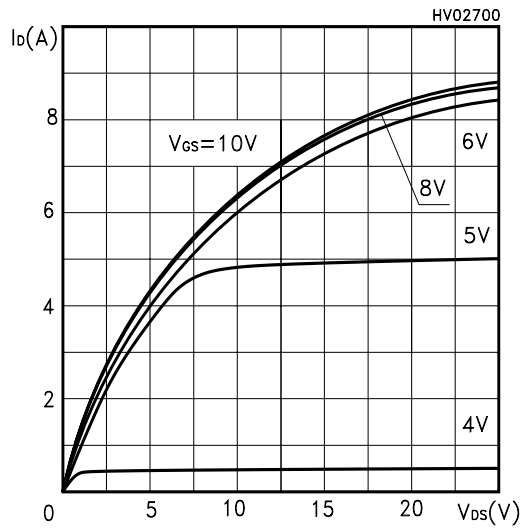
Safe Operating Area



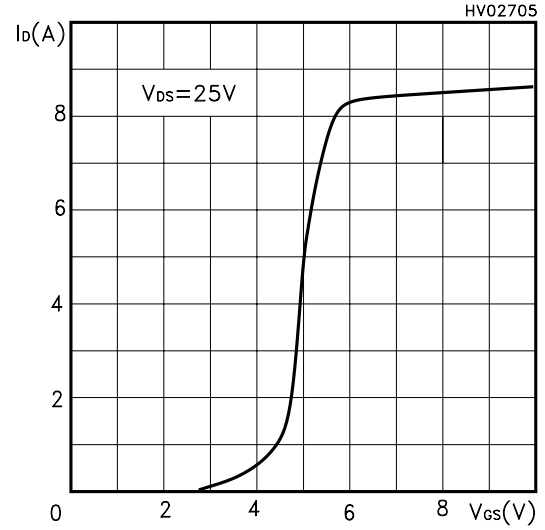
Thermal Impedance



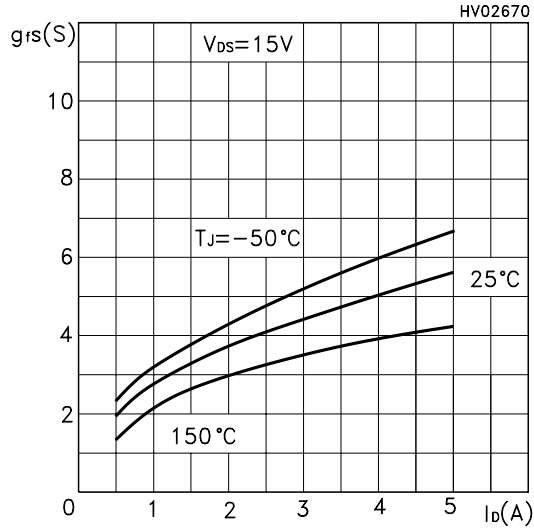
Output Characteristics



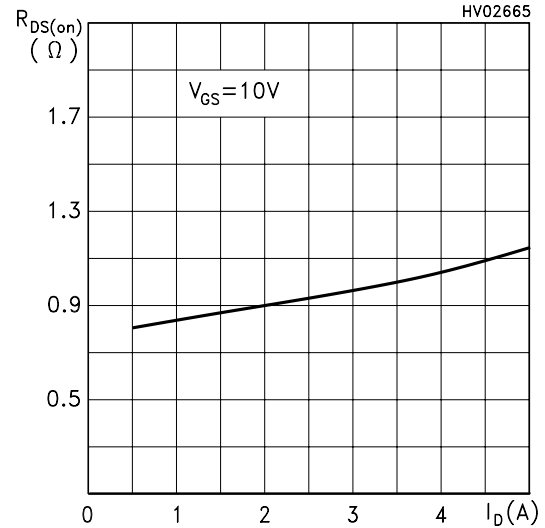
Transfer Characteristics



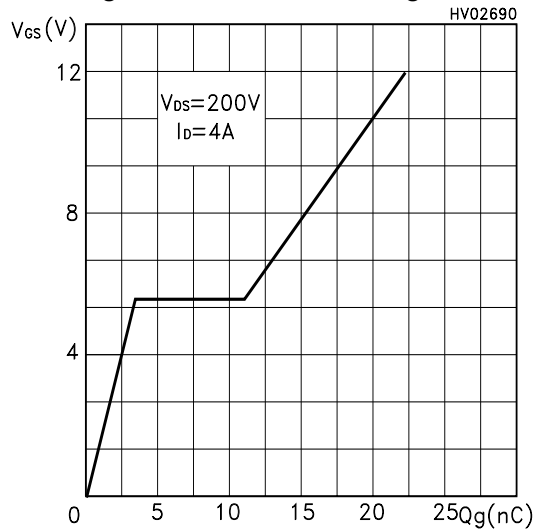
Transconductance



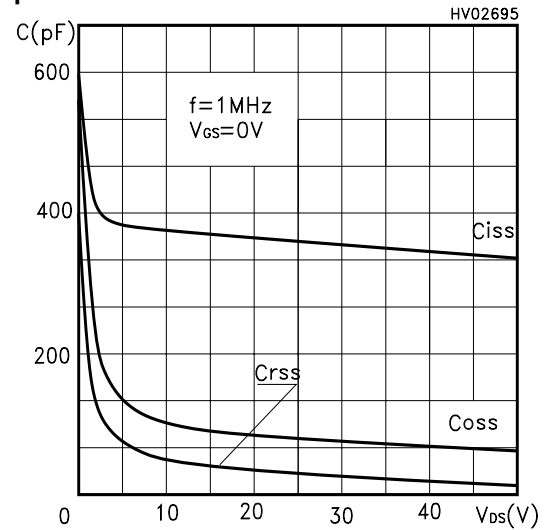
Static Drain-source On Resistance



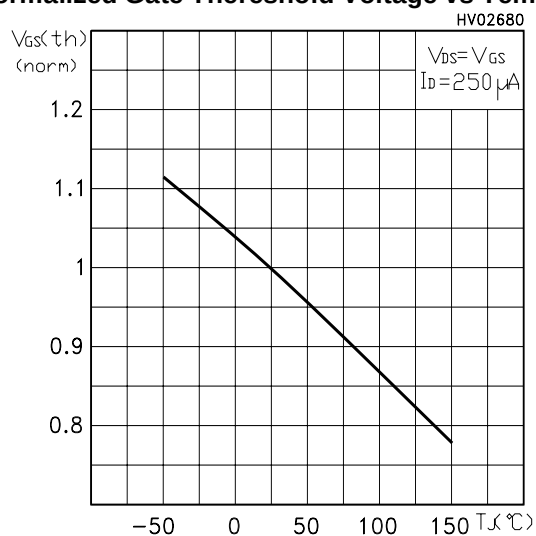
Gate Charge vs Gate-source Voltage



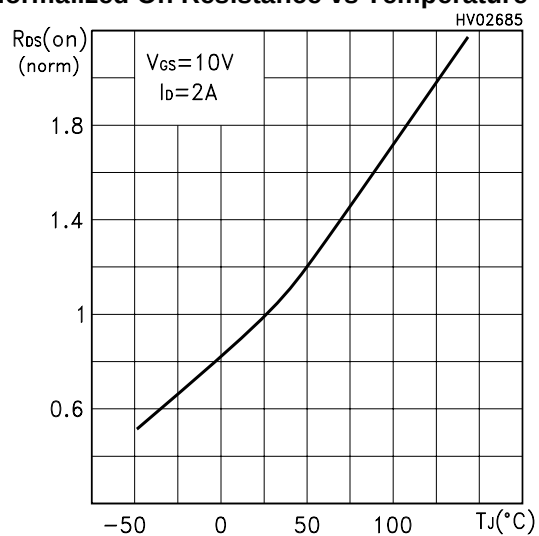
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

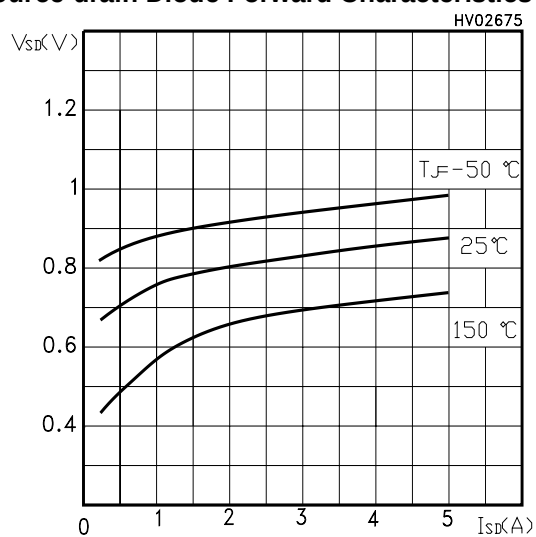


Fig. 1: Unclamped Inductive Load Test Circuit

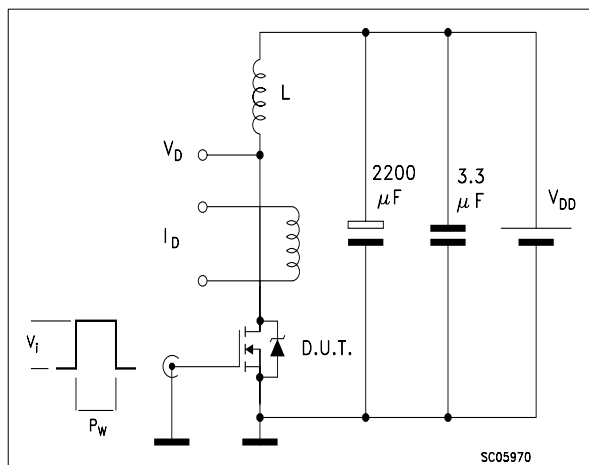


Fig. 2: Unclamped Inductive Waveform

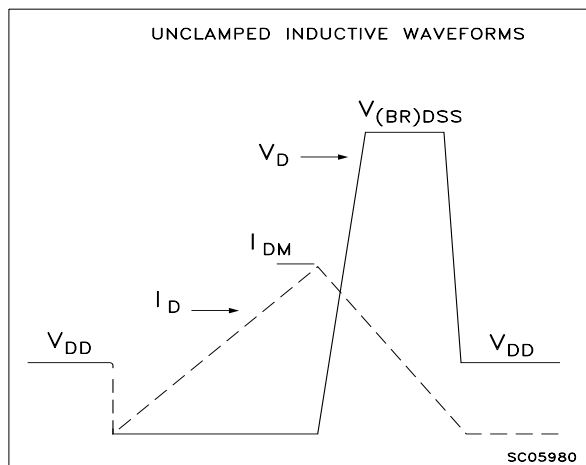


Fig. 3: Switching Times Test Circuit For Resistive Load

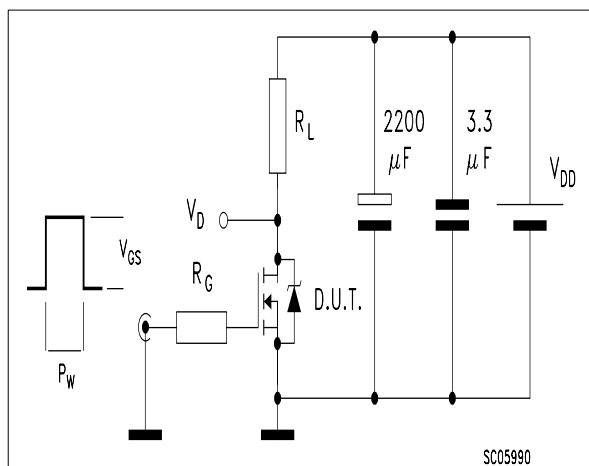


Fig. 4: Gate Charge test Circuit

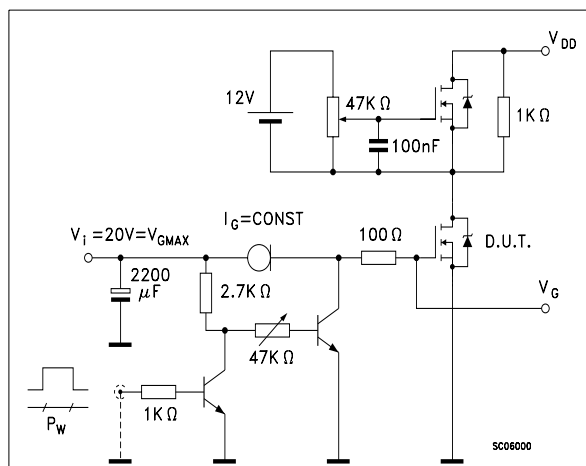
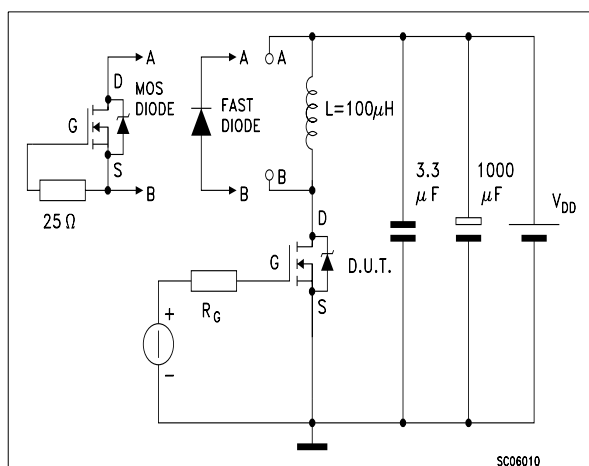
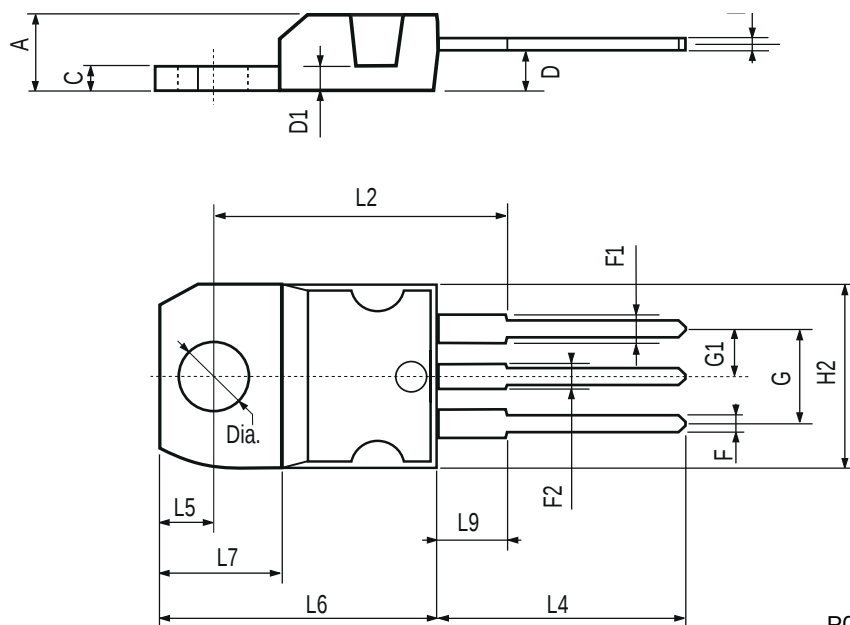


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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