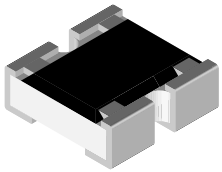
Thick Film Chip Attenuator, Surface Mount, Unbalanced π Type



FEATURES

- Single component reduces board space and component counts - replaces 3 or more components
- Tolerance matching and temperature tracking superior to individual components
- Maximum power dissipation: 0.075 W for CZA06S; 0.040 W for CZA04S
- Consult factory for extended values, non-standard tolerances, impedance matching and other attenuation values
- Frequency range: DC to 3 GHz
- Surface mount chip attenuator in a resistor array package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available

e3 RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

STANDARD ELECTRICAL SPECIFICATIONS

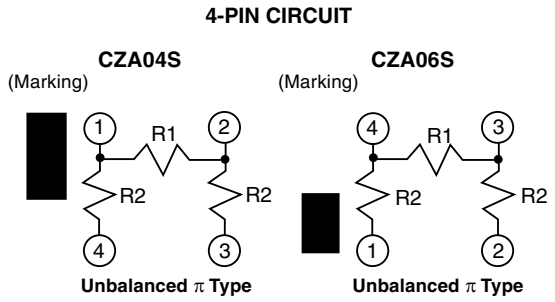
GLOBAL MODEL	POWER RATING $P_{70\,°C}$ W	IMPEDANCE Ω	ATTENUATION RANGE AND TOLERANCE	
			± 0.3 dB (L)	± 0.5 dB (H)
CZA04S	0.040	50	0 dB, 1 dB to 5 dB	6 dB to 20 dB
CZA06S	0.075	50/75/100/300/600	0 dB, 1 dB to 5 dB	6 dB to 20 dB

Note

- Power rating depends on the maximum temperature at the solder point, the component placement density and the substrate material

IMPEDANCE	50 Ω	75 Ω	100 Ω	300 Ω	600 Ω
Attenuation in dB (1)	1	1	1	1	1
	1.5	1.5	1.5	1.5	1.5
	2	2	2	2	2
	3	3	3	3	3
	4	4	4	4	4
	5	5	5	5	5
	6	6	6	6	6
	10	10	10	10	10
	11	11	11	11	11
	12	12	12	12	12
	13	13	13	13	13
	14	14	14	14	14
	15	15	15	15	15
	16	16	16	16	16
	17	17	17	17	17
	18	18	18	18	18
	19	19	19	19	19
	20	20	20	20	20

CIRCUIT SCHEMATIC



Note

(1) Consult factory for other attenuations

TECHNICAL SPECIFICATIONS

PARAMETER	UNIT	CZA04S	CZA06S
Rated dissipation at 70 °C	W	0.040	0.075
VSWR		1.2 max.	1.2 max.
Category temperature range	°C	-55 to +125	-55 to +150
Frequency range		DC to 3 GHz	DC to 3 GHz

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: CZA06S04015050LRT (preferred part numbering format)

C	Z	A	0	6	S	0	4	0	1	5	0	5	0	L	R	T	

MODEL	PIN COUNT	ATTENUATION	IMPEDANCE	TOLERANCE	PACKAGING	SPECIAL
CZA04S **CZA06S**	**04** = 4 pin	**010** = 1.0 dB **015** = 1.5 dB **020** = 2.0 dB **150** = 15.0 dB **000** = 0 dB or 0 Ω jumper	**050** = 50 Ω **075** = 75 Ω **100** = 100 Ω **000** = 0 Ω jumper	**H** = ± 0.5 dB **L** = ± 0.3 dB **Z** = 0 Ω Jumper	**EA** = lead (Pb)-free, T/R (all) **TD** = tin lead, T/R (04 only) **RT** = tin lead, T/R (06 only)	(Dash number) Up to 1 digit Blank = standard

Historical Part Number Example: CZA06S04015050LRT (will continue to be accepted)

CZA	06S	04	015	050	L	RT
MODEL	CASE SIZE	PIN COUNT	ATTENUATION	IMPEDANCE	TOLERANCE	PACKAGING

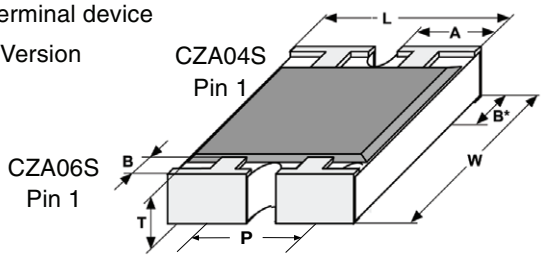
Note

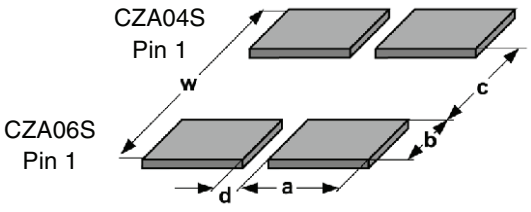
- For additional information on packaging, refer to the Surface Mount Network Packaging document (www.vishay.com/doc?31540)

DIMENSIONS

4-Terminal device

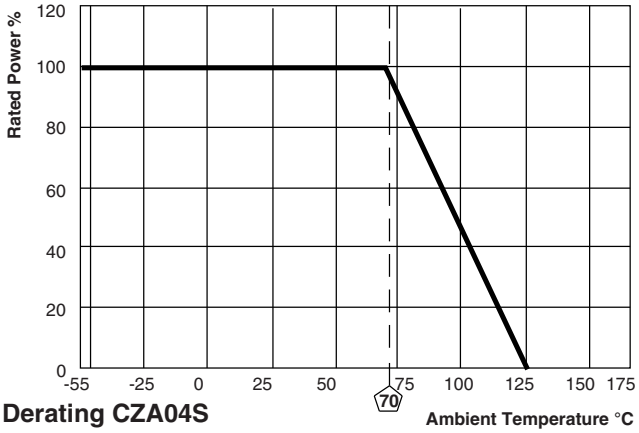
S - Version



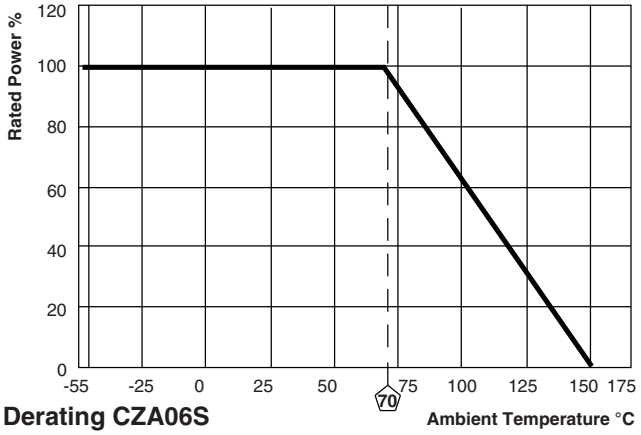


GLOBAL MODEL	DIMENSIONS in inches (millimeters)						
	L	W	T	A	P	B	B*
CZA04S	0.039 ± 0.004 (1.00 ± 0.10)	0.039 ± 0.006 (1.00 ± 0.15)	0.014 ± 0.004 (0.36 ± 0.10)	0.013 ± 0.006 (0.33 ± 0.15)	0.026 (0.65)	0.006 ± 0.004 (0.15 ± 0.10)	0.010 ± 0.004 (0.25 ± 0.10)
CZA06S	0.063 ± 0.006 (1.60 ± 0.15)	0.059 ± 0.006 (1.50 ± 0.15)	0.020 ± 0.004 (0.51 ± 0.10)	0.024 ± 0.006 (0.61 ± 0.15)	0.031 (0.80)	0.012 ± 0.006 (0.30 ± 0.15)	0.012 ± 0.006 (0.30 ± 0.15)

GLOBAL MODEL	SOLDER PAD DIMENSIONS in inches (millimeters)				
	c	w	d	a	b
CZA04S	0.018 (0.45)	0.083 (2.10)	0.008 (0.20)	0.018 (0.45)	0.032 (0.82)
CZA06S	0.031 (0.80)	0.122 (3.10)	0.014 (0.36)	0.025 (0.63)	0.045 (1.15)



Derating CZA04S



Derating CZA06S

PERFORMANCE			
TEST	CONDITIONS OF TEST	TEST RESULTS (TYPICAL TEST LOTS)	
		0.5 dB to 5 dB	6 dB to 20 dB
Endurance test at 70 °C per EIA 575-3.14	1000 h at 70 °C, 1.5 h “ON”, 0.5 h “OFF”	± 0.2 dB	± 0.3 dB
Overload per EIA 575-3.6	Short time overload	± 0.2 dB	± 0.3 dB
Thermal shock	Per EIA 575-3.5	± 0.2 dB	± 0.3 dB
Moisture resistance	Per EIA 575-3.10	± 0.2 dB	± 0.3 dB
Resistance to soldering heat	10 s at 260 °C solder bath temperature EIA 575 3.8	± 0.2 dB	± 0.3 dB
High temperature exposure	Per EIA 575-3.7	± 0.2 dB	± 0.3 dB
Low temperature operations	Per EIA-575-3.6	± 0.2 dB	± 0.3 dB
Solderability and leaching	EIA 575-3.12	95 % coverage	

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