

HD74HCT540, HD74HCT541

Octal Buffers/Line Drivers (with 3-state outputs)

REJ03D0668–0200
(Previous ADE-205-558)
Rev.2.00
Mar 30, 2006

Description

The HD74HCT540 is an inverting buffer and the HD74HCT541 is a non-inverting buffer. The 3-state control gate operates as a two-input NOR such that if either $\overline{G_1}$ or $\overline{G_2}$ are high, all eight outputs are in the high-impedance state.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (A to Y) = 12 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT540P HD74HCT541P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74HCT540FPEL HD74HCT541FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HCT541RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HCT540TELL HD74HCT541TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs			Output Y	
$\overline{G_1}$	$\overline{G_2}$	A	HD74HCT540	HD74HCT541
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

H : high level

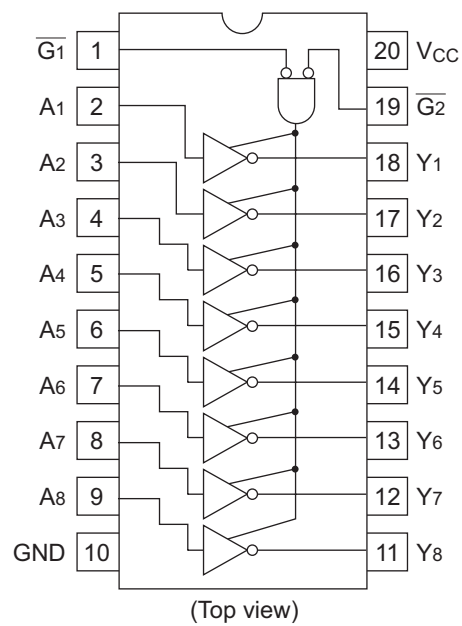
L : low level

X : irrelevant

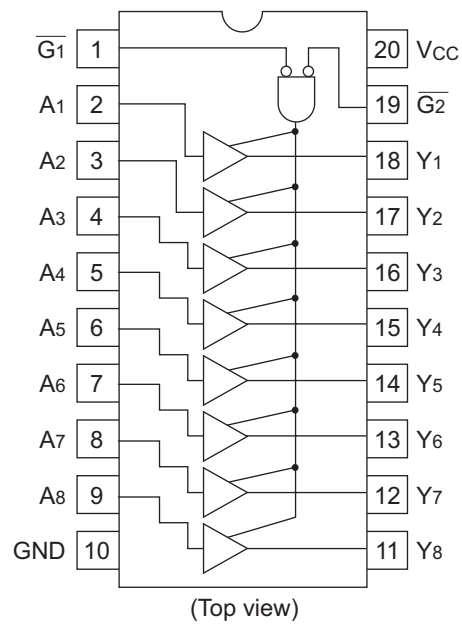
Z : off (high-impedance) state of a 3-state output

Pin Arrangement

HD74HCT540



HD74HCT541



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 500	ns	$V_{CC} = 4.5$ V

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

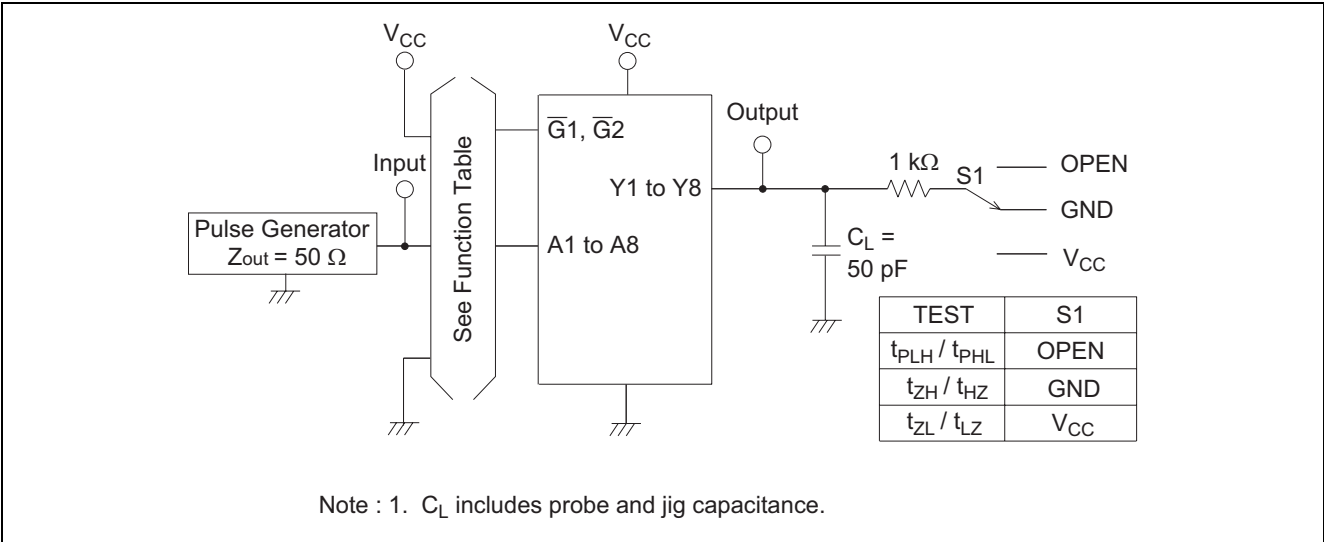
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V_{IL}	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V_{OH}	4.5	4.4	—	—	4.4	—	V	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$
		4.5	4.18	—	—	4.13	—	V		$I_{OH} = -6 \text{ mA}$
	V_{OL}	4.5	—	—	0.1	—	0.1	V	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$
		4.5	—	—	0.26	—	0.33	V		$I_{OL} = 6 \text{ mA}$
Off-state output current	I_{OZ}	5.5	—	—	± 0.5	—	± 5.0	μA	$V_{in} = V_{IH} \text{ or } V_{IL}, V_{out} = V_{CC} \text{ or } \text{GND}$	
Input current	I_{in}	5.5	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC} \text{ or } \text{GND}$	
Quiescent current	I_{CC}	5.5	—	—	4.0	—	40	μA	$V_{in} = V_{CC} \text{ or } \text{GND}, I_{out} = 0 \mu\text{A}$	

Switching Characteristics

($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t_{PLH}	4.5	—	11	20	—	25	ns	HD74HCT540 only
	t_{PHL}	4.5	—	12	20	—	25		
	t_{PLH}	4.5	—	10	23	—	29	ns	HD74HCT541 only
	t_{PHL}	4.5	—	13	23	—	29		
Output enable time	t_{ZL}	4.5	—	16	30	—	38	ns	
	t_{ZH}	4.5	—	20	30	—	38		
Output disable time	t_{LZ}	4.5	—	15	30	—	38	ns	
	t_{HZ}	4.5	—	15	30	—	38		
Output rise/fall time	t_{TLH}	4.5	—	4	12	—	15	ns	
	t_{THL}	4.5	—	4	12	—	15		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

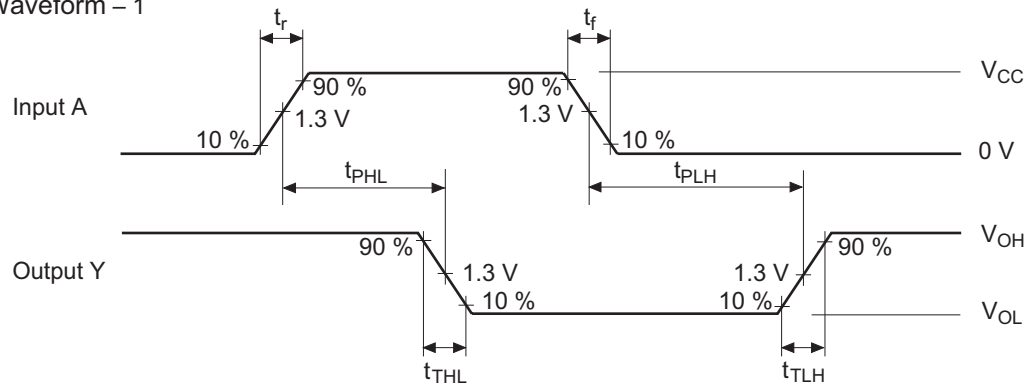
Test Circuit



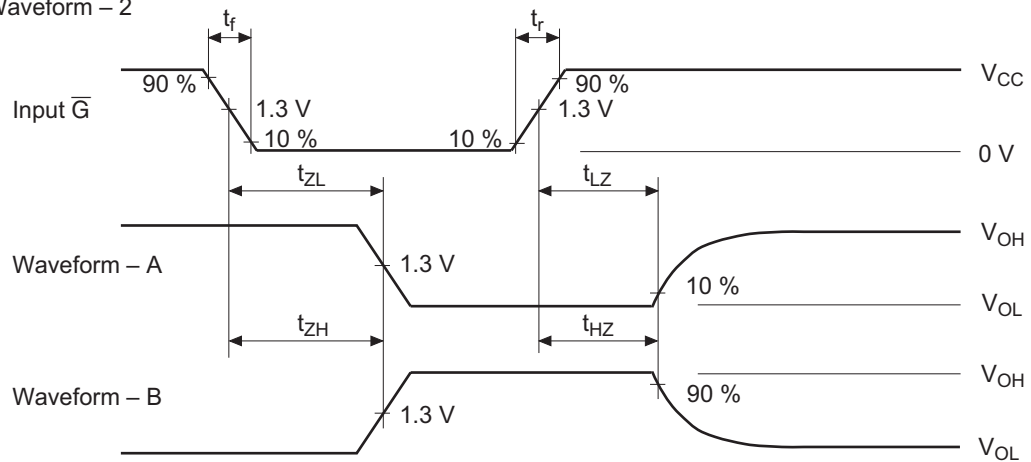
Waveforms

HD74HCT540

• Waveform – 1



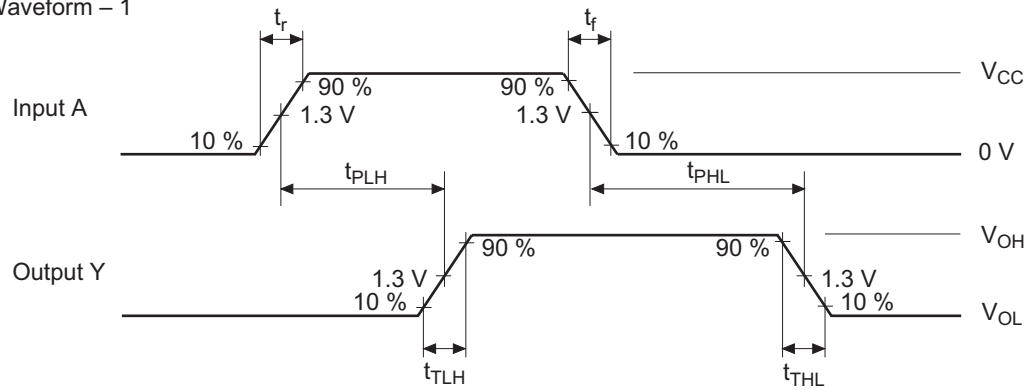
• Waveform – 2



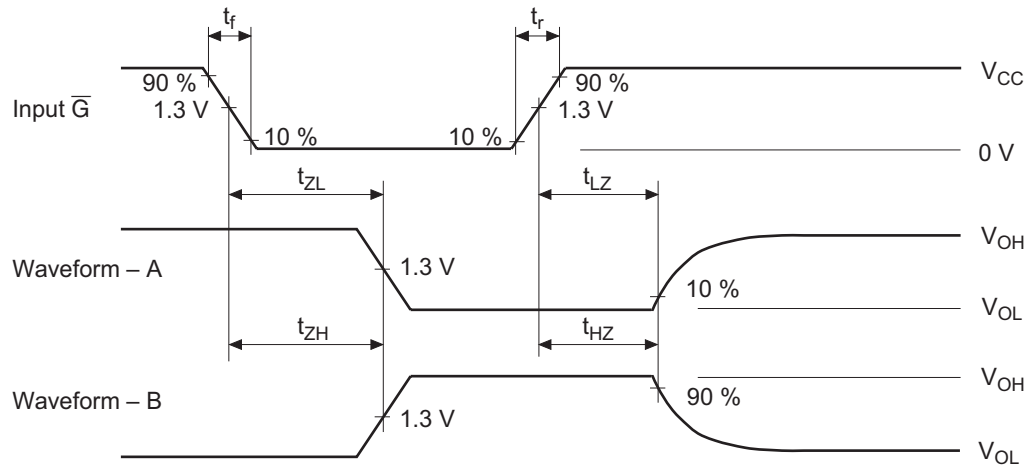
- Notes :
1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

HD74HCT541

• Waveform – 1

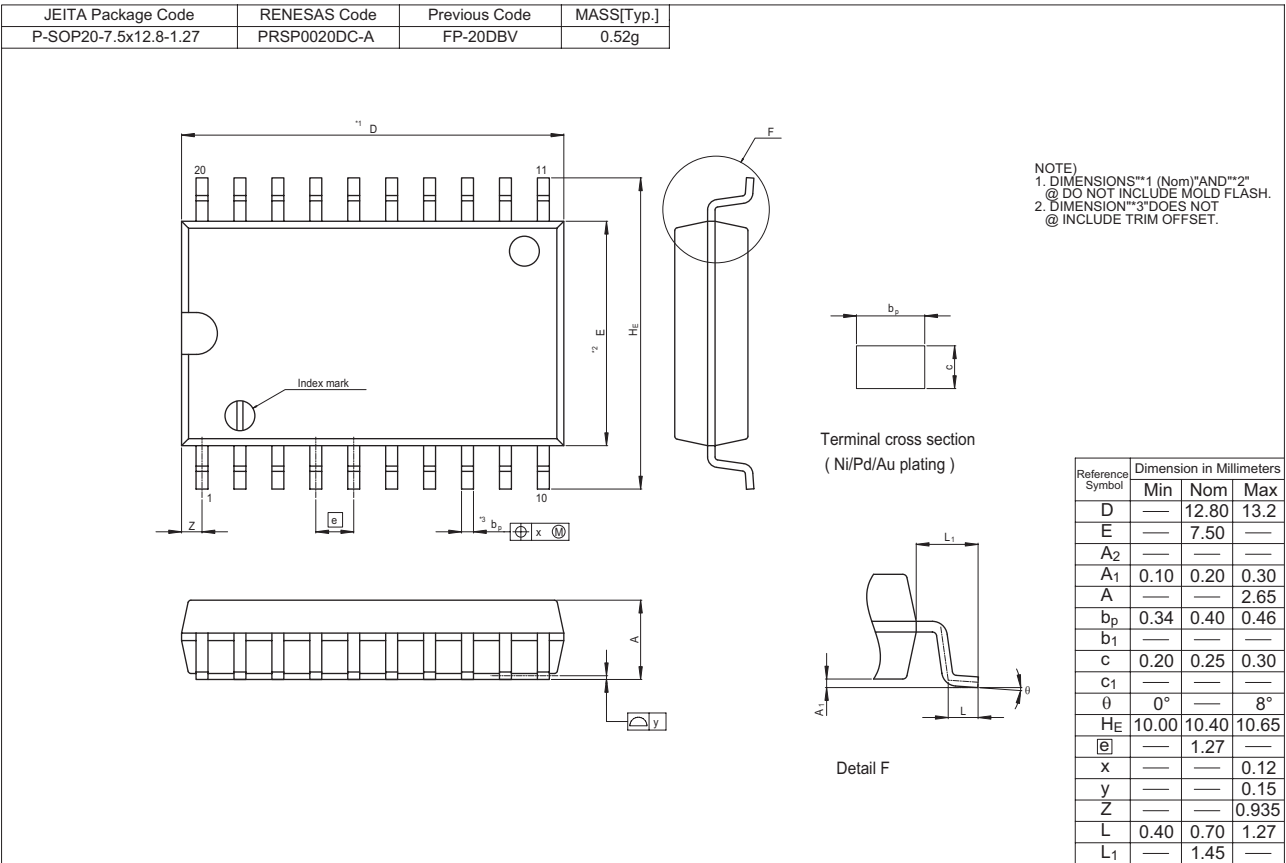
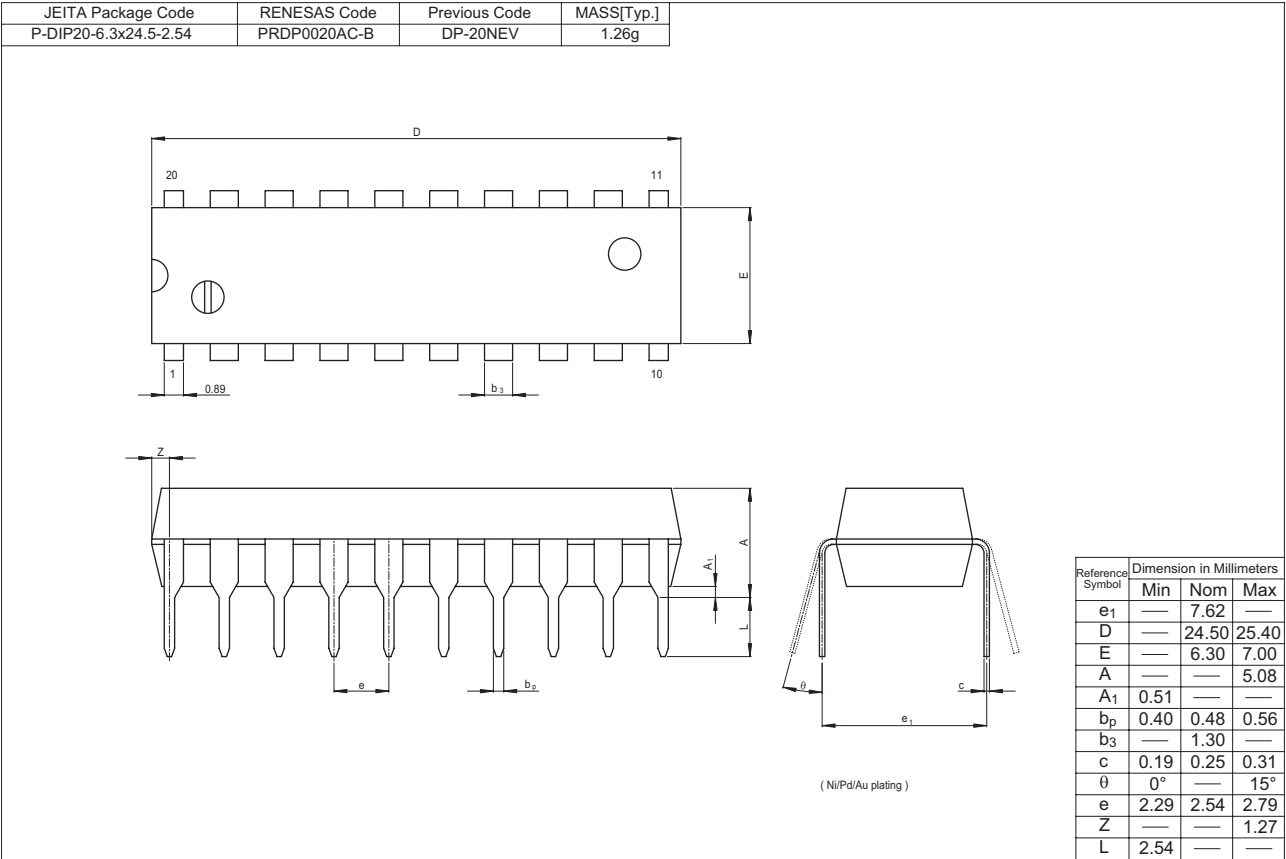


• Waveform – 2



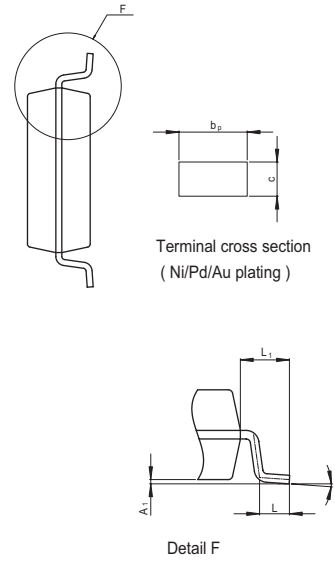
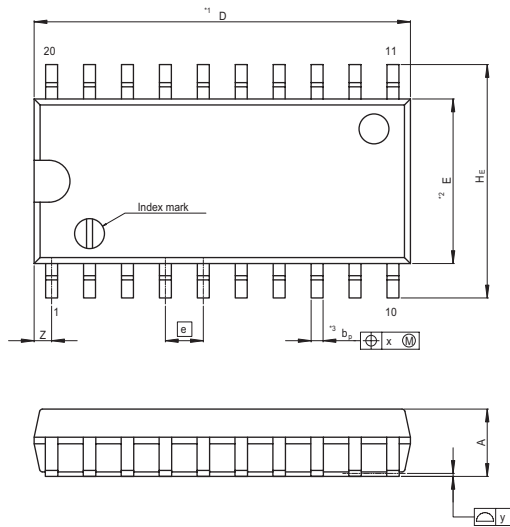
- Notes :
1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



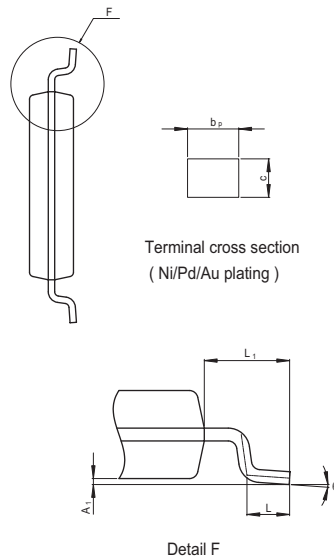
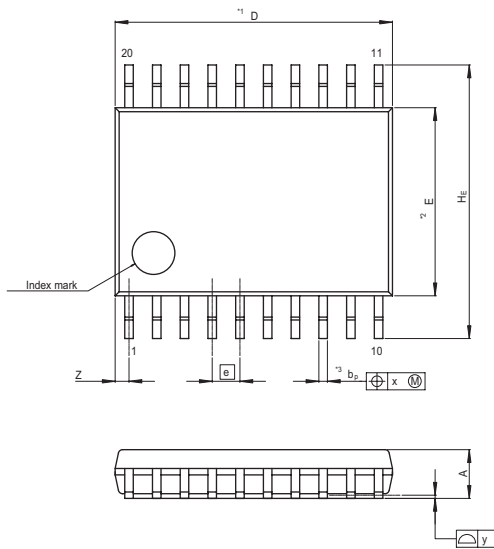
HD74HCT540, HD74HCT541

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g



Reference Symbol	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
⓪	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP20-4.4x6.5-0.65	PTSP0020JB-A	TTP-20DAV	0.07g



Reference Symbol	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
H _E	6.20	6.40	6.60
⓪	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L ₁	—	1.0	—

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