

## Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = 25^\circ\text{C}$
20V	$0.99\Omega @ V_{GS} = 4.5V$	760mA
	$1.2\Omega @ V_{GS} = 2.5V$	700mA
	$2.4\Omega @ V_{GS} = 1.8V$	500mA
	$3.0\Omega @ V_{GS} = 1.5V$	350mA

## Description and Applications


This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

## Features and Benefits

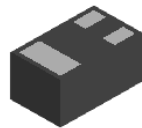
- Low On-Resistance
- Very low Gate Threshold Voltage, 1.0V max
- Low Input Capacitance
- Fast Switching Speed
- Ultra-Small Surface Mount Package 1mm x 0.6mm
- Low Package Profile, 0.5mm Maximum Package height
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

## Mechanical Data

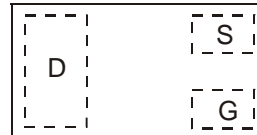
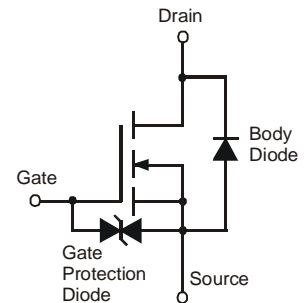
- Case: X1-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.001 grams (approximate)



X1-DFN1006-3



Bottom View


 Top View  
 Package Pin Configuration


Equivalent Circuit

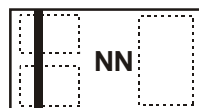
## Ordering Information (Note 4)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMN21D2UFB-7B	NN	7	8	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com>.

## Marking Information

DMN21D2UFB-7B


 Top View  
 Bar Denotes Gate and Source Side

NN = Product Type Marking Code

**Maximum Ratings** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V <sub>DSS</sub>	20	V
Gate-Source Voltage			V <sub>GSS</sub>	±12	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	760 610	mA
	t < 5s	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	850 700	mA
Maximum Continuous Body Diode Forward Current (Note 6)			I <sub>S</sub>	0.8	A
Pulsed Drain Current (Note 7)			I <sub>DM</sub>	1.0	A

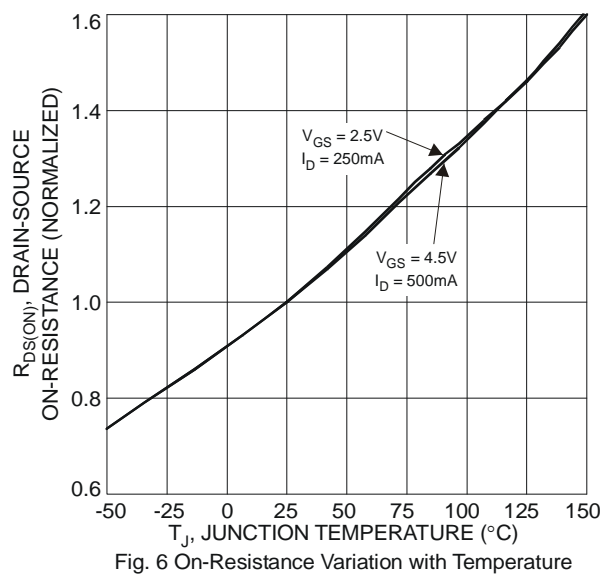
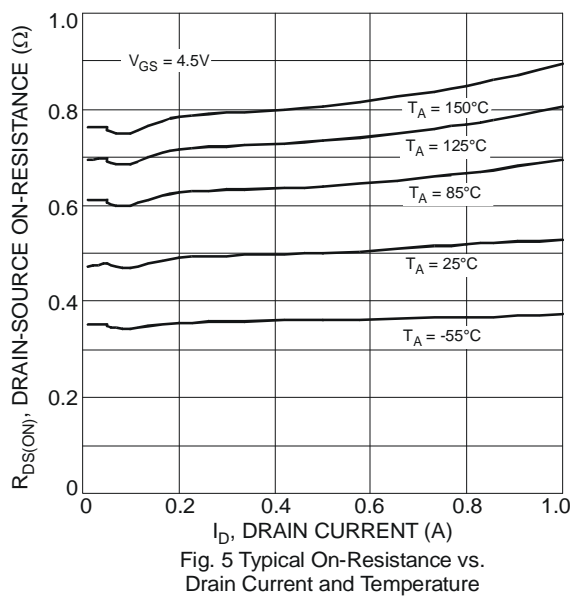
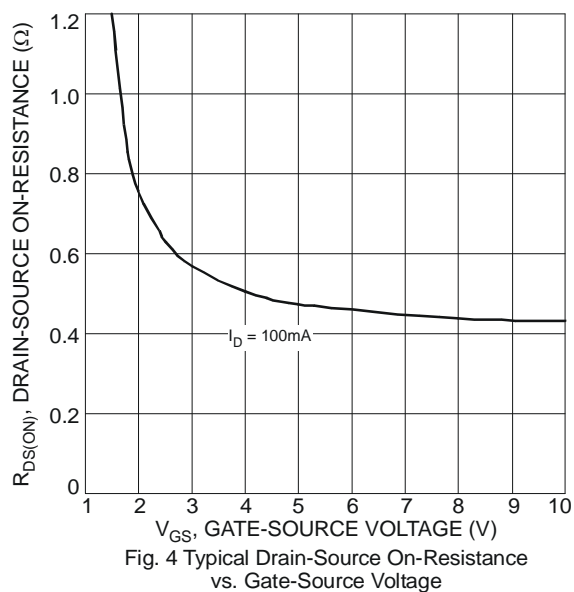
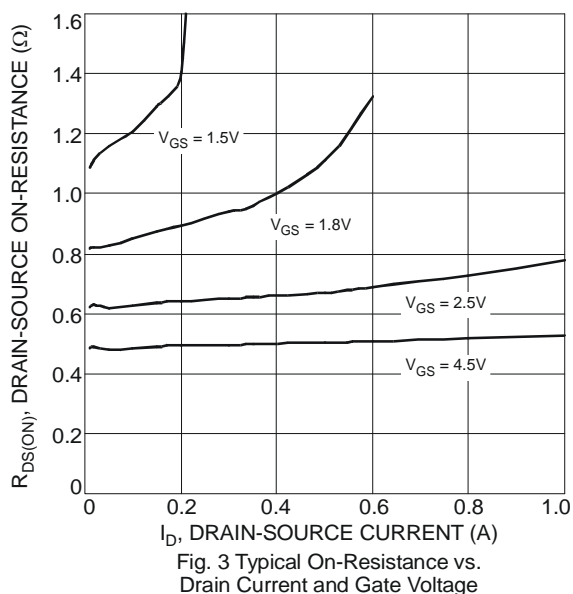
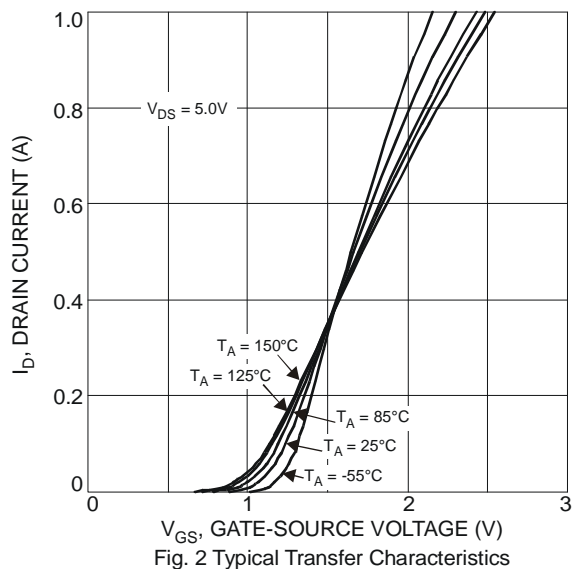
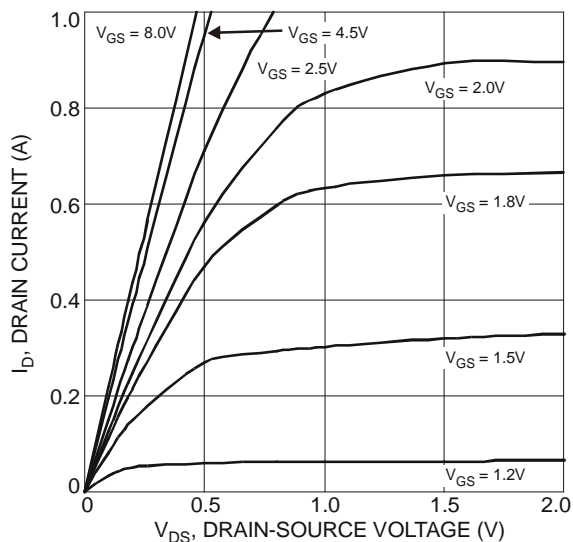
**Thermal Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 4)	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.38	W
	T <sub>A</sub> = 70°C		0.25	
Thermal Resistance, Junction to Ambient (Note 4)	Steady State	R <sub>θJA</sub>	325	°C/W
	t < 5s		244	
Total Power Dissipation (Note 5)	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.9	W
	T <sub>A</sub> = 70°C		0.57	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R <sub>θJA</sub>	141	°C/W
	t < 5s		106	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

**Electrical Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current @ T <sub>c</sub> = 25°C	I <sub>DSS</sub>	-	-	100	nA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±1	μA	V <sub>GS</sub> = ±10V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.4	-	1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	-	0.6	0.99	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 100mA
		-	0.7	1.2		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 50mA
		-	0.9	2.4		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 20mA
		-	1.2	3.0		V <sub>GS</sub> = 1.5V, I <sub>D</sub> = 10mA
Forward Transfer Admittance	Y <sub>fs</sub>	180	-	-	mS	V <sub>DS</sub> = 10V, I <sub>D</sub> = 400mA
Diode Forward Voltage	V <sub>SD</sub>	-	0.6	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 150mA
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	-	27.6	-	pF	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	-	4.0	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	2.8	-	pF	
Total Gate Charge V <sub>GS</sub> = 4.5V	Q <sub>g</sub>	-	0.41	-	nC	V <sub>DS</sub> = 10V, I <sub>D</sub> = 250mA
Total Gate Charge V <sub>GS</sub> = 10V	Q <sub>g</sub>	-	0.93	-	nC	
Gate-Source Charge	Q <sub>gs</sub>	-	0.06	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	0.06	-	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	-	3.5	-	ns	V <sub>DD</sub> = 10V, V <sub>GS</sub> = 4.5V, R <sub>L</sub> = 47Ω, R <sub>G</sub> = 10Ω, I <sub>D</sub> = 200mA
Turn-On Rise Time	t <sub>r</sub>	-	4.2	-	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	-	19.6	-	ns	
Turn-Off Fall Time	t <sub>f</sub>	-	9.8	-	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
  - Device mounted on minimum recommended pad layout test board, 10μs pulse duty cycle = 1%.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.



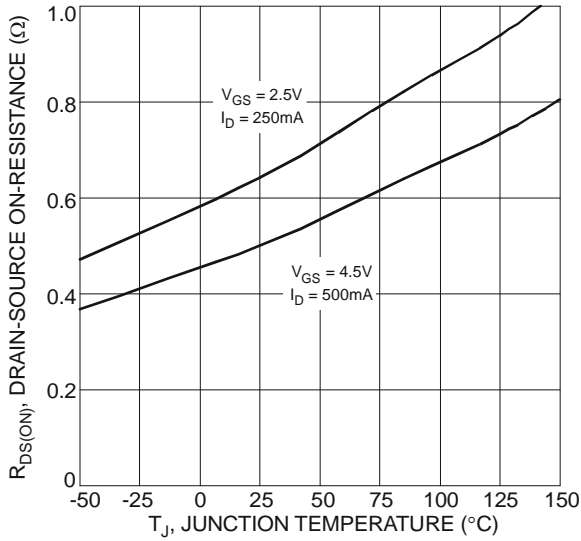


Fig. 7 On-Resistance Variation with Temperature

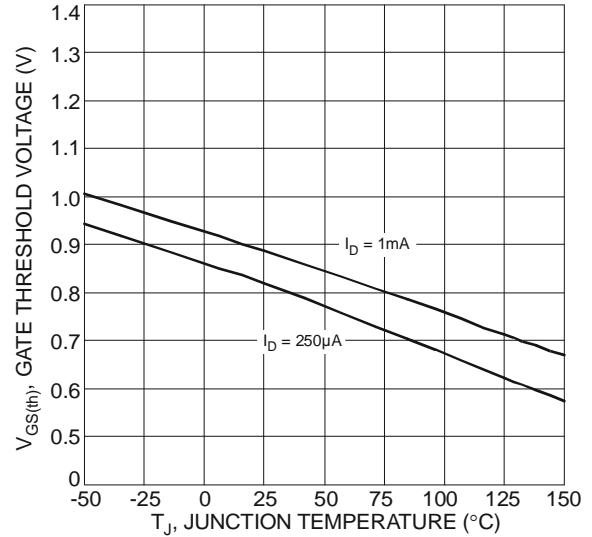


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

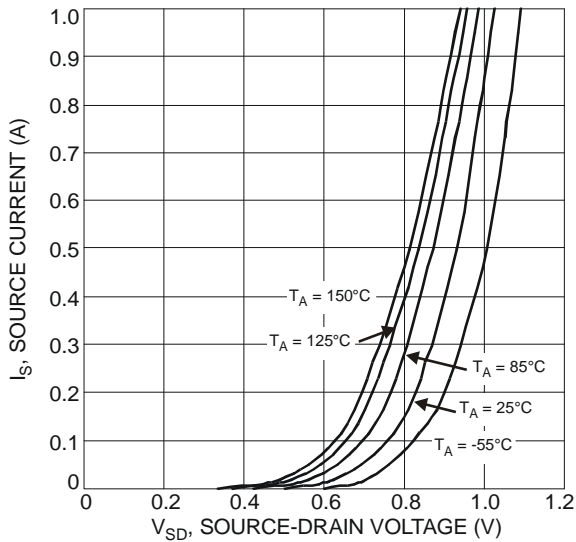


Fig. 9 Diode Forward Voltage vs. Current

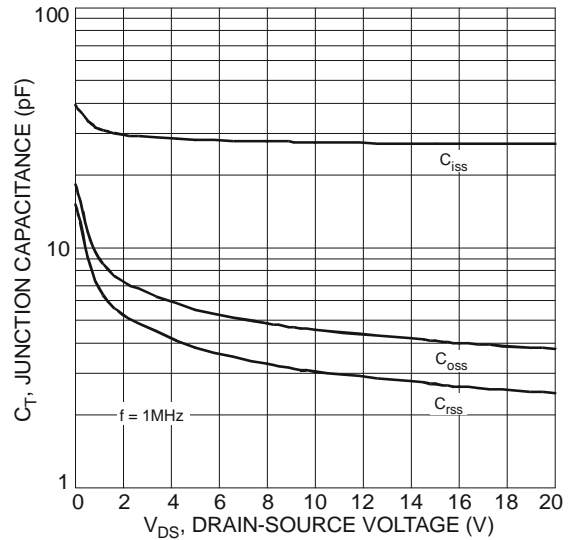


Fig. 10 Typical Junction Capacitance

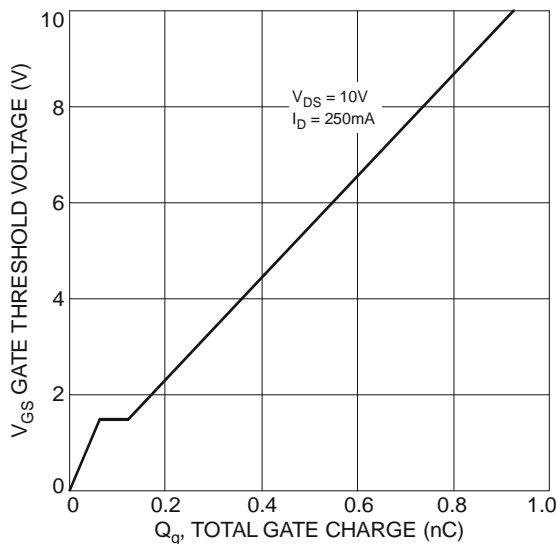


Fig. 11 Gate Charge

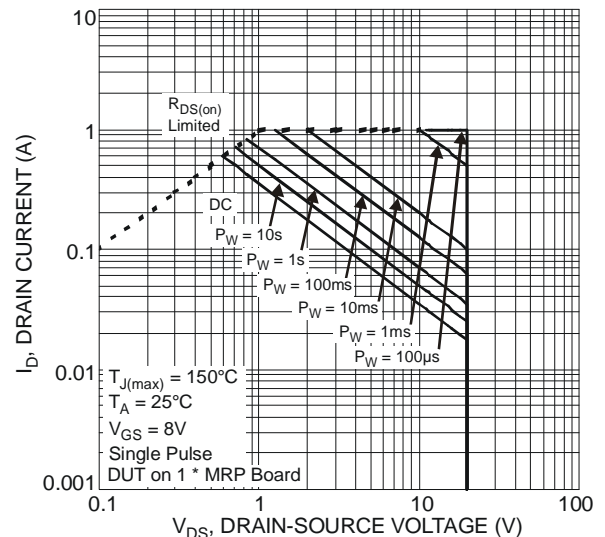
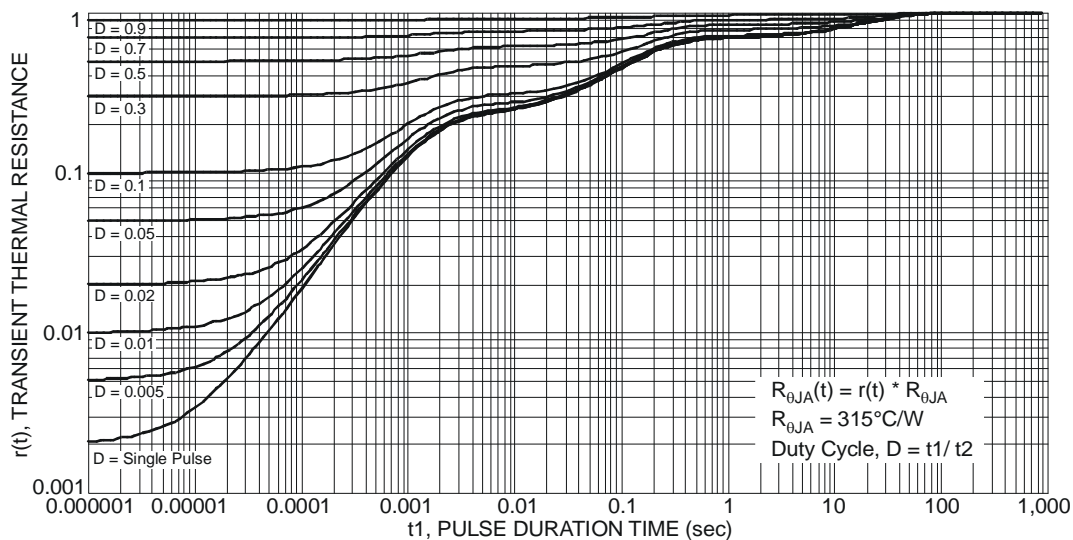
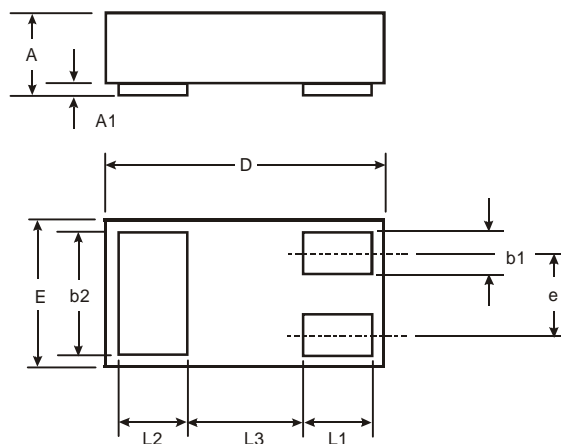


Fig. 12 SOA, Safe Operation Area

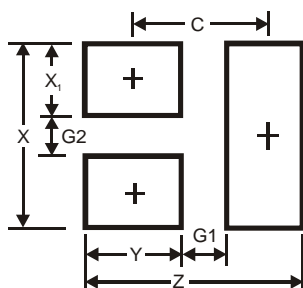


## Package Outline Dimensions



X1-DFN1006-3			
Dim	Min	Max	Typ
A	0.47	0.53	0.50
A1	0	0.05	0.03
b1	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	—	—	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	—	—	0.40
All Dimensions in mm			

## Suggested Pad Layout



Dimensions	Value (in mm)
Z	1.1
G1	0.3
G2	0.2
X	0.7
X1	0.25
Y	0.4
C	0.7

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