

SN54F109, SN74F109
DUAL J- \bar{K} POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

SDF047A – MARCH 1987 – REVISED OCTOBER 1993

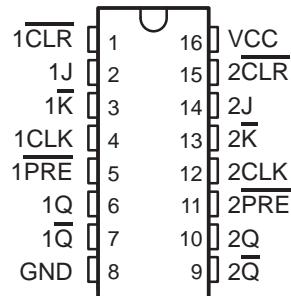
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

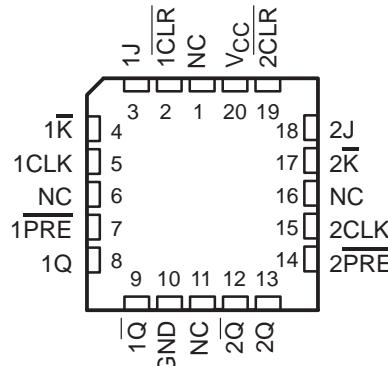
These devices contain two independent J- \bar{K} positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and \bar{K} input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and \bar{K} inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding \bar{K} and trying J high. They also can perform as D-type flip-flops if J and \bar{K} are tied together.

The SN54F109 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F109 is characterized for operation from 0°C to 70°C .

SN54F109 . . . J PACKAGE
SN74F109 . . . D OR N PACKAGE
(TOP VIEW)



SN54F109 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

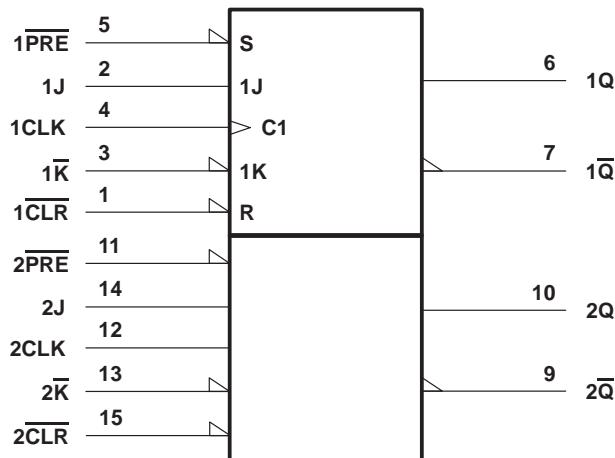
INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q ₀	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	\bar{Q}_0

[†] The output levels are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

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SDFS047A – MARCH 1987 – REVISED OCTOBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F109			SN74F109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2		V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-1			-1	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

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SDFS047A – MARCH 1987 – REVISED OCTOBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F109			SN74F109			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V	
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		V	
	$V_{CC} = 4.75 \text{ V}$, $I_{OH} = -1 \text{ mA}$				2.7				
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 20 \text{ mA}$		0.3	0.5		0.3	0.5	V	
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA	
I_{IL}	J, \bar{K}, CLK PRE or CLR	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.5 \text{ V}$		-0.6			-0.6	mA	
				-1.8			-1.8		
I_{OS}^{\ddagger}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0$		-60	-150	-60	-150		mA	
I_{CC}	$V_{CC} = 5.5 \text{ V}$, See Note 2			11.7	17		11.7	17	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with J, \bar{K}, CLK , and PRE grounded then with J, \bar{K}, CLK , and CLR grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$	SN54F109		SN74F109		UNIT		
			'F74		MIN MAX				
			MIN	MAX	MIN	MAX			
f_{clock}	Clock frequency		0	100	0	70	0	90	MHz
t_w	Pulse duration	CLK high, PRE or CLR low	4		4		4		ns
		CLK low	5		5		5		
t_{su}	Setup time, data before CLK^{\uparrow}	High	3		3		3		ns
		Low	3		3		3		
	Setup time, inactive-state before $\text{CLK}^{\uparrow\$}$	PRE or CLR to CLK	2		2		2		
t_h	Hold time, data after CLK^{\uparrow}	High	1		1		1		ns
		Low	1		1		1		

§ Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = 25^\circ\text{C}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^{\dagger\ddagger}$			UNIT		
				'F109					
				MIN	TYP	MAX	MIN	MAX	
f_{max}			100	150			70	90	MHz
t_{PLH}	CLK	Q or \bar{Q}	3	4.9	7		3	9	ns
			3.6	5.8	8		3.6	10.5	
t_{PHL}	PRE or CLR	Q or \bar{Q}	2.4	4.8	7	2.4	9	2.4	ns
			2.7	6.6	9	2.7	11.5	2.7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9758001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9758001Q2A SNJ54F 109FK	Samples
5962-9758001QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J	Samples
5962-9758001QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W	Samples
JM38510/34102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 34102B2A	Samples
JM38510/34102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 34102BEA	Samples
JM38510/34102BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 34102BFA	Samples
M38510/34102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 34102B2A	Samples
M38510/34102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 34102BEA	Samples
M38510/34102BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 34102BFA	Samples
SN74F109D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F109	Samples
SN74F109DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F109	Samples
SN74F109DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F109	Samples
SN74F109DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F109	Samples
SN74F109N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F109N	Samples
SNJ54F109FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9758001Q2A SNJ54F	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54F109J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J	Samples
SNJ54F109W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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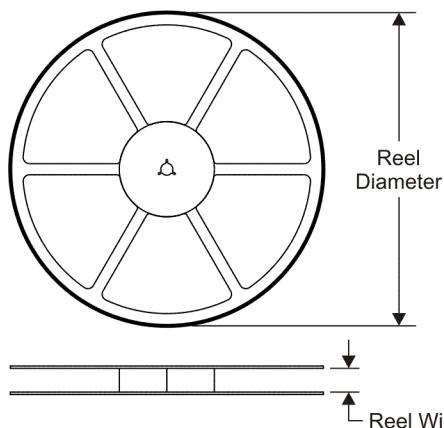
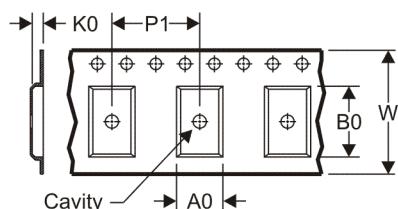
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OTHER QUALIFIED VERSIONS OF SN54F109, SN74F109 :

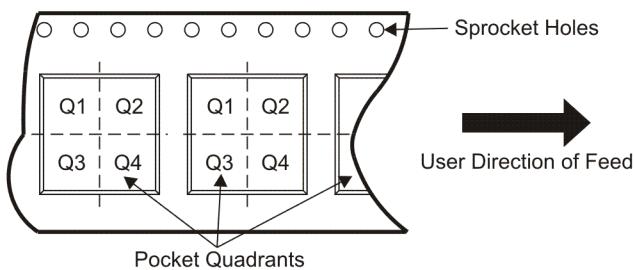
- Catalog: [SN74F109](#)
- Military: [SN54F109](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


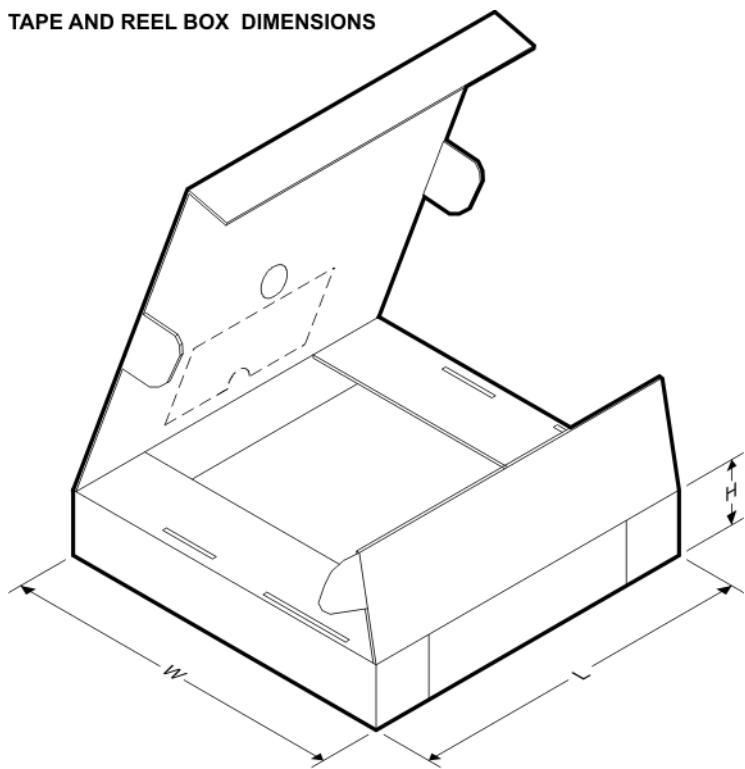
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F109DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



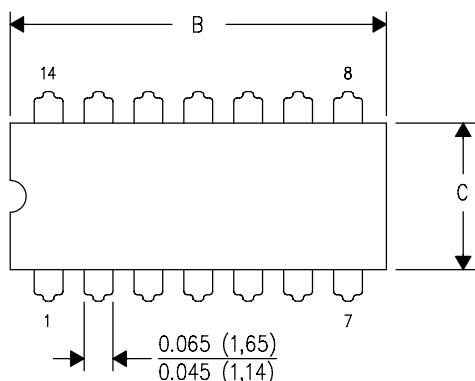
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F109DR	SOIC	D	16	2500	333.2	345.9	28.6

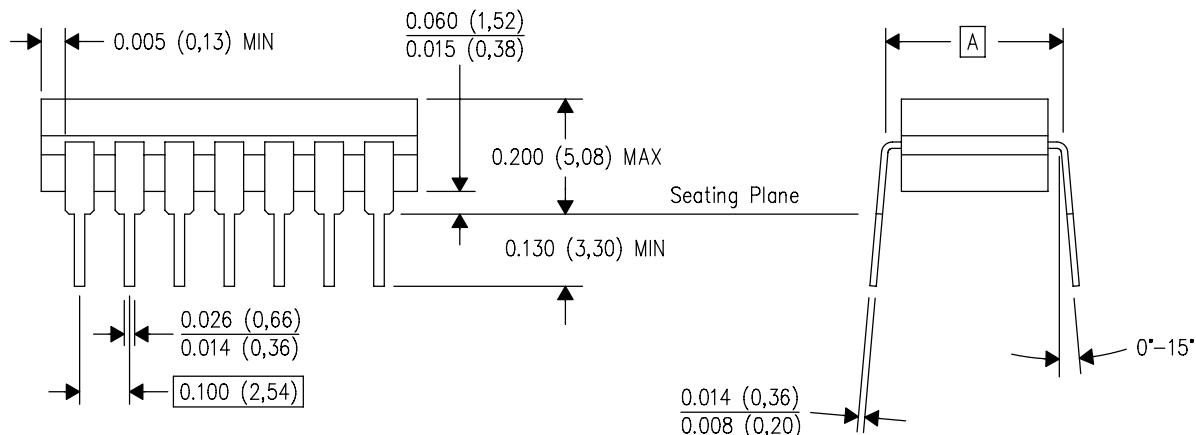
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

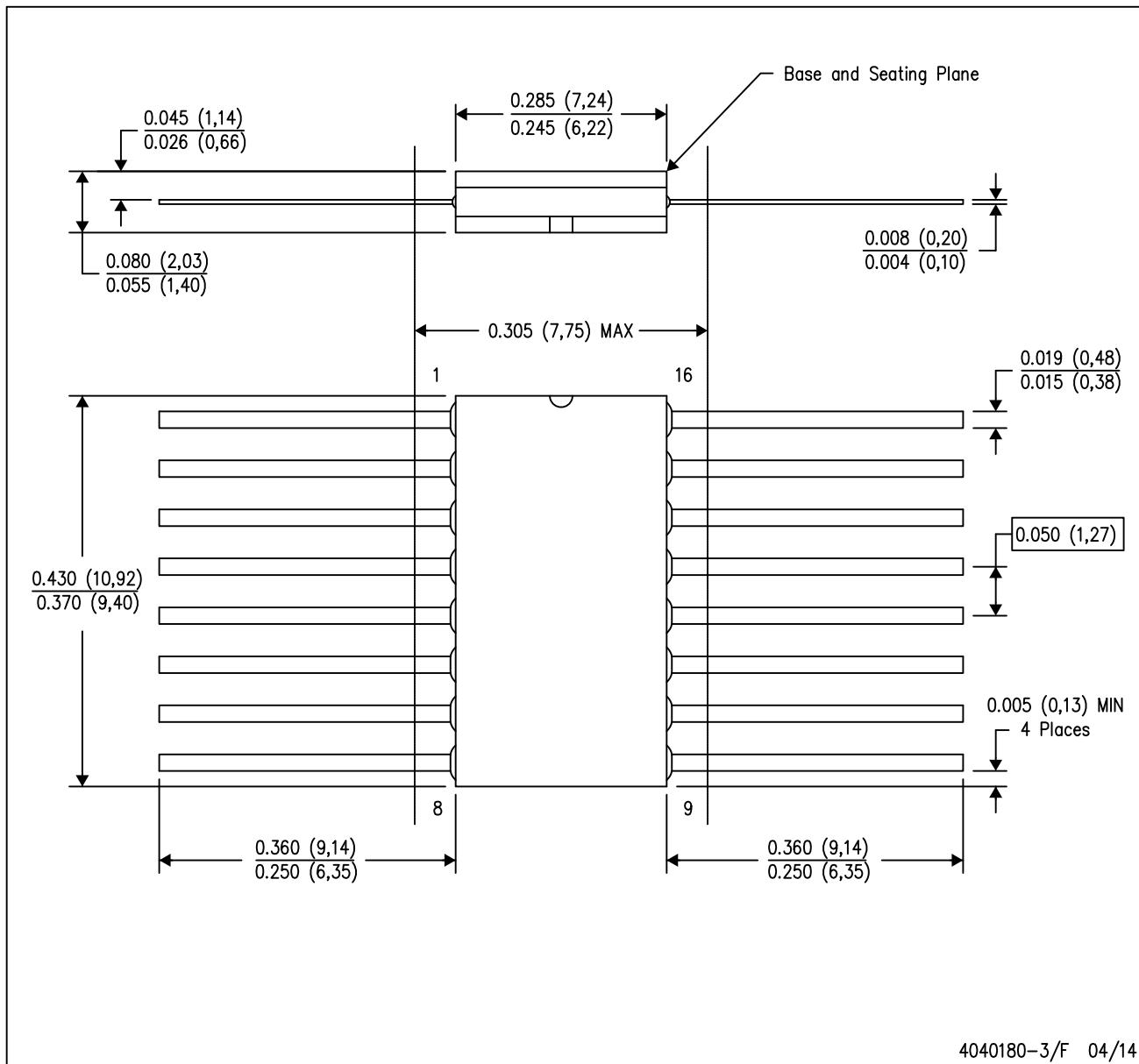


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



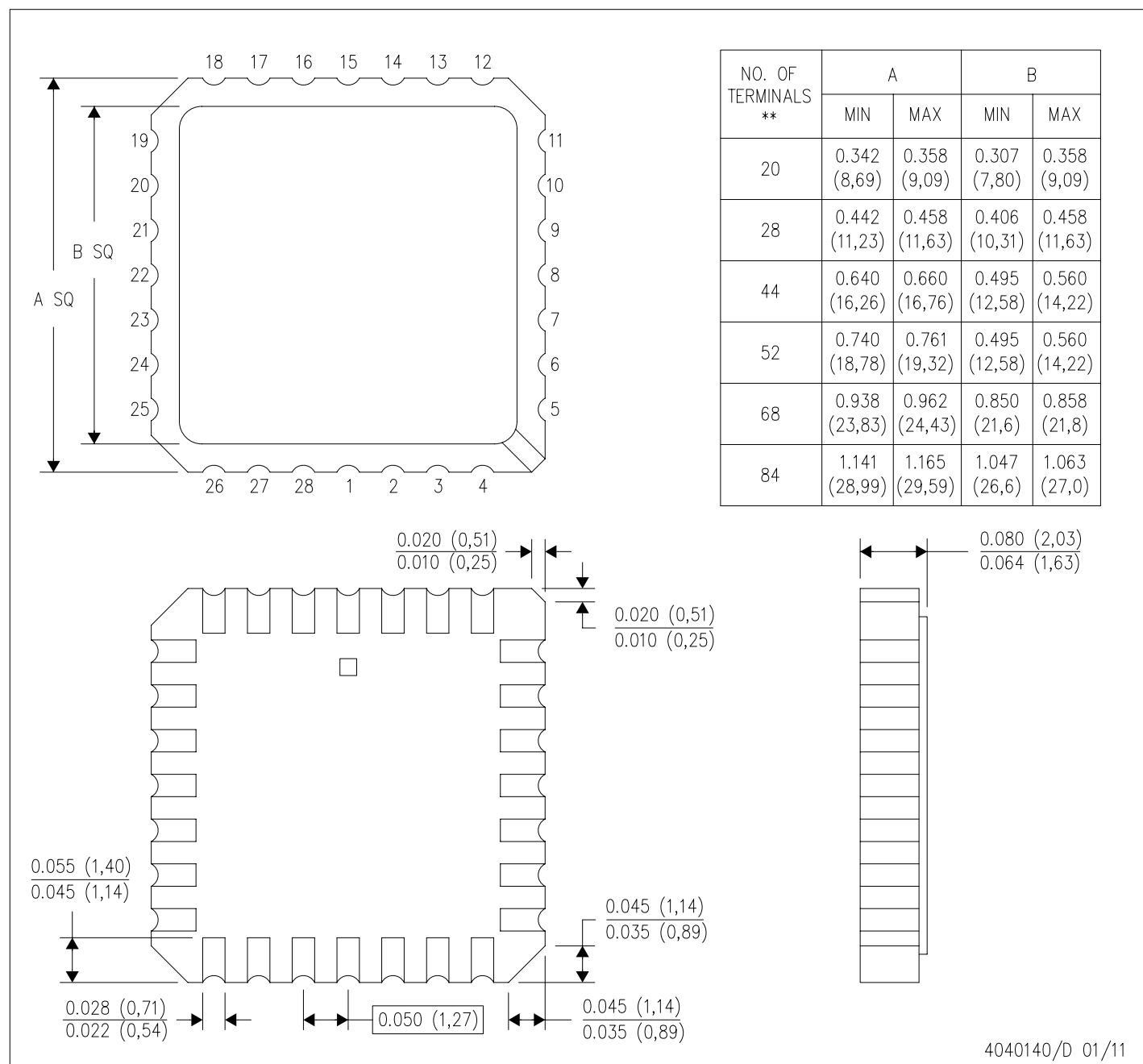
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

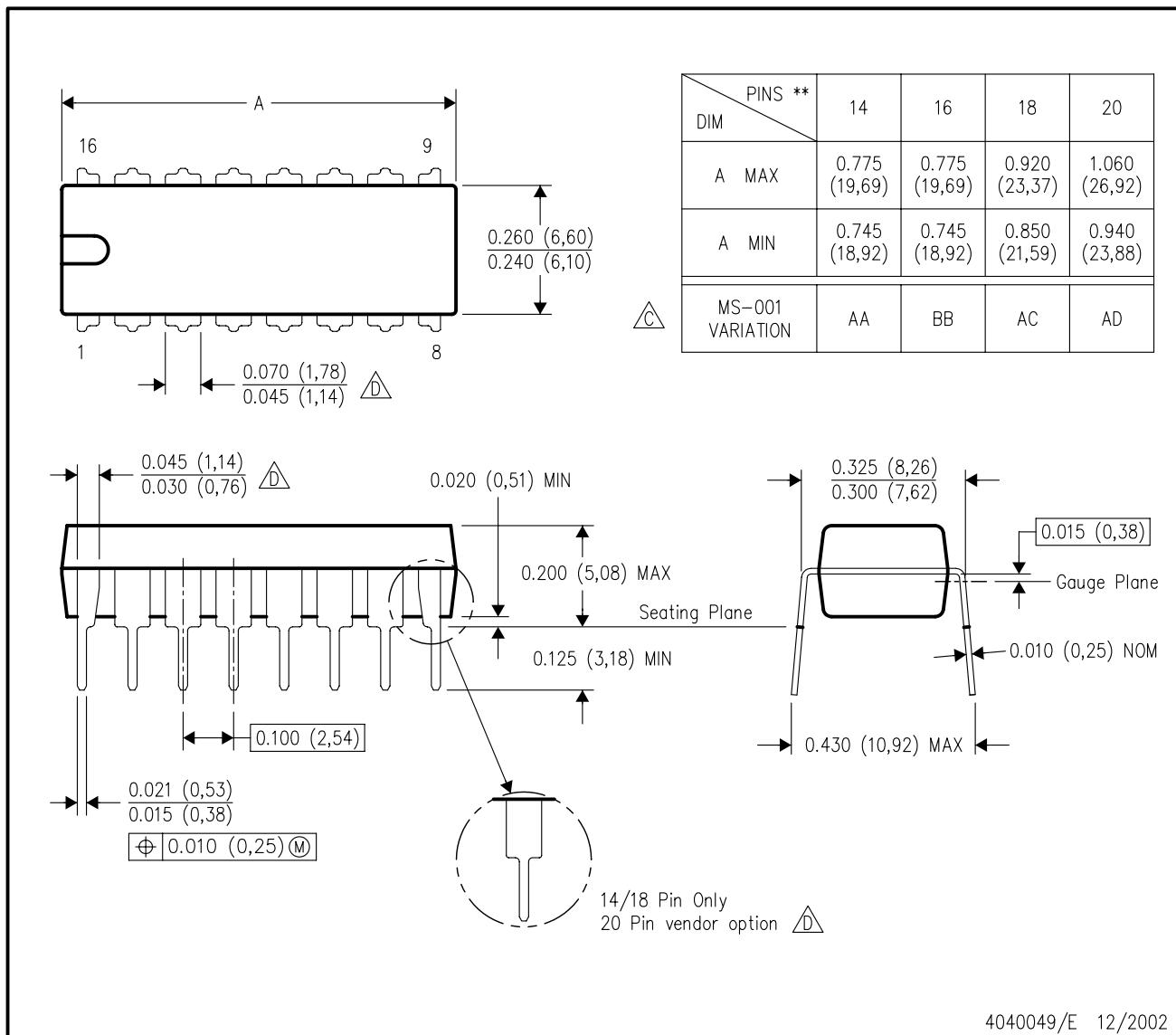
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



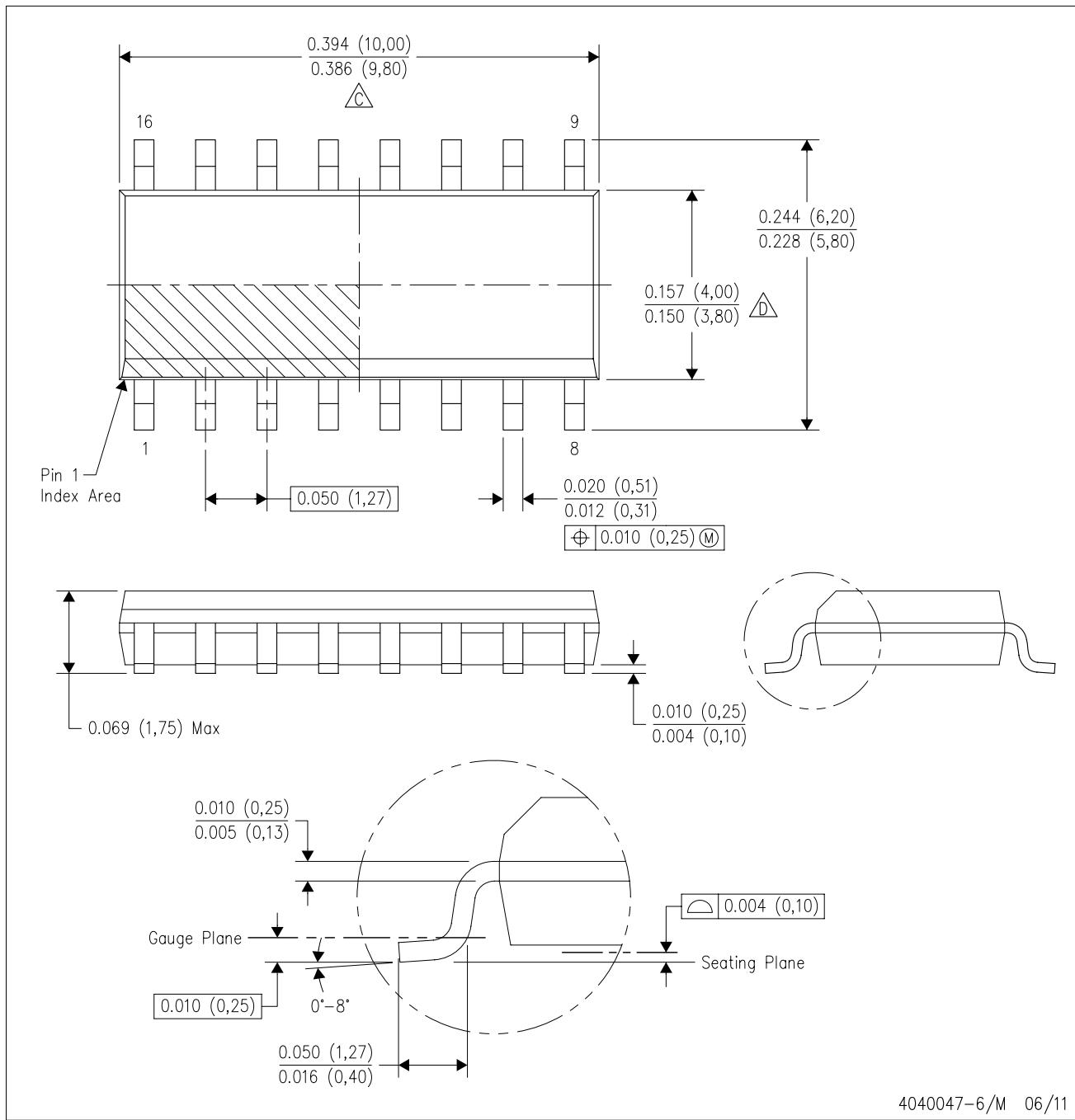
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

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