DATA SHEET

LP2985A-XX/LP2985AB-XX

Very low noise, low dropout, 150 mA linear regulator, CMOS process technology

Product data
Replaces LP2985A-XX dated 2003 Aug 18

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Philips Semiconductors

PHILIPS

Very low noise, very low dropout, 150 mA linear regulator, CMOS process technology

LP2985A-XX/ LP2985AB-XX

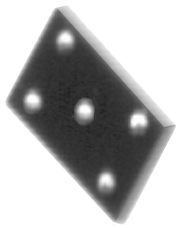
GENERAL DESCRIPTION

The LP2985A/AB-XX family are very low-noise, very low-dropout, low quiescent-current linear regulators designed for battery-powered applications, although they can also be used for devices powered by AC-DC converters. The parts are available in a range of preset output voltages from 2.5 V to 4.5 V. Typical dropout voltages are only 165 mV at 150 mA and 41 mV at 50 mA. Reverse battery current is extremely low, 0.5 μA typical.

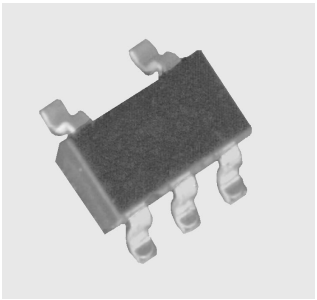
For demanding applications, output noise voltage of typically 30 μV_{rms} is achieved with a 0.01 μF capacitor on the bypass pin. The input voltage can vary from 2.5 to 6.5 V_{dc}, providing up to 150 mA output current.

An internal P-channel FET pass transistor maintains an 85 μA typical supply current, independent of the load current and dropout voltage. Other features include a 0.01 μA logic-controlled shutdown, short circuit and thermal shutdown protection, and reverse battery protection. The LP2985A-XX also includes an auto-discharge function which actively dischargers the output voltage to ground when the device is placed in shutdown.

To accommodate high density layouts, it is packaged in wafer-level chip-scale package (WL-CSP5) and regular SO5/SOT23-5 package.



WL-CSP5 (bottom view)



SO5 (SOT23-5)

FEATURES

- Low output noise: 30 μV_{rms}
- Low dropout voltages: 165 mV at 150 mA, 41 mV at 50 mA
- Thermal overload and short circuit protection
- Reverse battery protection
- Output current limit
- 85 μA no load supply current
- 100 μA typical operating supply current at I_{OUT} = 150 mA
- Preset output voltage of 2.7 V, 2.8 V, and 3.0 V; other voltages upon request in 100 mV increments

APPLICATIONS

- Cordless, PCS, and cellular telephones
- PCMCIA cards and modems
- Handheld and portable instruments
- Palmtop computers and electronic planners

SIMPLIFIED DEVICE DIAGRAM

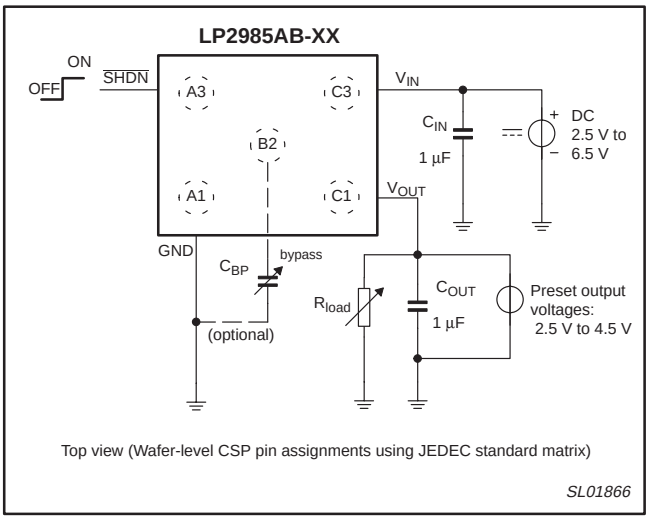


Figure 1. LP2985AB-XX Simplified device diagram.

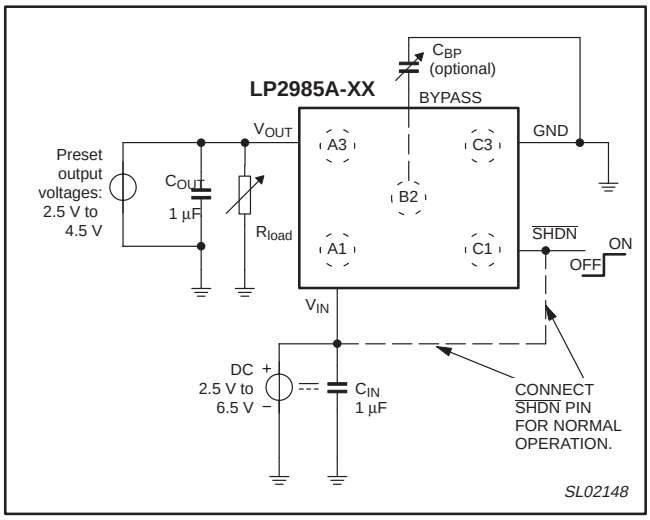


Figure 2. LP2985A-XX Simplified device diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
LP2985AB-**XX**UK	WL-CSP5	wafer-level, chip-scale 5 bump package, surface mount	–40 to +85 °C
LP2985A-**XX**UK	WL-CSP5	wafer-level, chip-scale 5 bump package, surface mount	–40 to +85 °C
LP2985A-**XX**D	SO5/SOT23-5	plastic small outline package; 5 leads; body width 1.5 mm	–40 to +85 °C

NOTE:
The device has three (3) voltage output options, indicated by the **XX** on the Type Number. Additional voltage output options may be available (see Table 1).

XX	VOLTAGE (Typical)
LP2985AB-27	2.7 V
LP2985AB-28	2.8 V
LP2985AB-30	3.0 V
LP2985A-27	2.7 V
LP2985A-28	2.8 V
LP2985A-30	3.0 V

Table 1. Marking code

Each device is marked with a four letter code. The first three letters designate the product. The fourth letter, represented by ‘x’, is a date tracking code.

Part	Marking
LP2985AB-27UK	ASKx
LP2985AB-28UK	ASLx
LP2985AB-30UK	ASMx
LP2985A-27D, LP2985A-27UK	ACCx
LP2985A-28UK	ACAx
LP2985A-30UK	AMPx
LP2985A-25D (Note 1)	APXx
LP2985A-26D (Note 1)	APYx
LP2985A-28D	APZx
LP2985A-30D	ARAx
LP2985A-33D (Note 1)	ARBx
LP2985A-36D (Note 1)	ARCx
LP2985A-42D (Note 1)	ARDx
LP2985A-45D (Note 1)	AREx

1. Consult factory for availability.

PIN CONFIGURATION

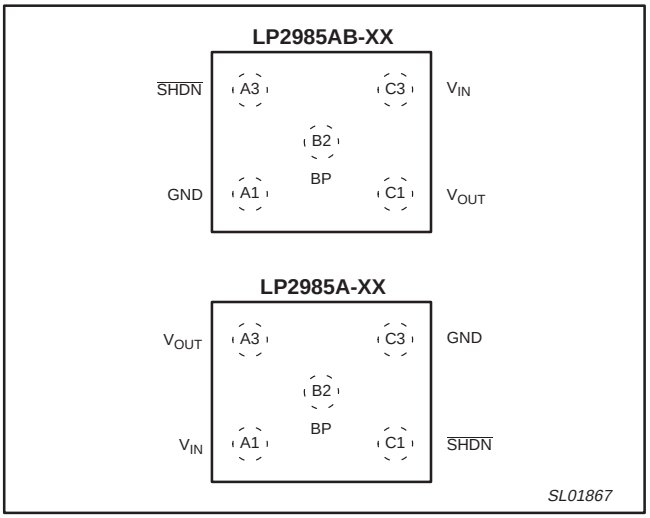


Figure 3. WL-CSP5 pin configuration (UK package).

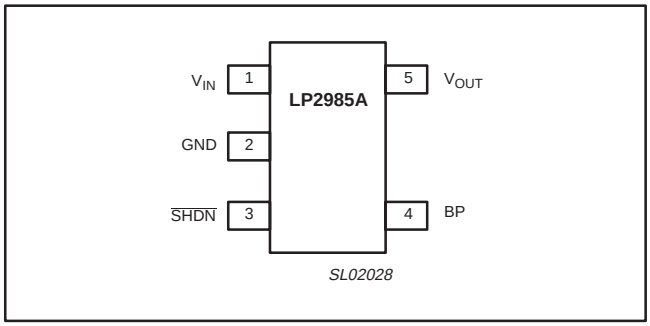


Figure 4. SO5/SOT23-5 pin configuration (D package).

PIN DESCRIPTION

BALL NO.		PIN NO.	SYMBOL	DESCRIPTION
LP2985AB-XX	LP2985A-XX			
A1	C3	2	GND	Ground. The bump may also serve as heat spreader by soldering it to a large PCB pad or circuit board ground plane to maximize power dissipation.
C1	A3	5	V_{OUT}	Regulator output. Sources up to 150 mA. Minimum output capacitor is 1 µF.
B2	B2	4	BP	Noise Bypass Pin: Low noise of typically 30 mV_{rms} with optional 0.01 µF bypass capacitor. Larger bypass capacitor further reduces noise.
A3	C1	3	$\overline{SHDN}$	Active-LOW Shutdown Input. This pin must be actively terminated. Tie to V_{IN} if this function is not used.
C3	A1	1	V_{IN}	Regulator Input. Supply voltage ranges from 2.5 V to 6.5 V. Bypass with a 1 µF capacitor to GND.

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IN}	Input voltage	2.5	+6.5	V
$V_{\overline{SHDN}}$	$\overline{SHDN}$ to GND voltage	–0.3	+6.5	V
$V_{\overline{SHDN}}$-V_{IN}	$\overline{SHDN}$ to V_{IN} voltage	–0.3	+6.5	V
V_{OUT}, V_{BP}	V_{OUT} and BP to GND voltage	–0.3	V_{IN} + 0.3	V
T_{stg}	Storage temperature range	–65	+150	°C
T_j	Junction temperature range	–55	+140	°C
T_{amb}	Ambient temperature range	–40	+85	°C
$R_{th(j-a)}$	Thermal resistance from junction to ambient	–	224	°C/W
P_D	Power dissipation (T_{amb} = 25 °C) (Derating factor above 25 °C)	–	637 5.1	mW mW/°C

NOTE:

2. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated condition is not implied. Functional operation should be restricted to the Recommended Operating Condition.
3. The absolute maximum power dissipation depends on the ambient temperature and can be calculated using the formula:

$$P_D = \frac{T_j - T_{amb}}{R_{th(j-a)}}$$

where T_j is the junction temperature, T_{amb} is the ambient temperature, and $R_{th(j-a)}$ is the junction-to-ambient thermal resistance. The 357 mW rating for SOT23-5 appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150 °C, to T_j, 70 °C for T_{amb}, and 220 °C/W for $R_{th(j-a)}$.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C (see Note 1), $V_{IN} = V_{OUT(nom)}$ + 0.5 V, –40 °C ≤ T_{amb} ≤ +85 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IN}	Input voltage			2.5	–	6.5	V
	Output voltage accuracy	I_{OUT} = 1 mA; T_{amb} = +25 °C; $V_{OUT} \geq$ 2.5 V		–1.4	–	1.4	%
		I_{OUT} = 1 mA to 150 mA; –40 °C ≤ T_{amb} ≤ +85 °C; $V_{OUT} \geq$ 2.5 V		–3.0	–	2.0	%
		I_{OUT} = 1 mA, T_{amb} = +25 °C, V_{OUT} < 2.5 V		–3.0	–	3.0	%
		I_{OUT} = 1 mA to 150mA; –40 °C ≤ T_{amb} ≤ +85 °C; V_{OUT} < 2.5 V		–3.5	–	3.5	%
$I_{OUT(max)}$	Maximum output current			150	–	–	mA
I_{LIM}	Current limit			160	390	–	mA
I_Q	Ground pin current	I_{OUT} = 0 mA		–	85	180	µA
		I_{OUT} = 150 mA		–	100	–	µA
I_{RBC}	Reverse battery current			–	0.5	–	µA
ΔV_{lnr}	Line regulation	2.5 V or (V_{OUT} + 0.1 V) ≤ V_{IN} ≤ 6.5V; I_{OUT} = 1 mA		–0.125	0	+0.125	%/V
ΔV_{ldr}	Load regulation	0.1 mA ≤ $I_{OUT;}$ C_{OUT} = 1.0 µF		–	0.01	0.02	%/mA
	Dropout voltage (Note 2)	I_{OUT} = 1 mA		–	1.0	–	mV
		I_{OUT} = 50 mA		–	41	90	mV
		I_{OUT} = 150 mA		–	165	–	mV
V_N	Output voltage noise	f = 10 Hz to 100 kHz C_{BP} = 0.01 µF	C_{OUT} = 10 µF	–	30	–	μV_{RMS}
			C_{OUT} = 100 µF	–	20	–	μV_{RMS}
Shutdown							
V_{IH}	$\overline{SHDN}$ input threshold	2.5 V ≤ V_{IN} ≤ 6.5 V		1.6	–	–	V
V_{IL}				–	–	0.4	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ input bias current	$V_{\overline{SHDN}} = V_{IN}$	T_{amb} = +25 °C	–	–	100	nA
			T_{amb} = +85 °C	–	0.5	–	µA
$I_{Q(\overline{SHDN})}$	$\overline{SHDN}$ supply current	V_{OUT} = 0 V	T_{amb} = +25 °C	–	0.01	1	µA
$t_{\overline{SHDN}\text{-Delay}}$	Shutdown exit delay (Note 3)	C_{BP} = 0.01 µF C_{OUT} = 1.0 µF; no load	T_{amb} = +25 °C	–	30	150	µs
			–45 °C ≤ T_{amb} ≤ +85 °C	–		300	µs
R_{SD}	Resistance shutdown discharge			–	300	–	Ω
Thermal protection							
$T_{\overline{SHDN}}$	Thermal shutdown junction temperature			–	140	–	°C
$\Delta T_{\overline{SHDN}}$	Thermal shutdown hysteresis			–	15	–	°C

NOTES:

1. Limits are 100% production tested at T_{amb} = +25 °C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) Methods.
2. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 100 mV below the value of V_{OUT} for $V_{IN} = V_{OUT}$ + 0.5 V. (Only applicable for V_{OUT} = +2.5 V to +4.5 V.)
3. Time needed for V_{OUT} to reach 95% of final value.

TYPICAL PERFORMANCE CURVES

LP2985A with conditions: $V_{IN} = V_{OUT(nom)} + 0.5$ V; $T_{amb} = -40$ °C to +85 °C unless otherwise noted. Typical values are at $T_{amb} = +25$ °C.

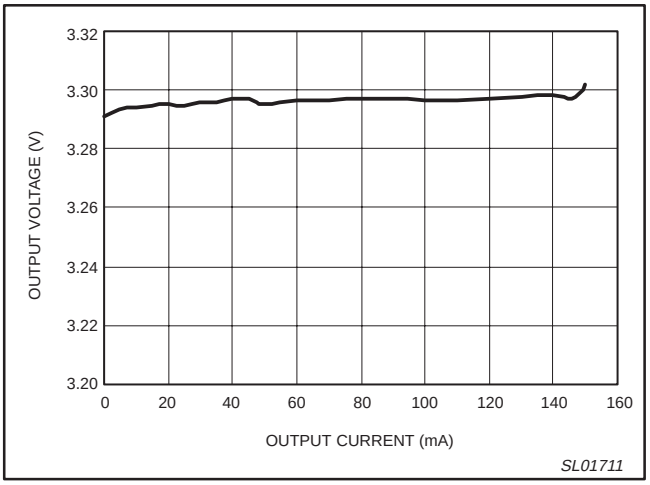


Figure 5. Output voltage versus output current.

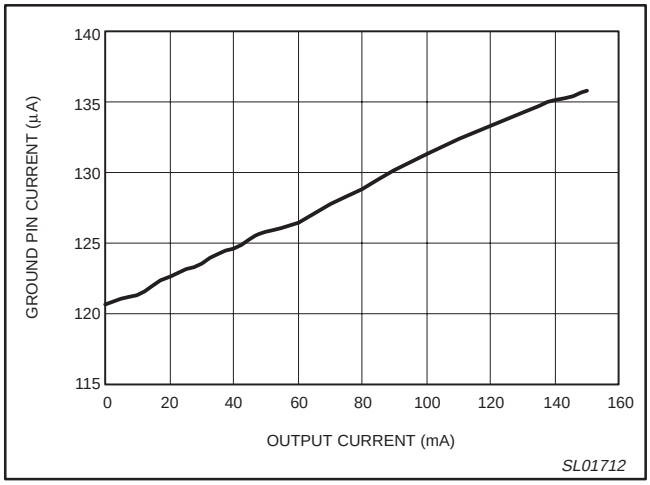


Figure 6. GND pin current versus output current.

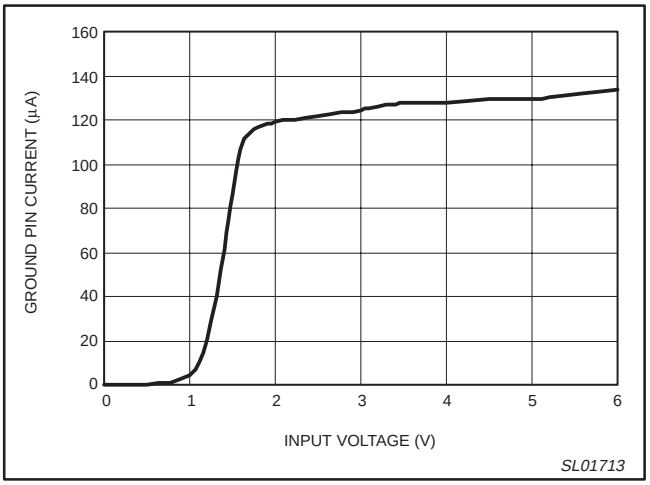


Figure 7. GND pin current (no load) versus input voltage.

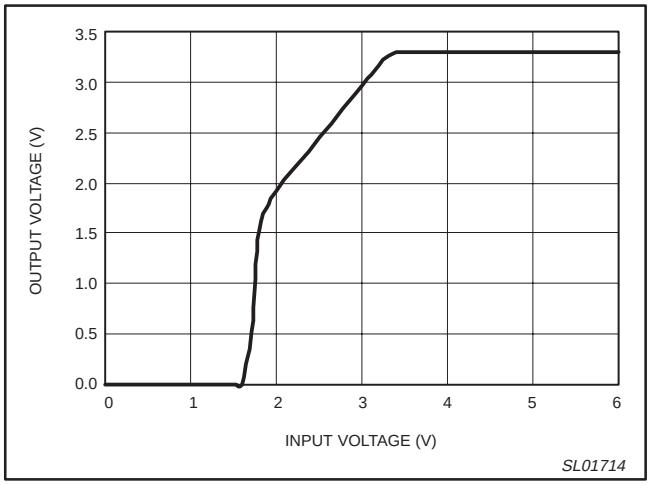


Figure 8. Output voltage (I_{OUT} = 50 mA) versus input voltage.

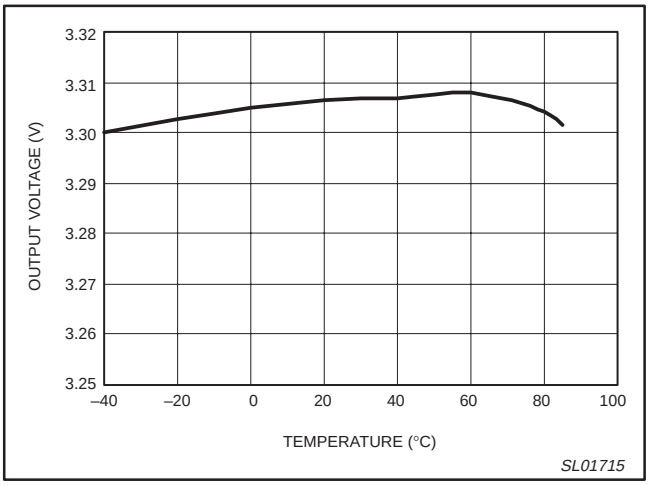


Figure 9. Output voltage (50 mA load) versus temperature.

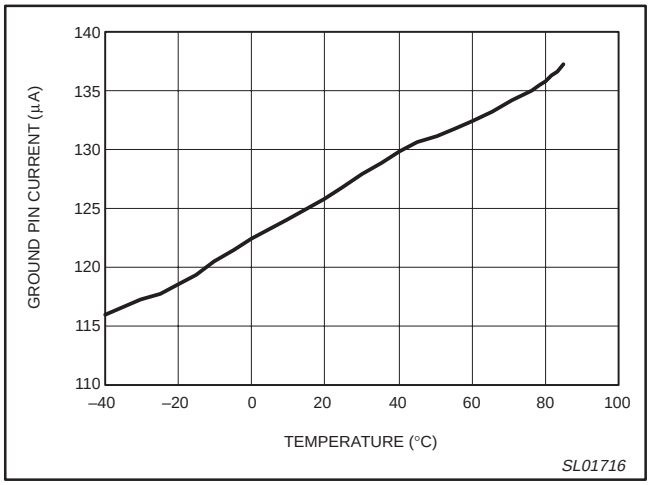


Figure 10. GND pin current (50 mA load) versus temperature.

TYPICAL PERFORMANCE CURVES (continued)

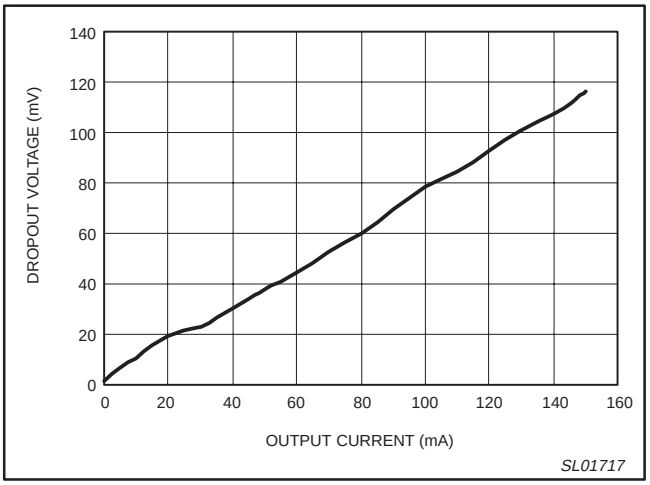


Figure 11. Dropout voltage versus output current.

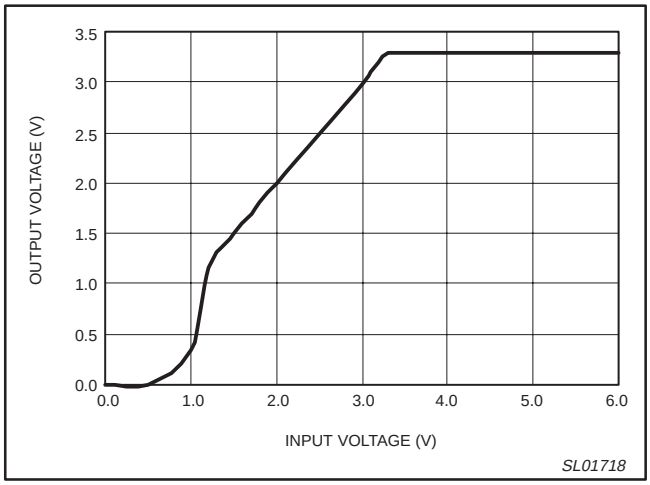


Figure 12. Output voltage (no load) versus input voltage.

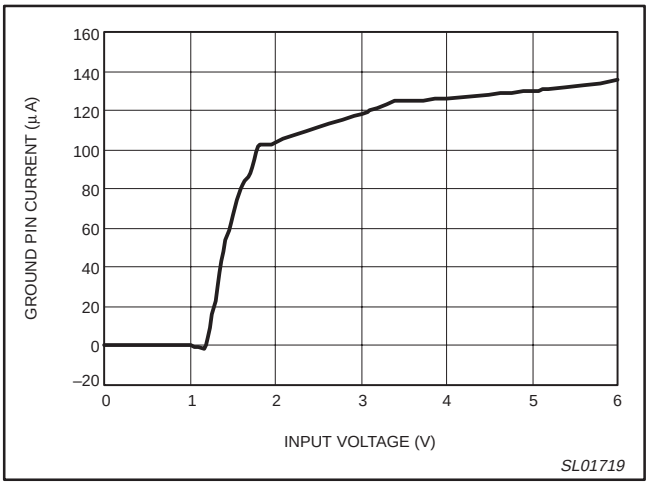


Figure 13. GND pin current (50 mA) versus input voltage.

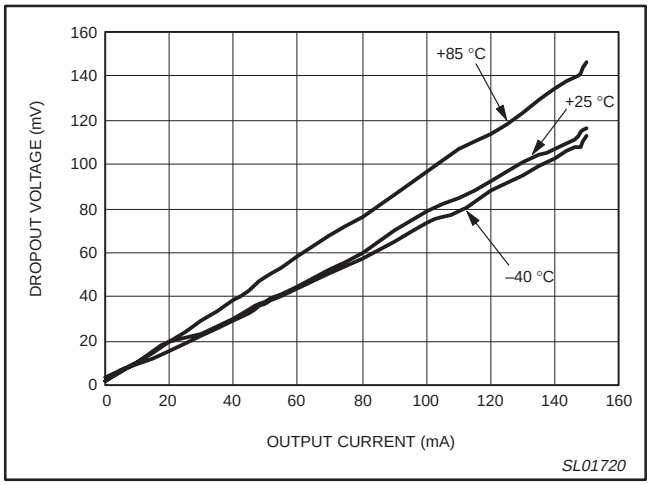


Figure 14. Dropout voltage versus output current.

TYPICAL PERFORMANCE CURVES (continued)

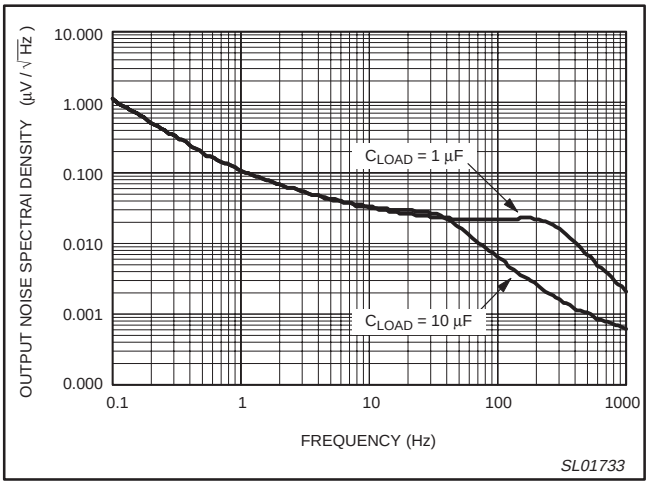


Figure 15. Output noise spectral density versus frequency.

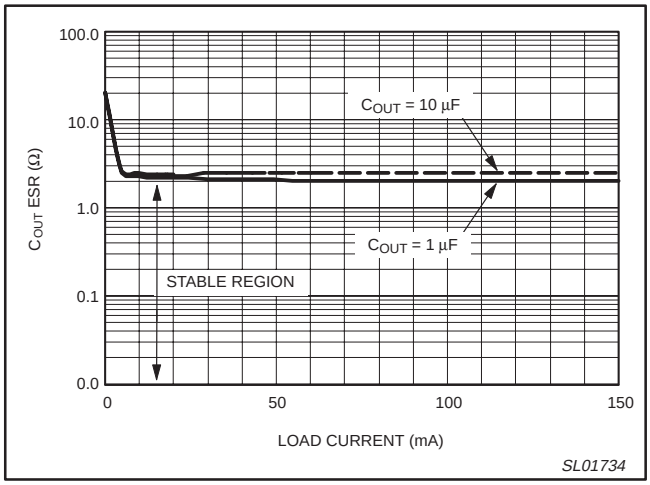


Figure 16. Region of stable C_{OUT} ESR versus load current.

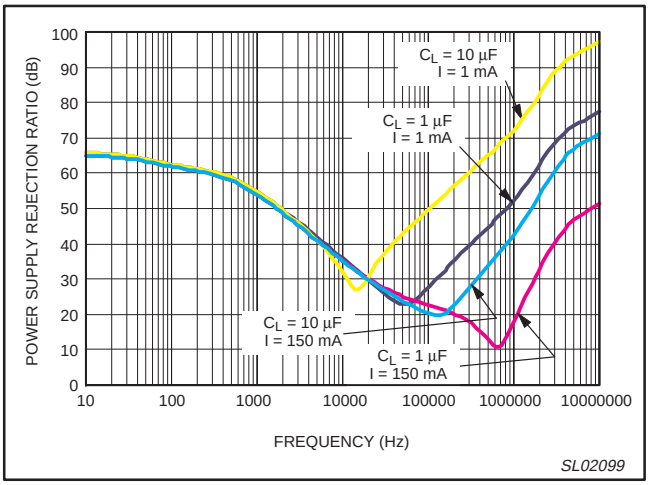


Figure 17. Power supply rejection ratio versus frequency.

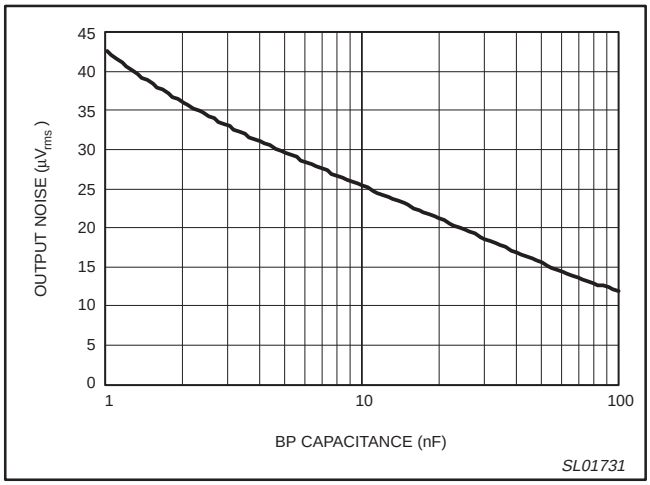


Figure 18. Output noise versus BP capacitance

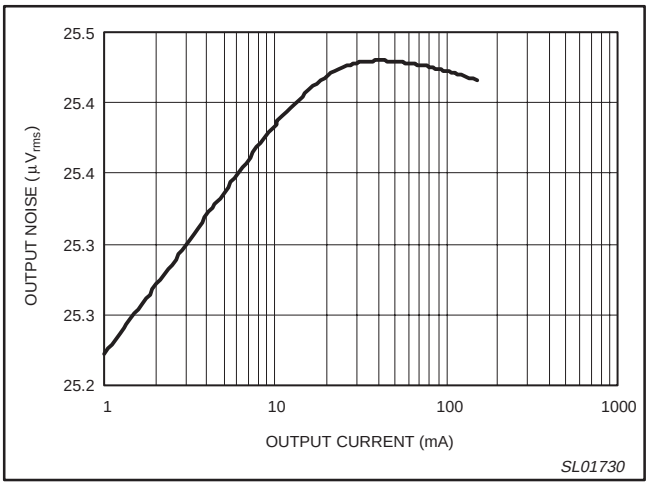


Figure 19. Output noise versus output current.

TYPICAL PERFORMANCE CURVES (continued)

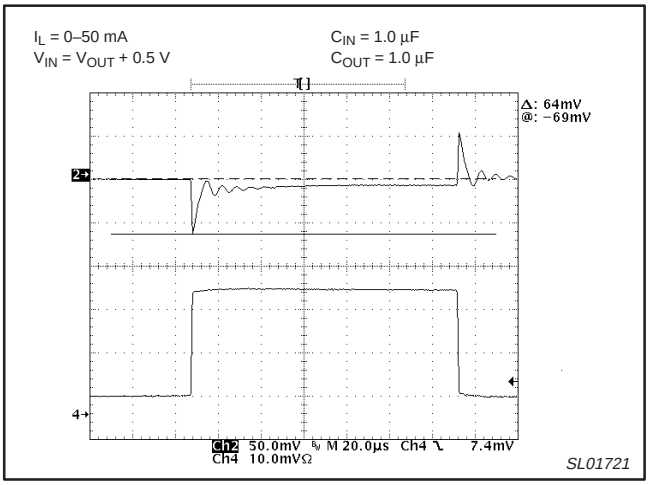


Figure 20. Load transient response (with power supply source).

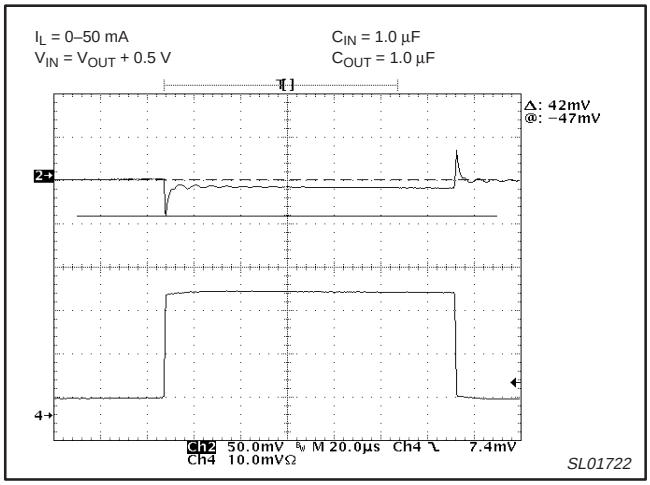


Figure 21. Load transient response (with AA battery source).

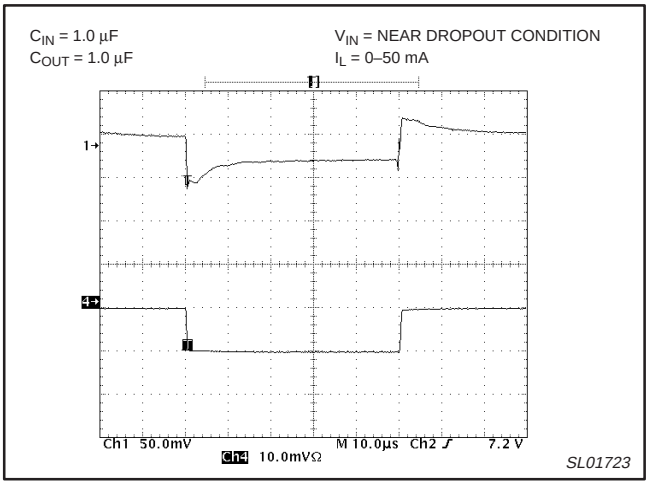


Figure 22. Load transient response.

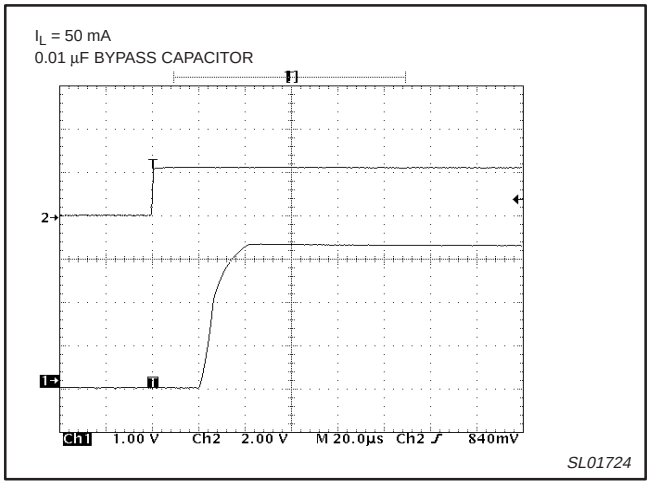


Figure 23. Shutdown exit delay.

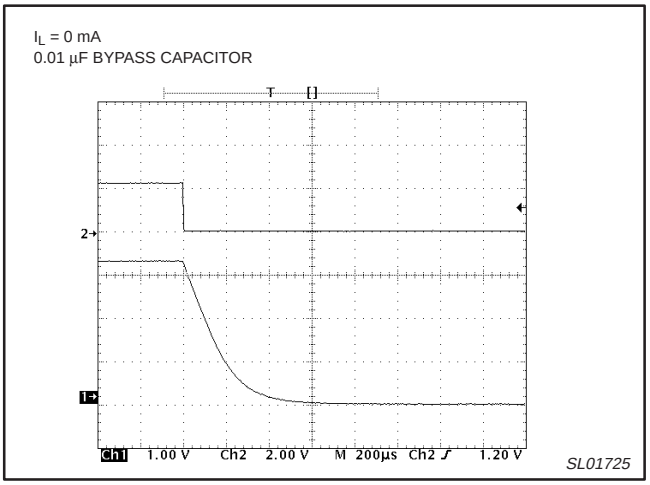


Figure 24. Entering shutdown (no load).

TECHNICAL DISCUSSION

The LP2985A-XX family are very low-noise, low-dropout, low quiescent-current linear regulators designed for battery-powered applications, although they can also be used for devices powered by AC-DC converters.

The voltage regulation components of the LP2985A-XX consist of a 1.23 V reference, an error amplifier, a P-channel pass transistor, and an internal feed-back voltage divider. The device also contains a reverse battery protection circuit, a thermal sensor, a current limiter, and shutdown logic.

Voltage regulation

The 1.23 V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, which allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. The output voltage is fed back through an internal resistor voltage divider connected to the V_{OUT} pin.

The LP2985A-XX uses a 1.0 Ω typical P-channel MOSFET pass transistor. The P-channel MOSFET requires no base drive, therefore the device has lower quiescent current than a comparable PNP transistor-based design. The LP2985A-XX uses 100 µA of quiescent current under any load conditions.

An optional external bypass capacitor connected between the BP pin and ground reduces noise at the output.

Power dissipation

The LP2985A's maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT} (V_{IN} – V_{OUT})$. The maximum power dissipation is:

$$P_{MAX} = (T_j – T_{amb}) / (\Theta_{JB} + \Theta_{BA})$$

where $T_j – T_{amb}$ is the temperature difference between the LP2985A-XX die junction and the surrounding air, Θ_{JB} (or Θ_{JC}) is the thermal resistance of the package, and Θ_{BA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air.

The GND pin provides an electrical connection to ground and a path for heat transfer away from the junction. Connect the GND pin to ground using a large pad or ground plane to maximize heat transfer.

Noise reduction

An optional external 0.01 µF bypass capacitor at BP, in conjunction with an internal 200 Ω resistor, creates an 80 Hz low-pass filter for noise reduction. The LP2985A-XX produces 30 μV_{RMS} of output voltage noise with C_{BP} = 0.01 µF and C_{OUT} = 10 µF. This is negligible in most applications.

Start-up time is minimized by a power-on circuit that pre-charges the bypass capacitor. The 'Typical Performance Curves' section shows graphs of 'Output noise versus BP capacitance' (Figure 18), 'Output noise versus output current' (Figure 19), and 'Output noise spectral density versus frequency' (Figure 15).

Device protection

The LP2985A-XX has several built-in protection circuits.

Current limiter: The current limiter controls the the pass transistor's gate voltage so the output current cannot exceed 390 mA. We recommend using 160 mA minimum to 500 mA maximum in the design parameters. Because of the current limiter, the output can be shorted to ground for an indefinite amount of time with no damage to the part.

Reverse battery protection: The reverse battery protection circuit prevents damage to the device if the supply battery is accidentally installed backwards. This circuit compares V_{IN} and V_{SHDN} to ground and disconnects the device's internal circuits if it detects reversed polarity. Reverse supply current is limited to 1 mA when this protective circuit is active, preventing the battery from rapidly discharging through the device.

Thermal overload protection: When the junction temperature exceeds +140 °C, the thermal sensor signals the shutdown logic to turn off the pass transistor. After the junction temperature has cooled by 15 °C the sensor signals the shutdown logic to turn the pass transistor on again. This will create a pulsed output during lengthy thermal overloads.

NOTE: Thermal overload protection is to protect the device during fault conditions. Do not exceed the maximum junction-temperature rating of T_j = +150 °C during continuous operation.

APPLICATION INFORMATION

Capacitor selection and regulator stability

Normally, use a 1 μF capacitor on the LP2985A-XX input and a 1 μF to 10 μF capacitor on the output. To improve the supply-noise rejection and line-transient response, use input capacitor values and lower ESRs. To reduce noise and improve load-transient response, stability, and power-supply rejection, use use large output capacitors.

For stable operation over the full temperature range and with load currents up to 150 mA, a 1 μF (min.) ceramic capacitor is recommended.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to increase the capacitance by a factor of 2 or more to ensure stability at temperatures below –10 °C. With X7R or X5R dielectrics, 1 μF should be sufficient at all operating temperatures for V_{OUT} = 2.5 V.

A graph of the Region of Stable C_{OUT} ESR versus Load Current is shown in Figure 16. Use a 0.01 μF bypass capacitor at BP for low output voltage noise. Increasing the capacitance will slightly decrease the output noise, but increase the start-up time. Values above 0.1 μF provide no performance advantage and are not recommended (see Figures 23 and 24 in the ‘Typical Performance Curves’).

Load-transient considerations

The LP2985A-XX load-transient response graphs (Figures 20, 21, and 22) show two components of the output response: a DC shift from the output impedance due to the load current change, and the transient response. Typical transient for a step change in the load current from 0 mA to 50 mA is 40 mV. Increasing the output capacitor’s value and decreasing the ESR attenuates the overshoot.

PSRR and operation from sources other than batteries

The LP2985A-XX is designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors, and through passive filtering techniques.

Power-supply rejection is 63 dB at low frequencies and rolls off above 10 kHz. See Figure 17, ‘Power supply rejection ratio versus frequency’. Figures 20, 21, and 22 show the LP2985A’s line- and load-transient responses.

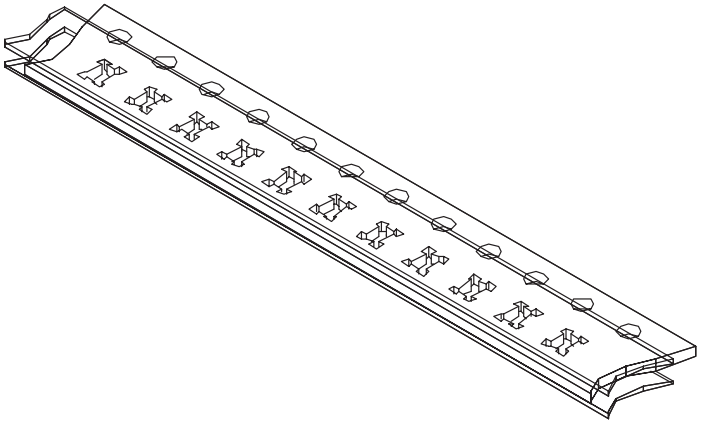
Input-output (dropout) voltage

For output voltage greater than the minimum input voltage (2.5 V), the regulator’s minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the LP2985A-XX uses a P-channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current (see ‘Typical Performance Curves’).

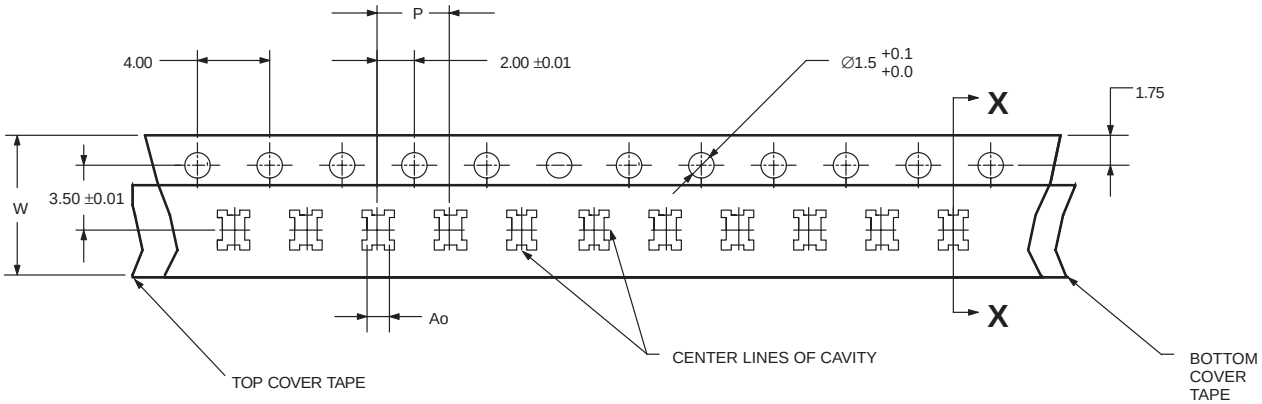
PACKING METHOD

The LP2985A-XX is packed in reels, as shown in Figure 25.

LOADED TAPE DIRECTION OF FEED



NOTES:
All dimensions in millimeters.
10 sprocket hole pitch cumulative tolerance ±0.20
Material: conductive polystyrene
Camber not to exceed 1.0 mm in 100 mm.
Cover tape shown for illustrative purposes only.

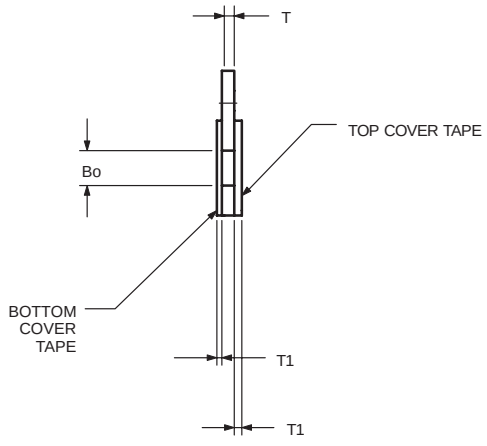


DIMENSIONS (mm are the original dimensions)

UNIT	Ao	Bo	T	T1	P	W
mm	1.09 0.99	1.598 1.498	0.76 0.74	0.10 (max.)	4.05 3.95	8.3 7.9

Heat seal cover tape for carrier tape width 8 mm

Type tape:	clear static dissipative tape
Base material:	transparent polyester
Cover tape width:	5.3 ± 0.1 mm
Cover tape length:	480 m/reel
Supplier:	Advanced Integrated Materials (AIM)
Part Number:	CT5–00530–0480

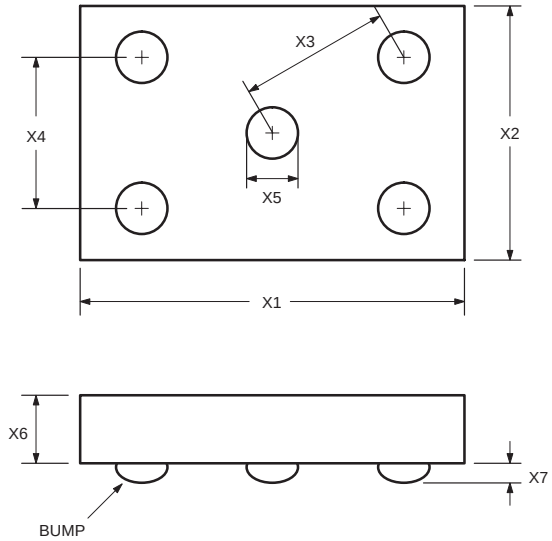


SECTION 'X – X'

SL02056

Figure 25. Tape and reel packing method.

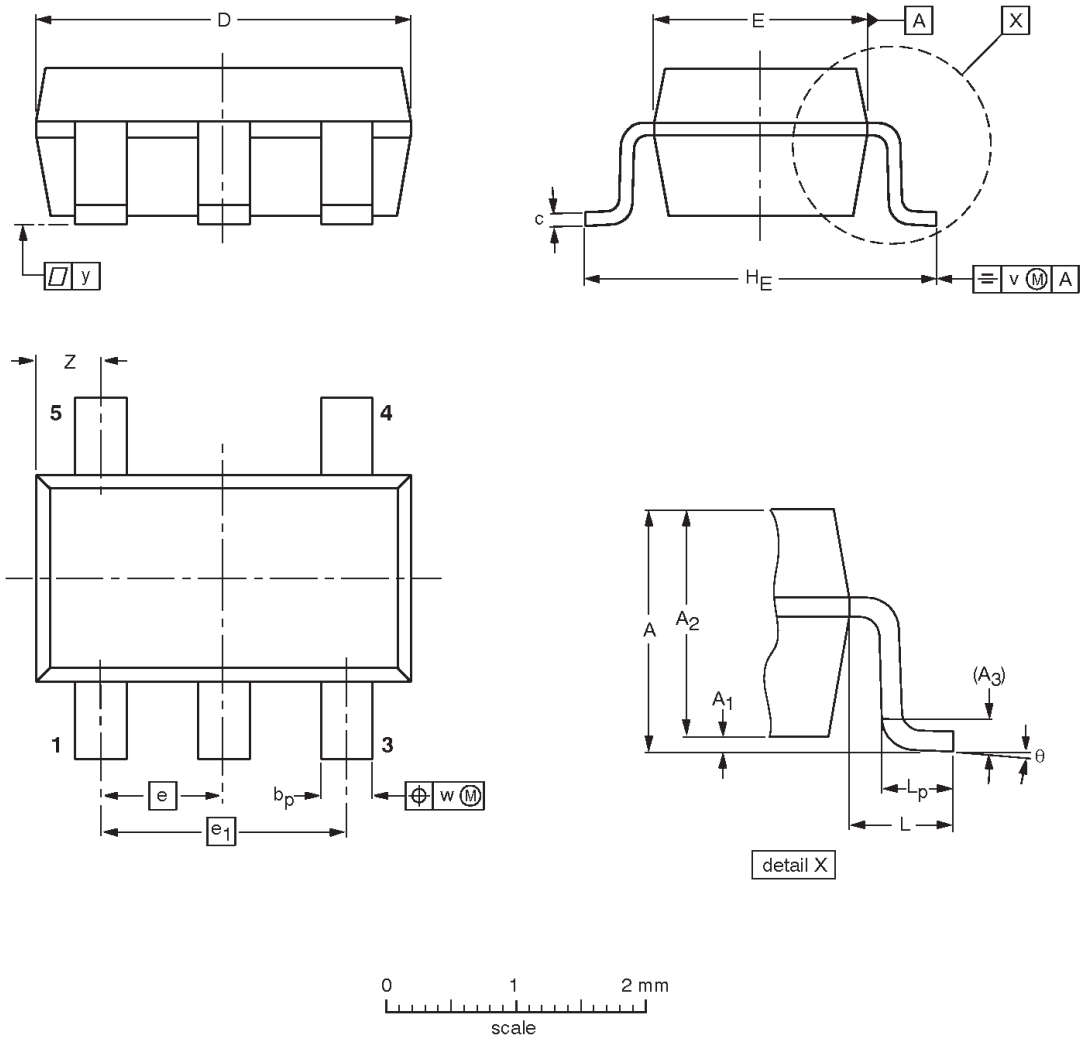
WL-CSP5: wafer level, chip-scale package; 5 bumps



DIMENSIONS (mm are the original dimensions)

UNIT	X1	X2	X3	X4	X5	X6	X7
mm	1.30 1.24	0.87 0.81	0.5	0.5	0.17	0.4 0.5	0.125 0.135

SOT23-5: plastic small outline package; 5 leads; body width 1.5 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p			y		θ
mm	1.35	0.15 0.05	1.2 1.0	0.25	0.55 0.41	0.22 0.08	3.00 2.70	1.70 1.50	0.95	1.90	3.00 2.60	0.60	0.55 0.35			0.1		8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			
	IEC	JEDEC	EIAJ	
		MO-178		

REVISION HISTORY

Rev	Date	Description
_5	20031002	**Product data (9397 750 12136); ECN 853-2417 30404 dated 01 October 2003. Replaces data sheet LP2985A-XX of 2003 Aug 18 (9397 750 11926).** Modifications: ● Add part type LP2985AB-XX. ● Figure 25 replaced.
_4	20030818	**Product data (9397 750 11926); ECN 853-2417 30203 dated 08 August 2003. Supersedes data of 2003 Jul 31 (9397 750 11751).**
_3	20030731	**Product data (9397 750 11751); ECN 853-2417 30090 dated 14 July 2003. Supersedes data of 2003 May 12 (9397 750 11501).**
_2	20030512	**Product data (9397 750 11501); ECN 853-2417 29829 dated 17 April 2003. Supersedes data of 2003 Apr 10 (9397 750 10998).**
_1	20030410	**Product data (9397 750 10998); ECN 853-2291 29248 dated 03 December 2002.**

Very low noise, very low dropout, 150 mA linear regulator, CMOS process technology

LP2985A-XX/
LP2985AB-XX

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Level	Data sheet status [1]	Product status [2] [3]	Definitions
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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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