CY4638

WirelessUSB™ LP VoIP Demo Kit Guide

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Contents

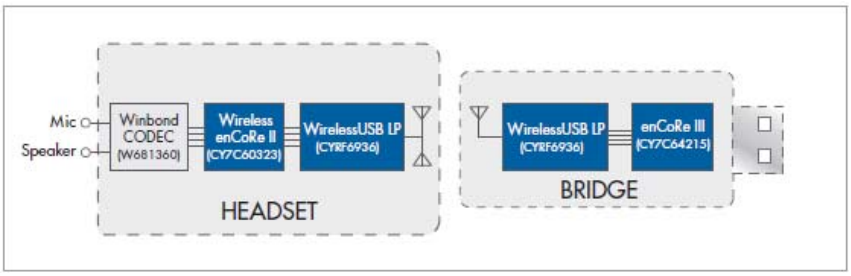
1. Introduction

Thank you for your interest in the CY4638 WirelessUSB™ LP VoIP Demo Kit featuring Cypress's CYRF6936 transceiver for point-to-point and multipoint-to-point wireless applications. This kit provides a design environment that introduces you to the WirelessUSB LP technology and enables you to develop a Wireless VoIP headset or handset.

PC-based voice over IP (VoIP) calls have proliferated with services such as Skype and Google Talk. VoIP users require wireless headsets for flexibility combined with long range and battery life. To meet this demand, designers require simple and easy-to-use platform to develop low-power and low-cost Wireless VoIP headset solutions.

Cypress provides this solution with the innovative dual antenna WirelessUSB LP VoIP Demo Kit. This kit provides a smart implementation of a robust, low-power, low-cost, duplex wireless headset to a single wireless receiver. It combines Cypress's WirelessUSB LP radio system-on-chip and enCoRe™ (Enhanced Component Reduction) microcontrollers with Winbond's W681360 13-bit low-power codec to implement clean signal quality and production-ready, 2.4 GHz wireless VoIP headsets.

Figure 1-1. VoIP Block Diagram



Getting Started chapter on page 9 describes the installation and configuration of the CY4638 WirelessUSB LP VoIP Demo Kit. Kit Operation chapter on page 15 and Hardware chapter on page 21 describes the kit and hardware operation. Code Examples chapter on page 37 describes the code examples provided with the kit. The Appendix on page 49 provides the schematics, bill of materials (BOM), and protocols associated with the CY4638 WirelessUSB LP VoIP Demo Kit.

The CY4638 WirelessUSB LP VoIP Demo Kit is used in the following applications:

- Wireless headset
- Wireless handset
- Voice activated toys
- Audio conference systems
- Wireless karaoke systems

1.1 Kit Contents

The CY4638 WirelessUSB LP VoIP Demo Kit includes:

- WirelessUSB headset board
- WirelessUSB Full-Speed USB bridge
- WirelessUSB LP VoIP Demo Kit CD/DVD-ROM
- Mono headset
- Battery charger
- USB extension cable for the bridge
- CY7C60323-PVXC, CYRF6936-40LTXC, and CY7C64215-28PVXC IC samples

Visit http://www.cypress.com/shop for more information. Inspect the contents of the kit. If any parts are missing, contact your nearest Cypress sales office for further assistance.

1.2 PSoC® Designer™

PSoC Designer is the integrated design environment (IDE) that you can use to customize your PSoC application. The latest version of PSoC Designer has many features, bug fixes, and support for new PSoC devices.

For more information about PSoC Designer, see the PSoC Designer IDE Guide located at: `<Install_Directory>:\Cypress\PSoC Designer\<version>\Documentation`

1.3 PSoC Programmer

PSoC Programmer 3.14 offers a simple GUI that connects to hardware and enables to program and configure PSoC devices.

1.4 Additional Learning Resources

Visit http://www.cypress.com for additional learning resources in the form of datasheets, technical reference manual, and application notes.

1.4.1 Reference Documents

- CYRF6936 - WirelessUSB LP 2.4 GHz Radio SoC
  http://www.cypress.com/?rID=14284
- CY7C603xx - enCoRe III Low Voltage
  http://www.cypress.com/?rID=13558
- MiniProg
  http://www.cypress.com/?rID=37459
- PSoC Designer Training
  http://www.cypress.com/?rID=40543

1.5 Document History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	05/06/2011	CSAI	Initial version of kit guide
*A	11/29/2011	ANTG	Updated web link in chapter 2
*B	03/28/2012	ANTG/ELIN	Corrected part number in section 4.2 to CY7C60323. Updated images in Getting Started section; Updated PSoC Programmer version
*C	05/03/2012	ELIN	Updated Figure 2-5. Added IC samples information in section 1.1

1.6 Documentation Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes cautions or unique functionality of the product.

2. Getting Started

This chapter describes the installation of the CY4638 WirelessUSB LP VoIP Demo Kit.

2.1 Kit Installation

To install the kit software, follow these steps:

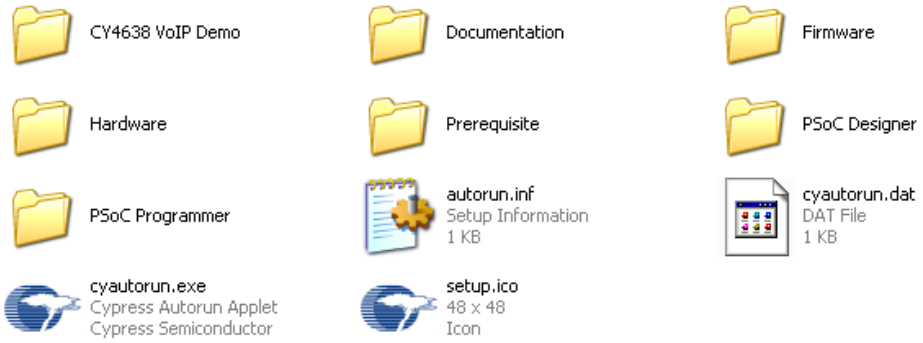
1. Insert the kit CD/DVD into the CD/DVD drive of your PC. The CD/DVD is designed to auto-run and the kit installer startup screen appears.

   You can also download the latest installer ISO file from http://www.cypress.com/go/CY4638. Create an installer CD/DVD or extract the ISO using WinRar and install the executables.
2. Click **Install CY4638 VoIP Demo Kit** to start the installation, as shown in Figure 2-1.

   Figure 2-1. Kit Installer Startup Screen

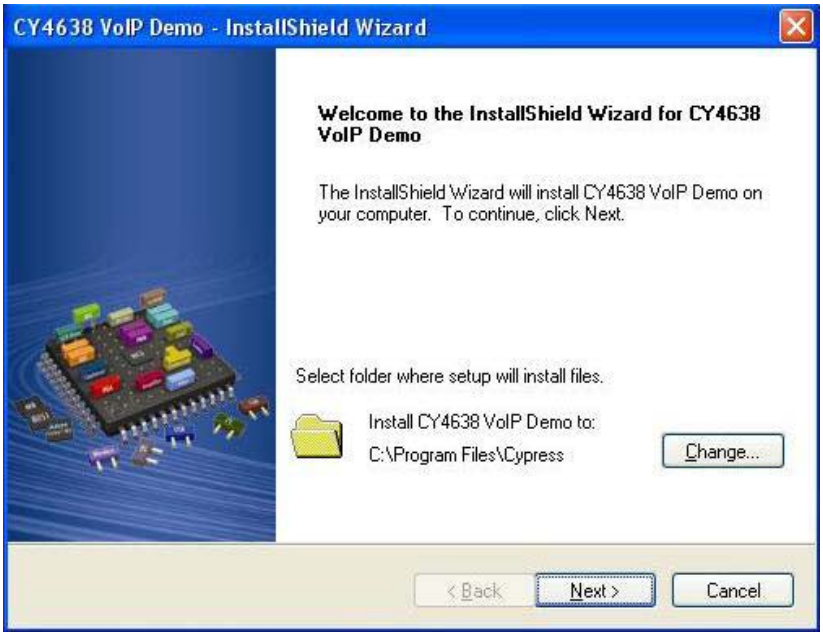
Note If auto-run does not execute, double-click the *cyautorun.exe* file on the root directory of the CD/DVD, as shown in Figure 2-2.

Figure 2-2. Root Directory of CD/DVD



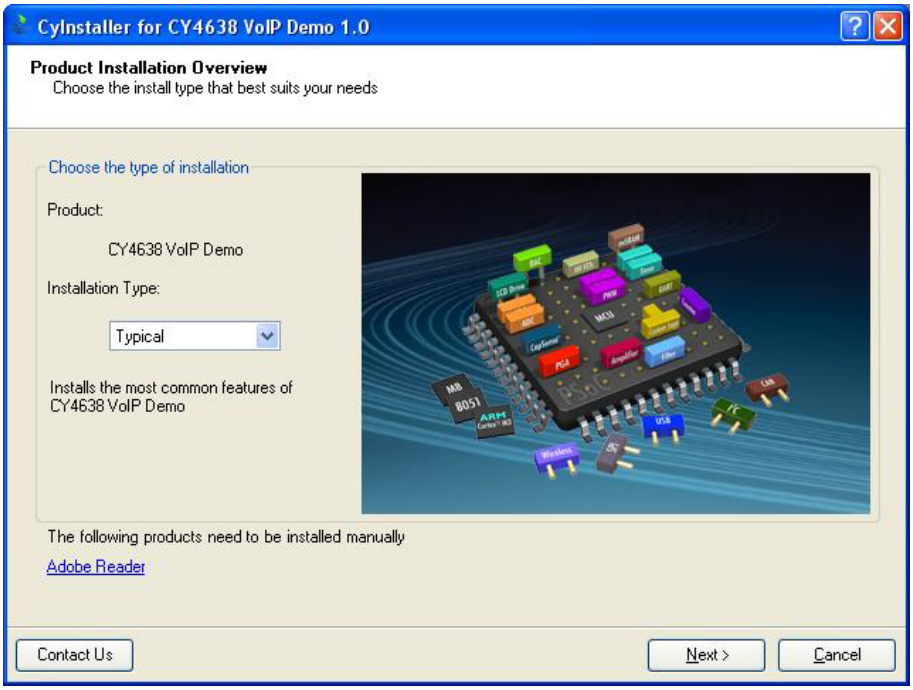
3. On the startup screen, click **Next** to start the installer.
4. The InstallShield Wizard appears. The default location for setup is shown on the InstallShield Wizard screen. You can change the location for setup using **Change**, as shown in Figure 2-3.
5. Click **Next** to launch the kit installer.

Figure 2-3. InstallShield Wizard



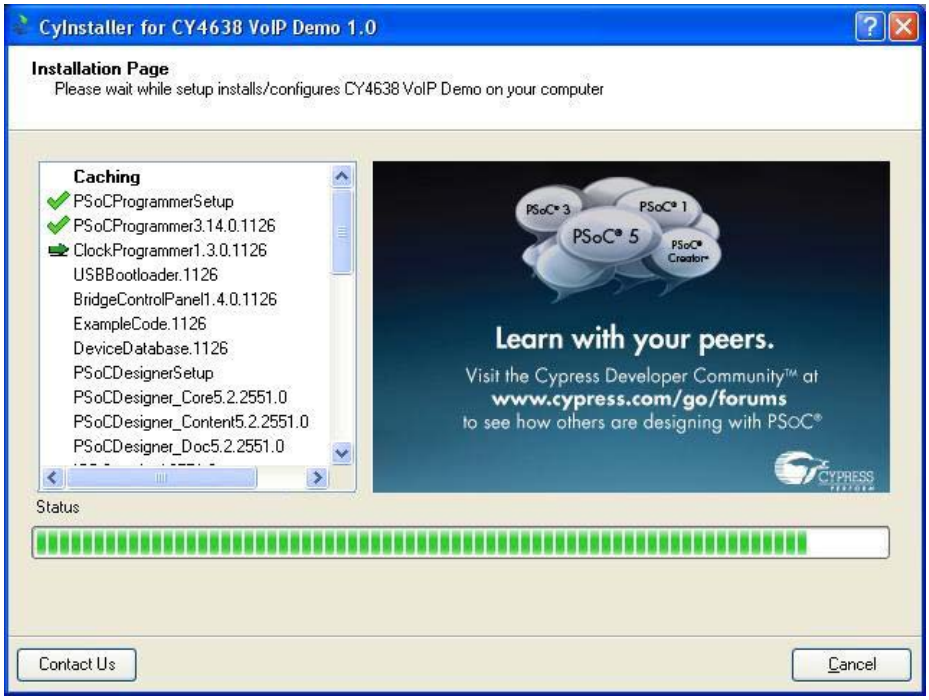
6. On the Product Installation Overview screen, select the installation type that best suits your requirement. The drop-down menu has three options - **Typical**, **Complete**, and **Custom**, as shown in Figure 2-4.
7. Click **Next** to start the installation.

Figure 2-4. Installation Type Options



8. When the installation begins, a list of all packages appears on the Installation Page. A green check mark appears adjacent to every package that is downloaded and installed.
9. Wait until all the packages are downloaded and installed successfully.

Figure 2-5. Installation Page



10. Click **Finish** to complete the installation, as shown in Figure 2-6.

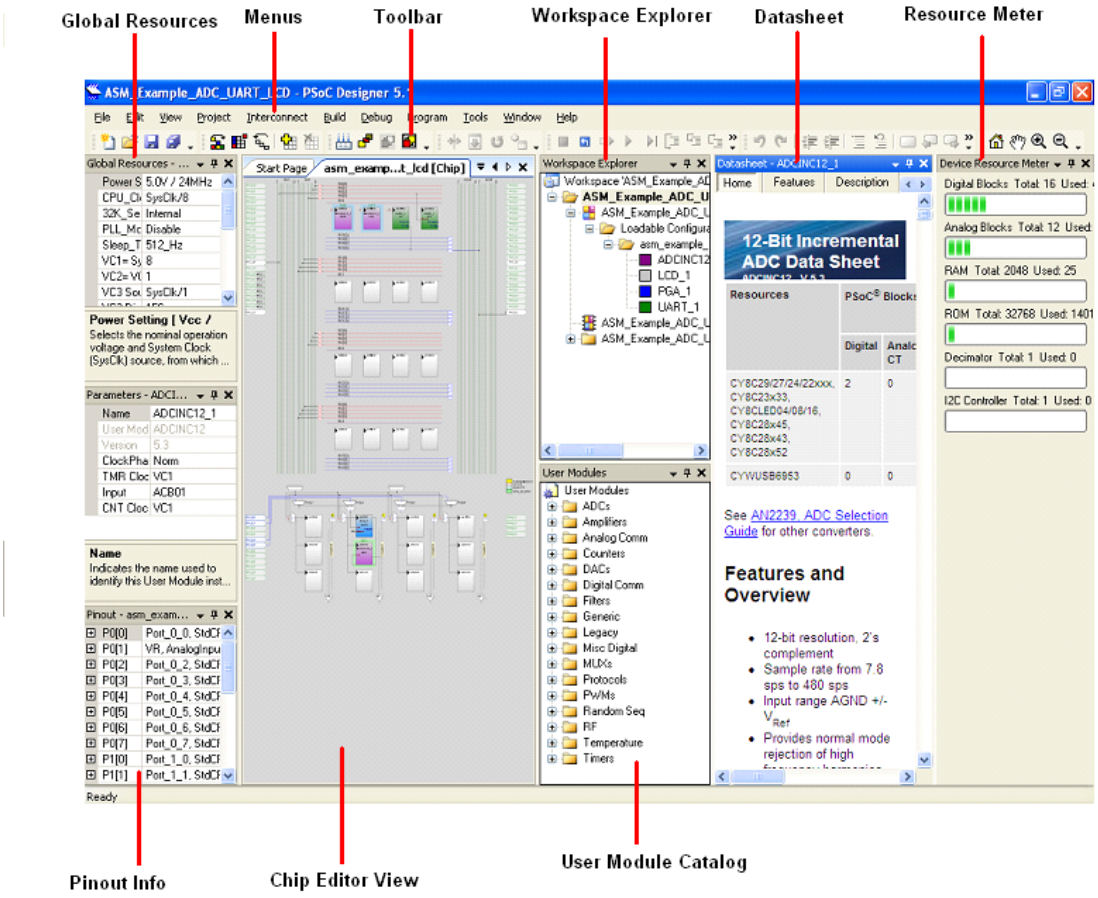
Figure 2-6. Installation Completion Page

Note After software installation, verify your installation and setup.

2.2 PSoC Designer

1. Click **Start > All Programs > Cypress > PSoC Designer <version> > PSoC Designer <version>**.
2. Click **File > New Project** to create new project; click **File > Open Project/Workspace** to work with an existing project.

   Figure 2-7. PSoC Designer Interconnect View



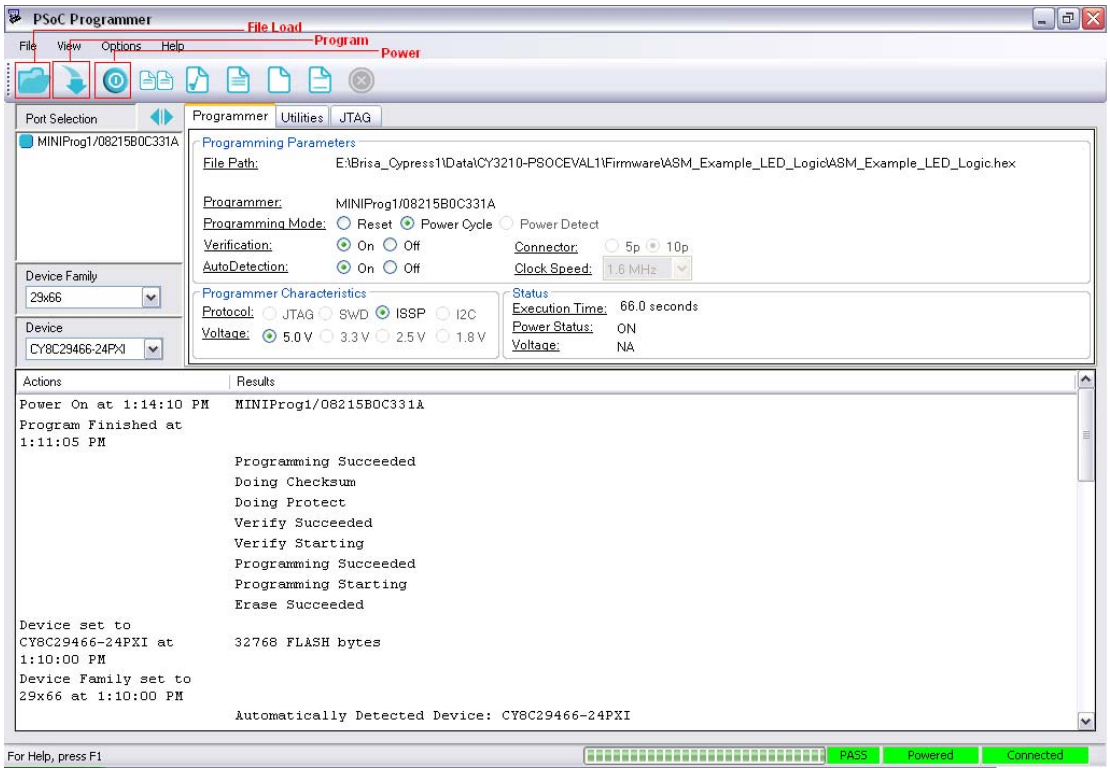
3. To experiment with the code examples, go to Code Examples on page 37.

Note For more details on PSoC Designer, see the PSoC Designer IDE Guide at: `<Install_Directory>:\Cypress\PSoC Designer\<version>\Documentation`.

2.3 PSoC Programmer

1. Click **Start > All Programs > Cypress > PSoC Programmer <version> > PSoC Programmer <version>**.
2. Select the MiniProg from **Port Selection**, as shown in Figure 2-8.

Figure 2-8. PSoC Programmer Window



3. Click the **File Load** button from the PSoC Programmer menu bar; navigate and select the appropriate hex file.
4. Use the **Program** button to load the hex file on to the chip.
5. When programming is successful, **Programming Succeeded** appears in the Actions pane.
6. Close PSoC Programmer.

Note For more details on PSoC Programmer, see the user guide at: `<Install_Directory>:\Cypress\Programmer\<version>\Documents`.

2.4 Install Hardware

No hardware installation required for this kit.

3. Kit Operation

The CY4638 WirelessUSB LP VoIP Demo Kit solution includes the following:

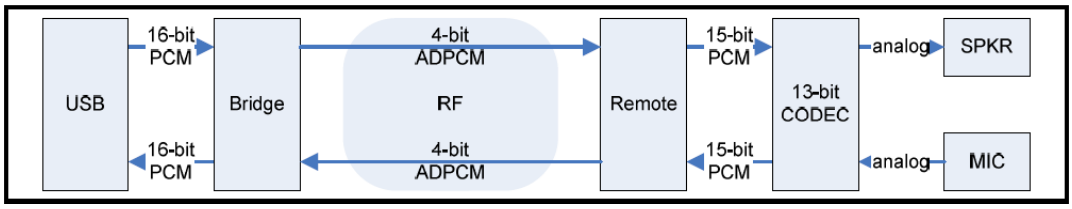
- WirelessUSB Full-Speed USB Bridge - This is a simple and small form factor bridge. It uses WirelesUSB LP (CYRF6936) and enCoRe III (CY7C64215) USB flash MCU.
- WirelessUSB Headset Board - This is an innovative dual antenna design for range and robustness. It uses WirelessUSB LP (CYRF6936), Wireless enCoRe III (CY7C60323) flash MCU, and Winbond (W681360) 3-V single-channel codec.

3.1 Packet Structure

3.1.1 Audio Considerations

The USB PCM rate is 8 Ksps and each PCM sample is 16 bits. This is 128 Kbps in each direction or a total of 256 Kbps for mono audio. Compressing the 16-bit samples with ADPCM yields a 4-bit sample stream (at the same sample rate), reducing the total from 256 Kbps to 64 Kbps.

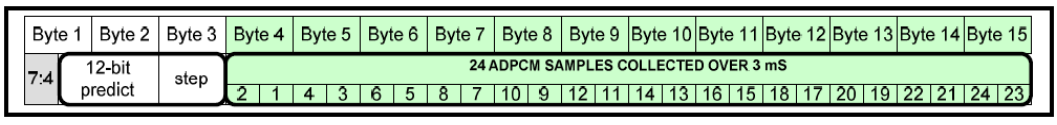
Figure 3-1. Audio Path



3.1.2 Radio Considerations

The raw RF rate is 250 Kbps. Allowing for ~50 percent overhead, it yields about 128 Kbps to contain the 64 Kbps audio stream. Figure 3-2 shows a 15-byte radio packet that contains 24 samples of ADPCM audio. These 24 samples contain 3 ms of audio (24 samples/8 Ksps = 3 ms). The 8-bit Step and 12-bit Predict values are discussed in ADPCM on page 16. The first four bits in the grayed-out area are available for future use.

Figure 3-2. VoIP Packet Structure



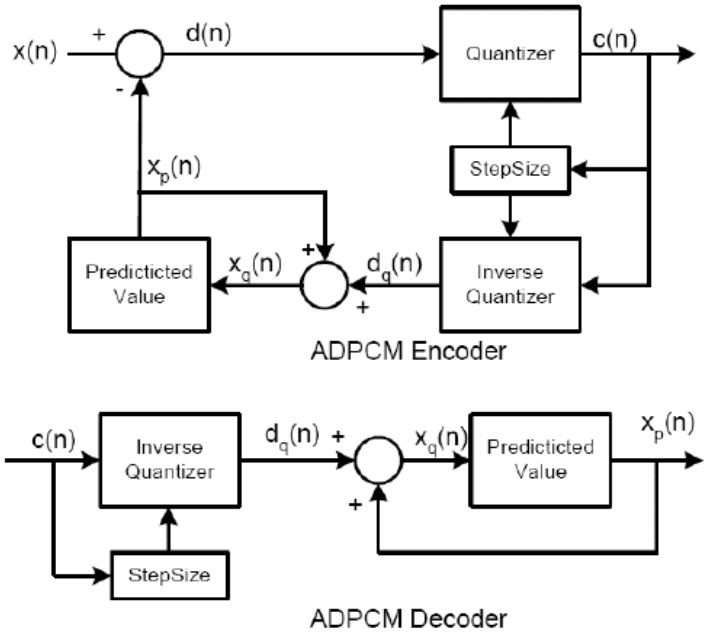
Because audio is latency sensitive, the standard "Transaction Acks" available from the CYRF6936 radio are not used. Retransmitting an audio packet introduces variable latency and the radio's Transaction Ack increases the RF channel usage.

Although the USB PCM is 16 bits, it is truncated to 15 bits before ADPCM encoding to simplify implementation. Also, the Winbond codec interfaced to the speaker and microphone is only 13 bits and is shifted to convert to 15 bits at ADPCM encode/decode. Such manipulations do not typically result in noticeable speech degradation.

3.1.3 ADPCM

ADPCM takes advantage of high correlation between consecutive speech samples, enabling future sample values to be predicted. Instead of encoding the speech sample, ADPCM encodes the difference between a predicted sample and the speech sample. This provides efficient compression, yet preserves the overall speech quality. This ADPCM algorithm is based on the Interactive Multimedia Association's (IMA) *Recommended Practices for Enhancing Digital Audio Compatibility in Multimedia Systems*, revision 3.00. The ITU (formerly CCITT) G.721 ADPCM algorithm is well known and uses floating-point arithmetic and logarithmic functions. This is not an approach that works for an embedded processor. The IMA reference algorithm significantly reduces mathematical complexity of ITU G.721 by simplifying many of the operations and using table lookups where appropriate. Many examples of such implementations are available on the Internet; all compress 16-bit data to four bits.

Figure 3-3. ADPCM Block Diagram



The encoder takes the difference of input and the predicted value. This difference value is compressed to four bits. It is a function of the input and step size. This compressed value is then decompressed using a function that is approximately the inverse of the compressor. Ideally d(n) should equal dq(n). This quantized difference value is added to the old predicted value to generate the next predicted value. This new predicted value equals the original input. Xp(n) is the decoded value. The sections dealing with the decode process are duplicated on the receive side. If the receive side has the same step size and predicted value, then the Xp(n) calculated on the transmit side is the same as the one calculated on the receive side. The step size is increased or decreased as a function of the 4-bit compression value.

3.1.3.1 ADPCM Step and Predict Values

By the nature of ADPCM compression, the encoder remembers and updates its step-size and also its prediction value. The decoder tracks these values based only on the 4-bit ADPCM sample

stream. As long as there are no ADPCM data samples lost, the ADPCM encoder and decoder always contains identical step and predict values. For example, the step and predict values just before Sample 10 is encoded is identical to the step and predict values just before Sample 10 is decoded by the decoder.

However, the RF communication channel is subject to loss, so the step and predict values at the decoder cannot always track those at the encoder without the ability to be manually synchronized. With the 3-ms "packets", it is convenient to attach the beginning step and predict values for each packet. This enables stand-alone decoding of each 3-ms voice packet, regardless of whether prior packet(s) are decoded. The disruption of one packet is confined to a 3-ms event and does not ripple beyond 3 ms.

3.1.4 Radio Channel and Multipath Fading

The RF channel can have multipath fading similar to constructive and destructive waves of water. If only one antenna path is available, it is easy to place these two antennas in such a multipath null. Move either the bridge or remote antenna 3 cm and the signal is good again. For bursty wireless applications such as keyboard, mouse, and keyfob, multipath is not a problem. A keyboard or mouse is usually within a few feet of the bridge, rarely in the adjacent room. Users do not notice 10 ms or 20 ms delay, so messages can be retried many times if needed. Users expect to move a keyfob and push the key again if it occasionally does not work the first time.

However, audio is different; you listen to the radio link quality constantly while sometimes stationary and sometimes moving around 10 meters from your PC. Nulls becomes obvious interruptions in the audio stream.

To mitigate multipath nulls, the RF path (or the environment) must change. A second antenna at the remote (although it can be moved to the bridge) is implemented in this kit. Because the ~128 Kbps channel can contain a redundant copy of the 64 Kbps voice stream, you can send one packet using Remote Antenna A and the duplicate packet using Remote Antenna B. This provides the far side (bridge) two different RF paths.

Similarly, the bridge can send two copies of the same packet and the far side (remote) can use Remote Antenna A to receive the first packet and switch to Remote Antenna B to receive the duplicate packet. In this way, both paths must be in a multipath null to lose packet(s). This happens, but is much less frequent than if only a single antenna path is used.

Figure 3-4. Packet Slotting Over 3-ms Audio Set

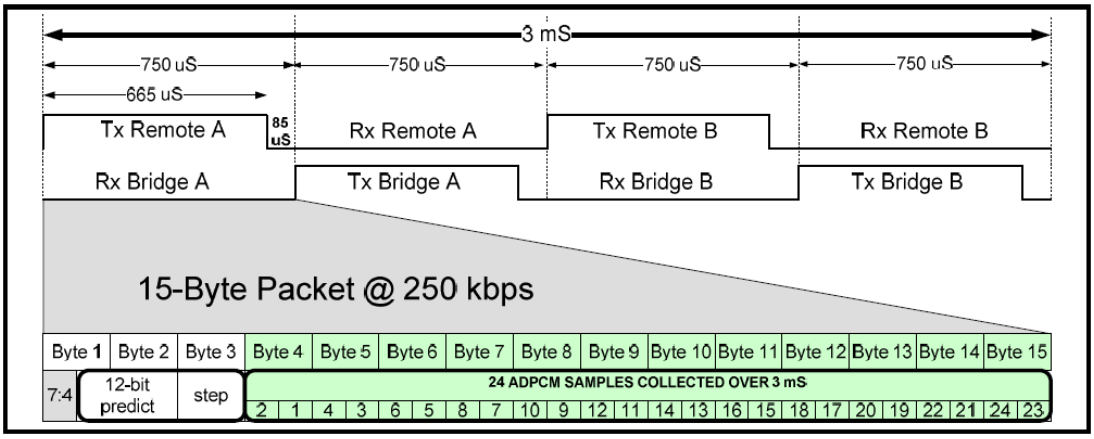


Figure 3-4 shows that four packets (each containing 3 ms of audio) can be sent over the RF link every 3 ms. The remote sends two copies of the packet and the bridge sends two copies of the same

packet. The receiving device needs only one packet to successfully arrive. The resulting RF channel occupancy is about 89 percent duty cycle (RF power for 665 µs every 750 µs).

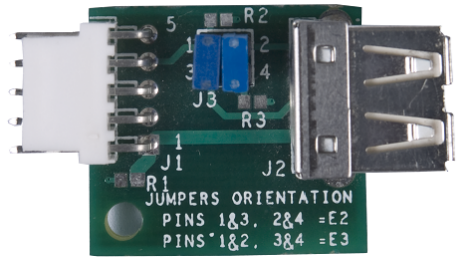
3.1.5 Bluetooth Hopper Interference

Bluetooth hoppers last less than 750 µs. Figure 3-3 shows that each audio packet copy is spaced by 750 µs and the Bluetooth interferer cannot collide with both copies.

3.2 WirelessUSB Full-Speed USB Bridge

The WirelessUSB Full-Speed USB bridge can be programmed through the USB connector using a Cypress USB adapter board CY3655-PLG.

Figure 3-5. Cypress USB Programming Adapter



1. Connect the bridge to the USB adapter board.
2. Connect the MiniProg to the ISSP header on the USB adapter, as shown in Figure 3-6.
3. Connect the MiniProg to the PC through USB A to Mini B cable.
4. On the USB adapter, place two jumpers between pins 1 and 2 and pins 3 and 4.

To program the hex file on to the bridge using the MiniProg:

1. Open PSoC Programmer and select the MiniProg from **Port Selection**.
2. Click **Program**. While programming is in progress, the target power LED on the MiniProg is on.

Figure 3-6. Programming the Bridge

3. When **Programming Succeeded** appears in the Actions pane, detach the MiniProg.
4. Connect the bridge dongle through the USB port to the PC, wait for the bridge to enumerate.

The bridge enumerates as a USB audio device (PID 0x04B4, VID 0x4B55) using 8 Ksps 16-bit PCM. The standard Windows XP driver works. Currently there are no audio level adjustments available via USB. The green LED blinks when connected to the remote handset. The red LED indicates USB-out traffic from the PC.

3.3 WirelessUSB Headset Board

J1 is a programming header. The PSoC MiniProg is used to program the remote microcontroller using this ISSP header. Connect your computer to the ISSP header on the remote using the Mini-Prog and a USB cable (A to Mini B). You can program using the PSoC Programmer software.

To program the hex file on to the remote using the MiniProg:

1. Open PSoC Programmer and select the MiniProg from **Port Selection**.
2. Click **Program**. While programming is in progress, the target power LED on the MiniProg is on.

Figure 3-7. Programming Remote

3. When **Programming Succeeded** appears in the Actions pane, detach the MiniProg.

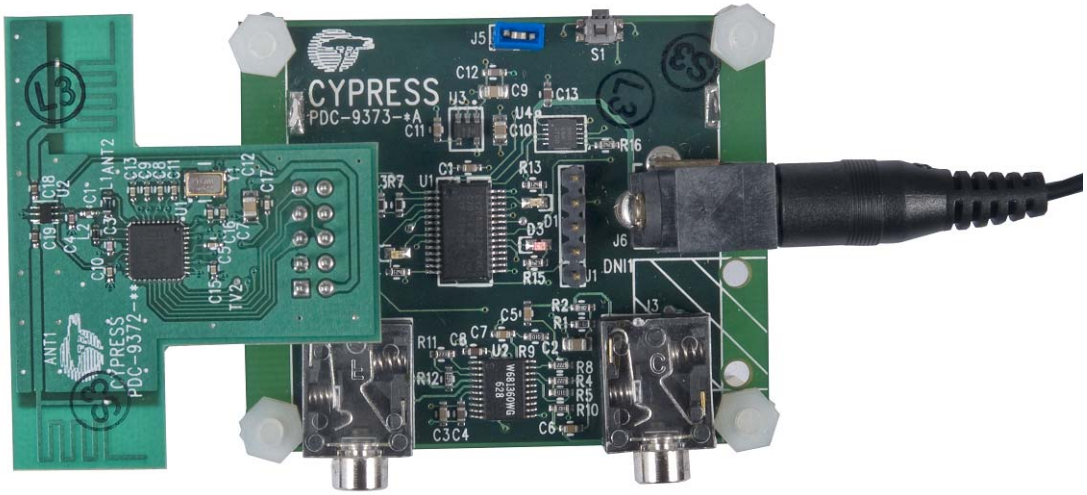
The Li-Ion battery is attached when jumper J5 is installed. During VoIP operation, the green LED blinks. The radio transmits and receives, and the bridge can synchronize to the remote stream. The remote draws about 35 mA in this mode and the Li-Ion battery capacity is 350 mAh; this results in about eight hours "talk time". The yellow LED begins blinking when the battery voltage falls to 3.65 V and the red LED when the voltage falls to 3.45 V. When the battery falls to 3.15 V, only the red LED blinks and the unit hibernates to avoid over-discharge of the Li-Ion battery. Currently there is no "standby mode".

3.4 Charging

With the battery jumper installed, attach the wall-wart charger (5VDC on the center pin). The green and yellow LEDs should blink. The battery is charged in about an hour; when fully charged, only the green LED blinks. When charged, unplug the charger and remove the jumper to power down the remote. Power-cycle the remote before it begins VoIP operation.

Note Although the remote knows when the charger is initially inserted, it does not know when you remove the charger.

Figure 3-8. Charge Battery



3.5 Channel Operation

Either the remote or base may initiate a channel change using a fast and slow trigger derived from packet error rate. The fast trigger changes channels within 50 ms of nearly complete signal loss, while the slow trigger changes channels within 2 seconds of coherent, but "scratchy" audio.

The S1 switch on the remote manually changes channels. There are 26 channels available, spaced 3 MHz apart. Currently, no exclusive and unique "binding" is implemented between a bridge and a remote. Any bridge can communicate with any remote.

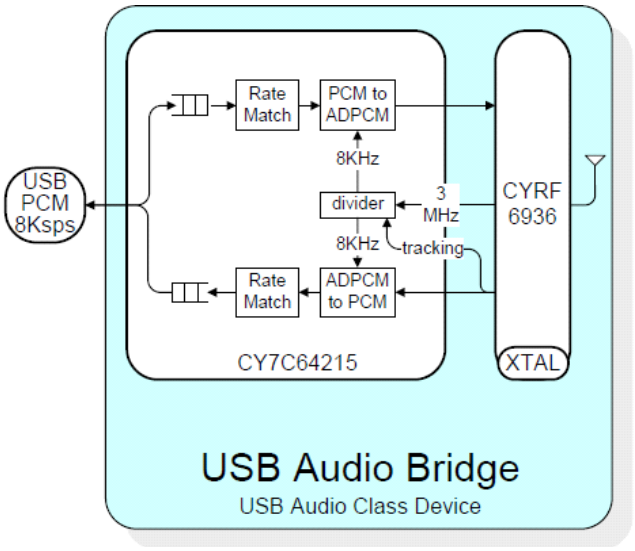
4. Hardware

4.1 WirelessUSB Full-Speed USB Bridge

WirelessUSB Full-Speed USB Bridge is a simple and small form-factor bridge. It uses WirelesUSB LP (CYRF6936) and enCoRe III (CY7C64215) USB flash MCU.

The CYRF6936 radio provides a 3 MHz clock to the CY7C64215 processor. This is divided by 375 using a 16-bit counter (actually a PWM16 module, but it is used as a 16-bit counter) to generate the 8-kHz interrupt time base. The 8-kHz interrupt drives radio communication stream.

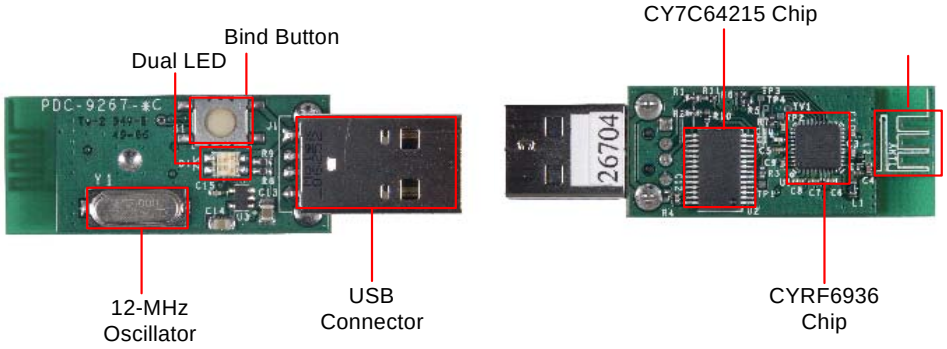
Figure 4-1. Bridge Block Diagram



4.1.1 Functional Description

The following figure shows the different functional blocks on the CY4638 bridge dongle.

Figure 4-2. Bridge Board Functional Blocks



4.1.1.1 CYRF6936 Chip

The CYRF6936 WirelessUSB LP radio is a second generation member of the Cypress WirelessUSB Radio System-On-Chip (SoC) family. The CYRF6936 is interoperable with the first generation CYWUSB69xx devices. The CYRF6936 IC adds a range of enhanced features, including increased operating voltage range, reduced supply current in all operating modes, higher data rate options, reduced crystal start up, synthesizer setting, and link turnaround times.

The CYRF6936 chip operates with a 2.4 GHz Direct Sequence Spread Spectrum (DSSS) radio transceiver; it operates in the unlicensed worldwide Industrial, Scientific, and Medical (ISM) band (2.400 GHz to 2.483 GHz). The operating current is 21 mA (transmit at –5 dBm). The transmit power is up to +4 dBm and has a receive sensitivity of up to –97 dBm.

The CYRF6936 chip is targeted towards the following applications:

- Wireless keyboards and mice
- Wireless gamepads
- Remote controls
- Toys
- VOIP and wireless headsets
- White goods
- Consumer electronics
- Home automation
- Automatic meter readers
- Personal health and entertainment

Figure 4-3. Schematic View of CYRF6936 Chip

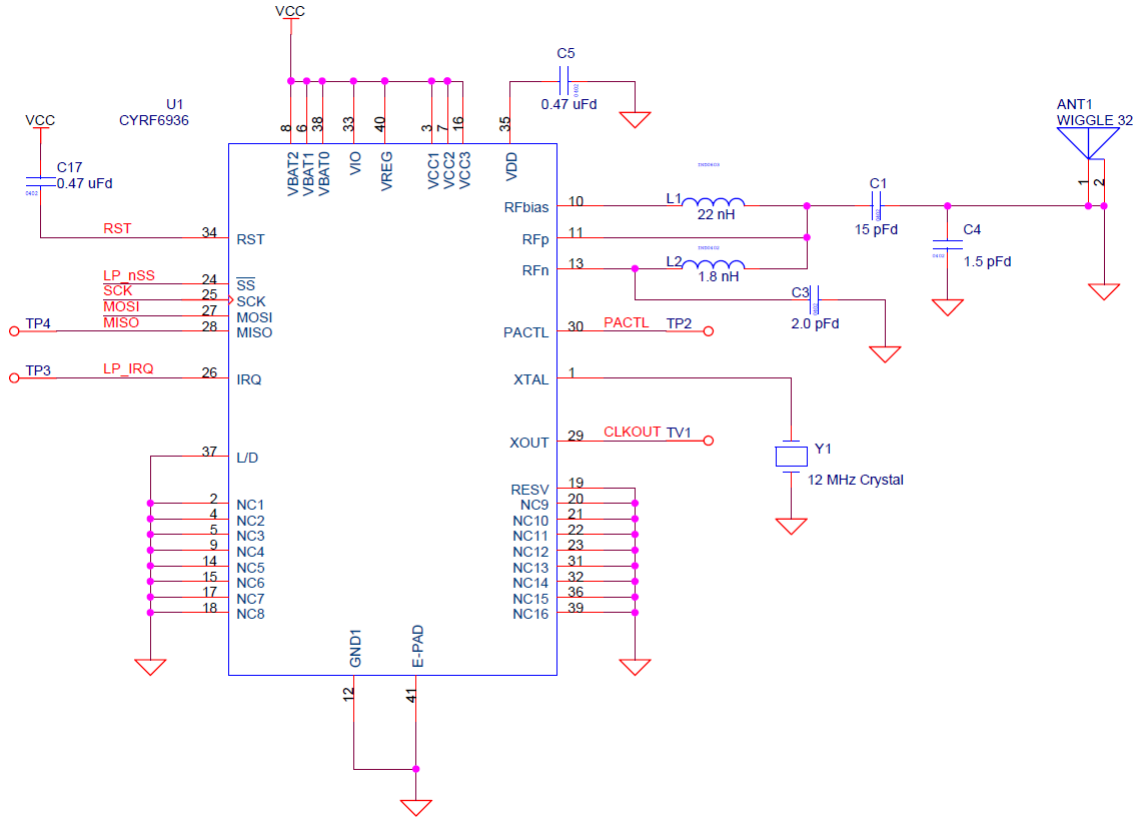


Table 4-1. Pin Details of CYRF6936 Chip

Pin	Name	Description
1	XTAL	12-MHz crystal
2	NC	Connect to GND
3	VCC	VCC = 2.4 V to 3.6 V. Typically connected to VREG
4	NC	Connect to GND
5	NC	Connect to GND
6	VBAT(0-2)	VBAT = 1.8 V to 3.6 V. Main supply
7	VCC	VCC = 2.4 V to 3.6 V. Typically connected to VREG
8	VBAT(0-2)	VBAT = 1.8 V to 3.6 V. Main supply
9	NC	Connect to GND
10	RFBIAS	RF I/O 1.8 V reference voltage
11	RFP	Differential RF signal to and from antenna
12	GND	Ground
13	RFN	Differential RF signal to and from antenna
14	NC	Connect to GND
15	NC	Connect to GND
16	VCC	VCC = 2.4 V to 3.6 V. Typically connected to VREG
17	NC	Connect to GND
18	NC	Connect to GND

Table 4-1. Pin Details of CYRF6936 Chip

Pin	Name	Description
19	RESV	Must be connected to GND
20	NC	Connect to GND
21	NC	Connect to GND
22	NC	Connect to GND
23	NC	Connect to GND
24	SS	SPI enable, active LOW assertion. Enables and frames transfers
25	SCK	SPI clock
26	IRQ	Interrupt output (configurable active HIGH or LOW), or GPIO (general purpose I/O)
27	MOSI	SPI data input pin (Master Out Slave In), or SDAT
28	MISO	SPI data output pin (Master In Slave Out), or GPIO (in SPI 3-pin mode). Tri-states when SPI 3PIN = 0 and SS is deasserted
29	XOUT	Buffered 0.75, 1.5, 3, 6, or 12 MHz clock, PACTL, or GPIO.Tri-states in sleep mode (configure as GPIO drive LOW)
30	PACTL	Control signal for external PA, T/R switch, or GPIO
31	NC	Connect to GND
32	NC	Connect to GND
33	VIO	I/O interface voltage, 1.8 V to 3.6 V
34	RST	Device reset. Internal 10 kohm pull down resistor. Active HIGH, connect through a 0.47 µF capacitor to VBAT. Must have RST = 1 event the first time power is applied to the radio. Otherwise, the state of the radio control registers is unknown
35	VDD	Decoupling pin for 1.8 V logic regulator, connect through a 0.47 µF capacitor to GND
36	NC	Connect to GND
37	L/D	PMU inductor/diode connection, when used. If not used, connect to GND
38	VBAT(0-2)	VBAT = 1.8 V to 3.6 V. Main supply
39	NC	Connect to GND
40	VREG	PMU boosted output voltage feedback

4.1.1.2 CY7C64215 Chip

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12 Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer and communication applications. This architecture enables to create customized peripheral configurations that match the requirements of individual applications.

The CY7C64215 is targeted at the following applications:

PC human interface devices

- Mouse (optomechanical, optical, trackball)
- Keyboards
- Joysticks

Gaming

- Game pads
- Console keyboards

General purpose

- Barcode scanners
- POS terminal
- Consumer electronics
- Toys
- Remote controls
- USB to serial

Figure 4-4. Schematic View of CY7C64215 Chip

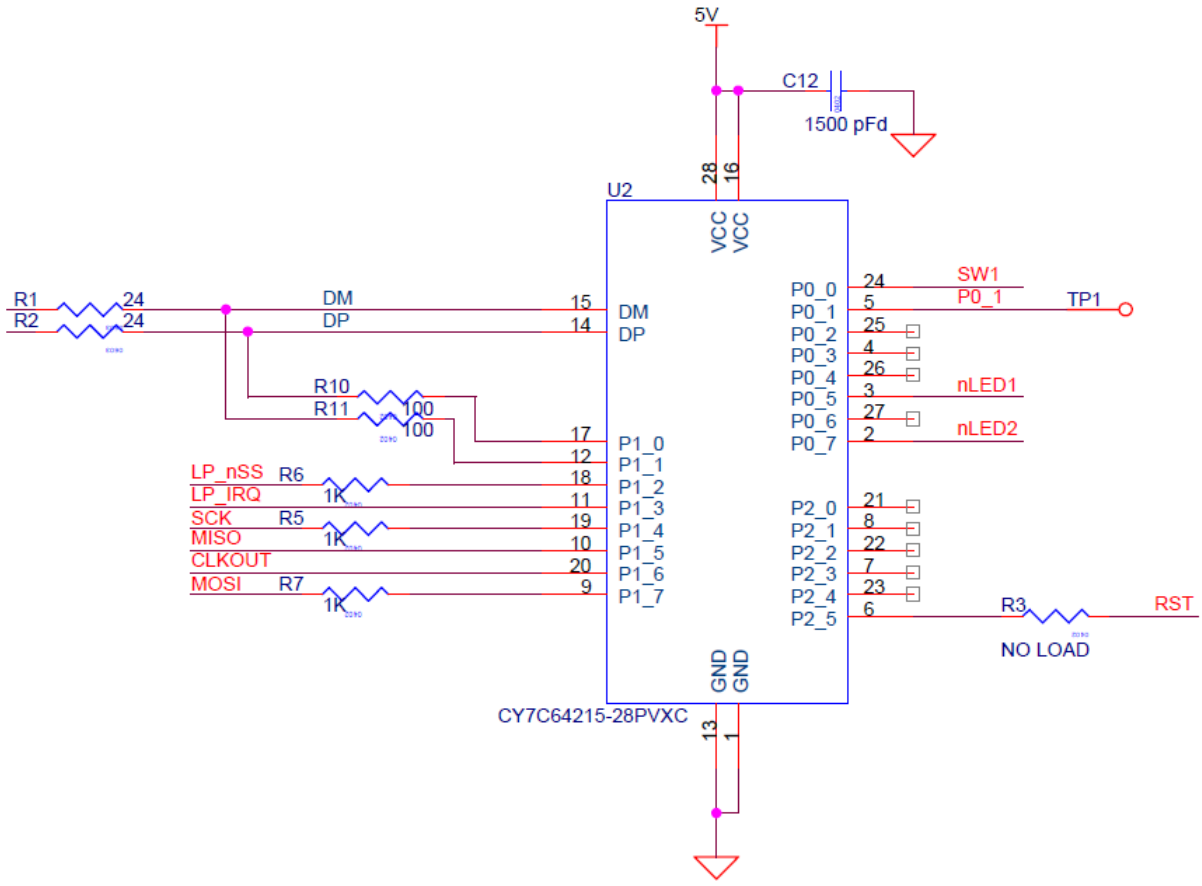


Table 4-2. Pin Details of CY7C64215 Chip

Pin	Name	Description
1	GND	Ground connection
2	P0.7	Analog column mux input
3	P0.5	Analog column mux input and column output
4	P0.3	Analog column mux input and column output
5	P0.1	Analog column mux input
6	P2.5	
7	P2.3	Direct switched capacitor block input
8	P2.1	Direct switched capacitor block input
9	P1.7	I2C SCL

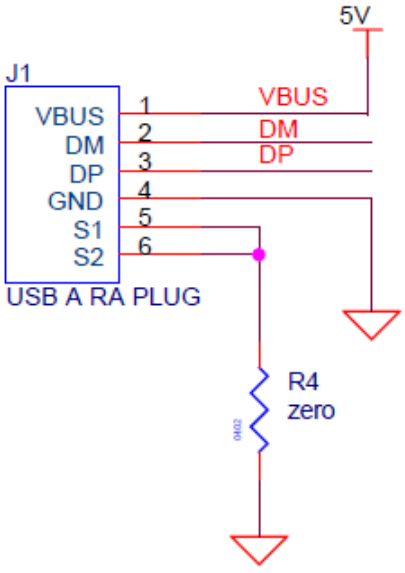
Table 4-2. Pin Details of CY7C64215 Chip

Pin	Name	Description
10	P1.5	I2C SDA
11	P1.3	
12	P1.1	I2C SCL, ISSP-SCLK
13	GND	Ground connection
14	D+	USB DP
15	D-	USB DM
16	VDD	Supply voltage
17	P1.0	I2C SCL, ISSP-SDATA
18	P1.2	
19	P1.4	
20	P1.6	
21	P2.0	Direct switched capacitor block input
22	P2.2	Direct switched capacitor block input
23	P2.4	External analog ground (AGND) input
24	P0.0	Analog column mux input
25	P0.2	Analog column mux input and column output
26	P0.4	Analog column mux input and column output
27	P0.6	Analog column mux input
28	VDD	Supply voltage

4.1.1.3 *USB A Connector*

The USB A connector communicates between the PC and bridge; it also supplies an input voltage of 5 V to power up the bridge.

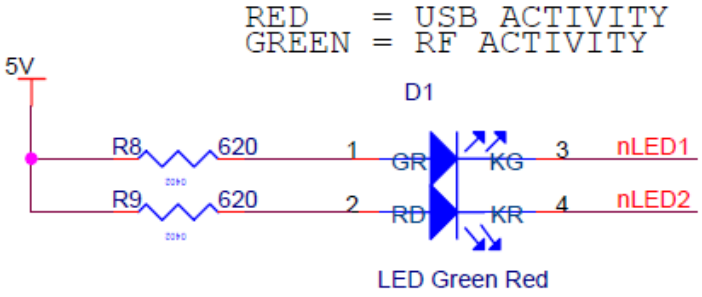
Figure 4-5. Schematic View of USB A Connector



4.1.1.4 LEDs

The CY4638 bridge board has dual LED to indicate different status. The green LED blinks when connected to the remote handset. The red LED indicates USB-out traffic from the PC.

Figure 4-6. Schematic View of LEDs



4.1.2 Power Supply System

The CY4638 bridge board is supplied power from the USB A connector on the board.

Figure 4-7. Power Supply System Structure for Bridge

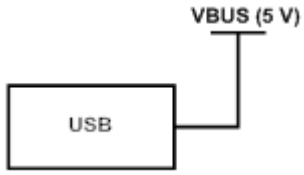
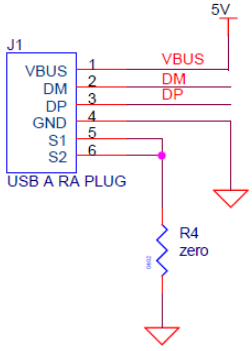


Figure 4-8. Schematic View of Bridge Power Supply System



4.2 WirelessUSB Headset Board

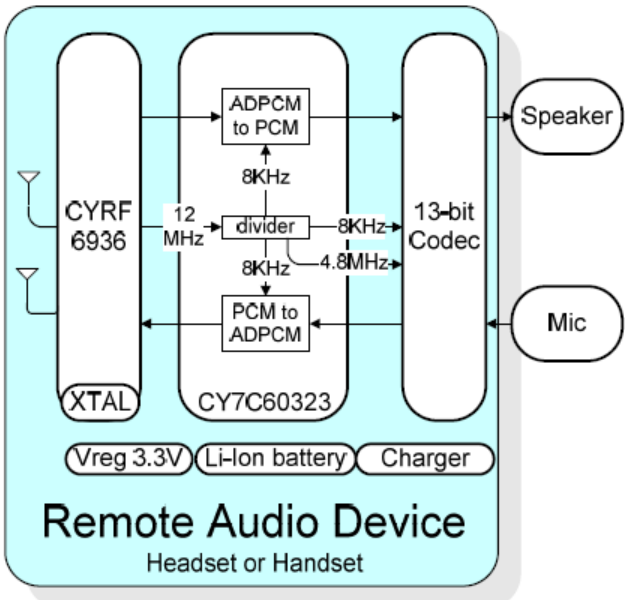
The CYRF6936 radio provides a 12-MHz clock to the CY7C60323 processor. This is the 12-MHz CPU SyClk and is doubled (SysClkx2) to 24 MHz in the PSoC. The 24 MHz is divided by 5 with a PWM8 module to give 4.8 MHz Master Clock (MCLK) to the Winbond codec.

The 12-MHz SysClk is divided by 6 in VC3 to 2 MHz and divided by 250 in a PWM8 to give 8 kHz for both an interrupt and the Winbond codec Frame Sync (FS) signal.

The SPI interface (to both the radio and codec) is 3 MHz using VC1 to divide SysClk by 2. Similar to the bridge, the 8-kHz interrupt drives radio communication stream.

The remote codec samples at nominally 8 Ksps based on its local clock, while the PC samples at nominally 8 Ksps based on its local clock. The combined error between these clocks results in a few samples per second drift. Rate matching inserts or deletes samples to maintain a steady buffer level.

Figure 4-9. Remote Block Diagram



4.2.1 Functional Description

The WirelessUSB LP headset board includes a Cypress Wireless enCoRe III flash microcontroller, a low-power Winbond codec, and a rechargeable battery with the radio module.

Figure 4-10. Functional Blocks of Remote

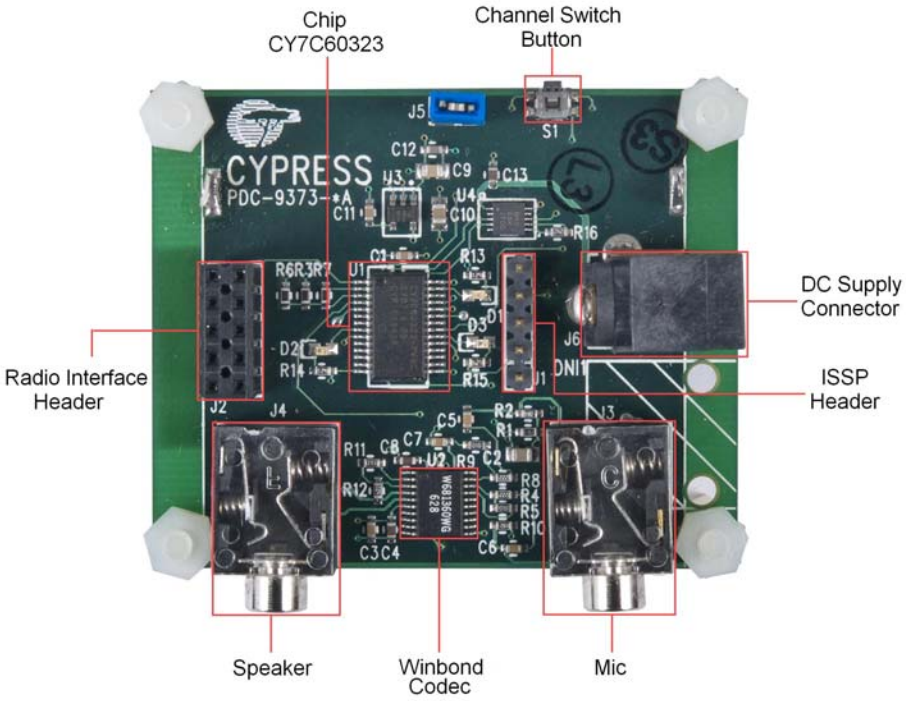
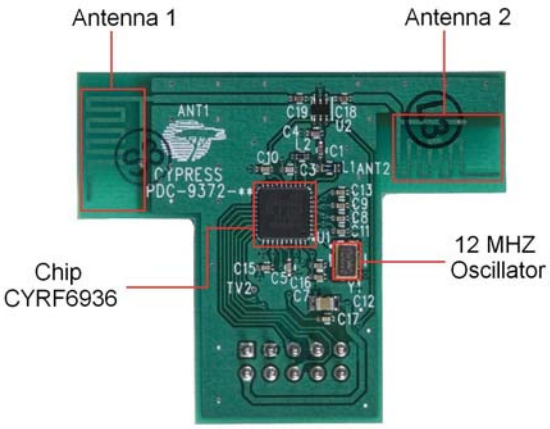


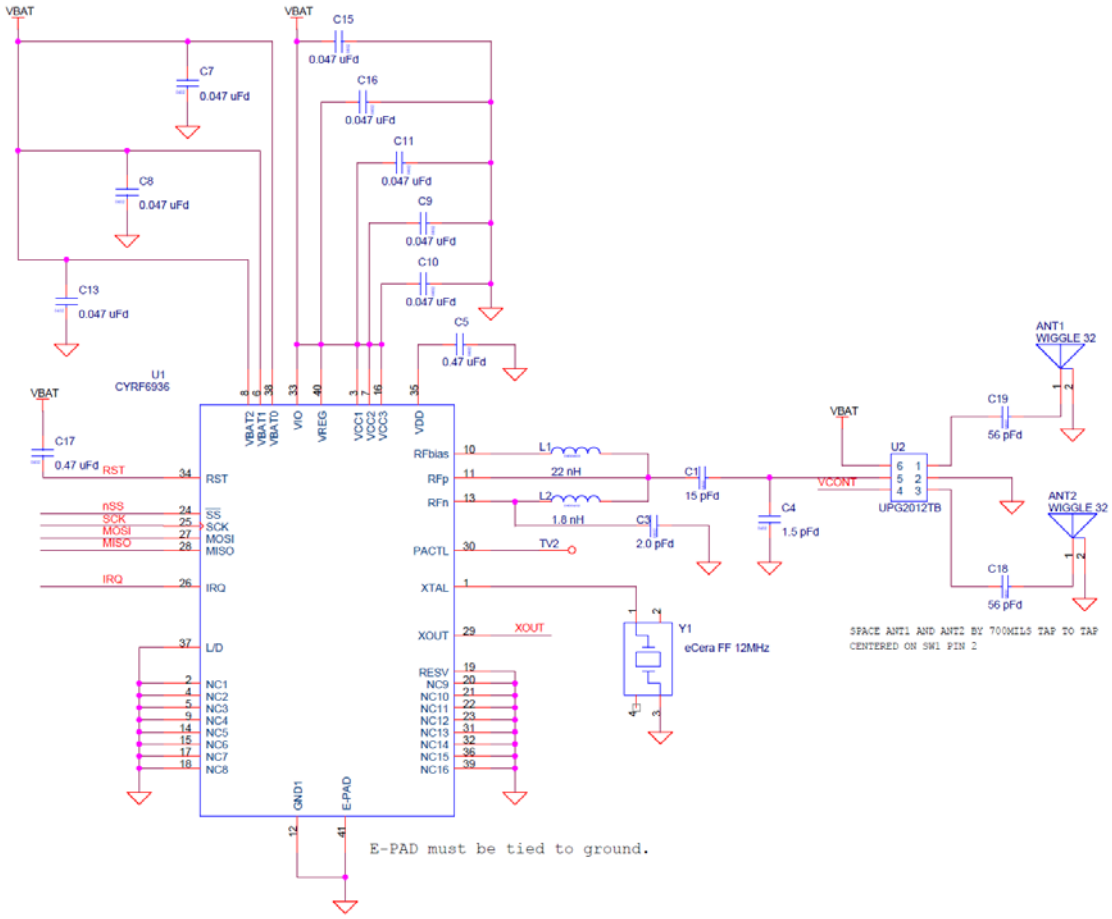
Figure 4-11. Functional Blocks of Radio Board



4.2.1.1 *CYRF6936 Chip*

The radio transmitter board uses the CYRF6936 chip for radio transmission; two antennas are provided for headset with antenna diversity to maximize range and robustness.

Figure 4-12. Schematic View of CYRF6936 Chip



For pin details, see CYRF6936 Chip on page 22.

4.2.1.2 CY7C60323 Chip

The enCoRe III Low Voltage (LV) CY7C603xx device is based on the flexible PSoC architecture. A simple set of peripherals is supported that can be configured as required to match the needs of each application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included.

The enCoRe III LV core is a powerful engine that supports a rich feature set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO).

The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a four MIPS 8-bit Harvard architecture microprocessor. The core includes a CPU, memory, clocks, and configurable GPIO.

System resources provide additional capability, such as digital clocks to increase flexibility; I2C functionality to implement an I2C master, slave, multimaster; an internal voltage reference that provides an absolute value of 1.3 V to a number of subsystems; a switch mode pump (SMP) that generates normal operating voltages off a single battery cell; and various system resets supported by the M8C.

The CY7C60323 chip is targeted at the following applications:

- Wireless mice
- Wireless gamepads
- Wireless presenter tools
- Wireless keypads
- PlayStation 2 wired gamepads
- PlayStation 2 bridges for wireless gamepads
- Applications requiring a cost effective low voltage 8-bit microcontroller

Figure 4-13. Schematic View of CY7C60323 Chip

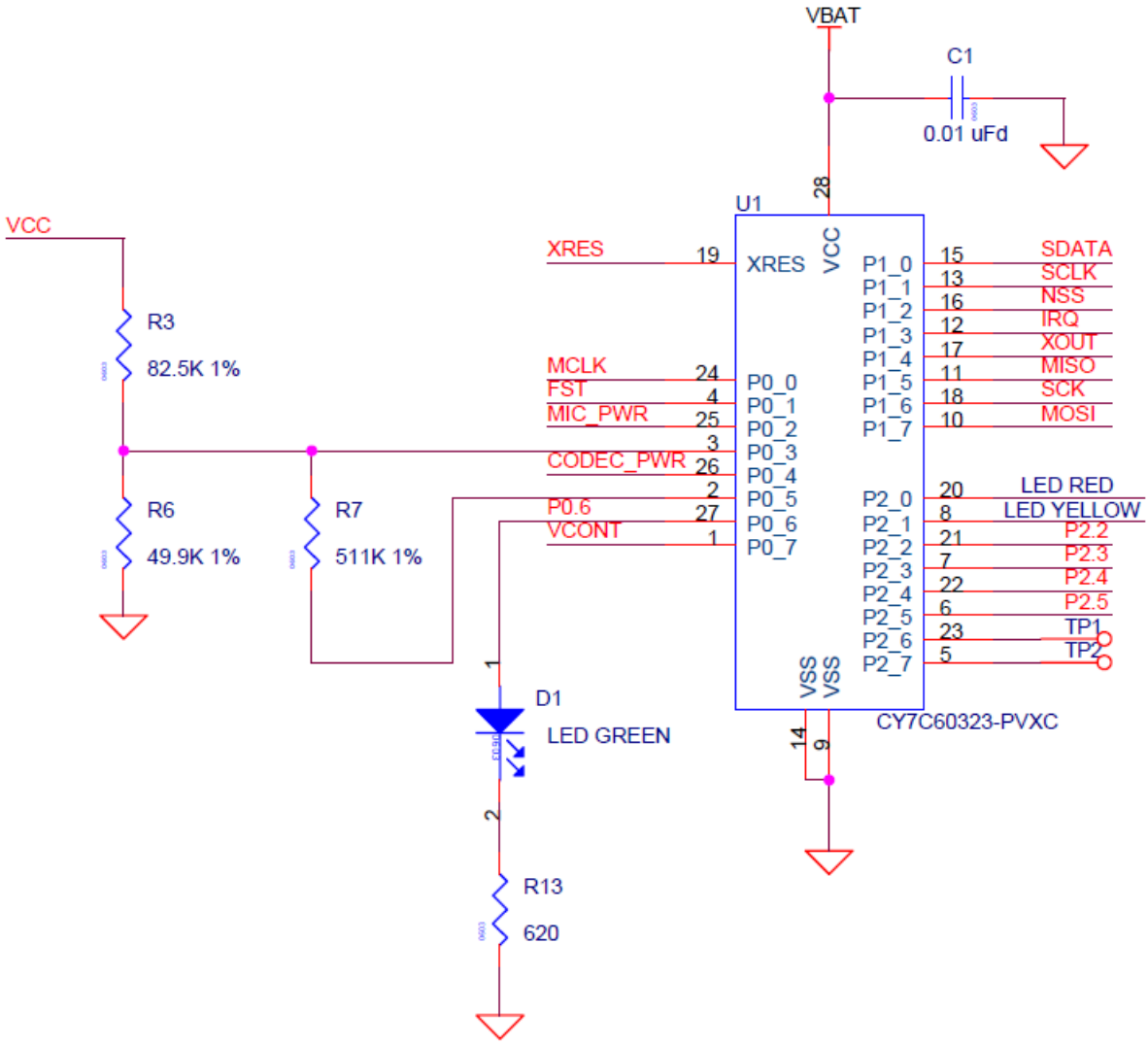


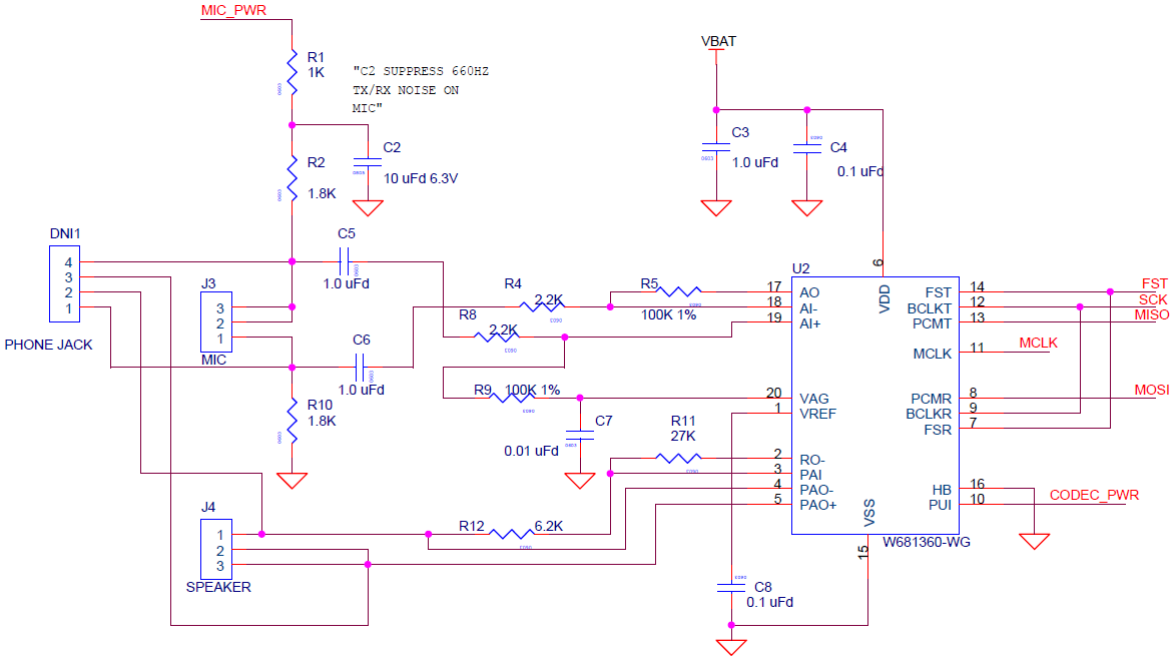
Table 4-3. Pin Details of CY7C60323 Chip

Pin	Name	Description
1	P0[7]	Analog column mux input
2	P0[5]	Analog column mux input and column output
3	P0[3]	Analog column mux input and column output, integrating input
4	P0[1]	Analog column mux input, integrating input
5	P2[7]	Test point 2
6	P2[5]	
7	P2[3]	Direct switched capacitor block input
8	P2[1]	Direct switched capacitor block input
9	Vss	Ground connection
10	P1[7]	I2C Serial Clock (SCL)
11	P1[5]	I2C Serial Data (SDA)
12	P1[3]	IRQ
13	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK
14	Vss	Ground connection
15	P1[0]	I2C Serial Data (SDA), ISSP-SDATA
16	P1[2]	NSS
17	P1[4]	Optional External Clock Input (EXTCLK)
18	P1[6]	SCK
19	XRES	Active HIGH external reset with internal pull down
20	P2[0]	Direct switched capacitor block input
21	P2[2]	Direct switched capacitor block input
22	P2[4]	
23	P2[6]	Test point 1
24	P0[0]	Analog column mux input
25	P0[2]	Analog column mux input
26	P0[4]	Analog column mux input
27	P0[6]	Analog column mux input
28	Vdd	Supply voltage

4.2.1.3 Winbond Codec

Winbond's W681360 single-channel voice codec is a 13-bit linear analog-to-digital and digital-to-analog converter. The W681360 offers high performance voice quality at the lowest power consumption in the industry, directly impacting talk-time and battery life. Winbond codec is used to implement clean signal quality and production-ready, 2.4 GHz wireless VoIP headset system. The microphone and the speaker are connected via the terminals J3 and J4, respectively.

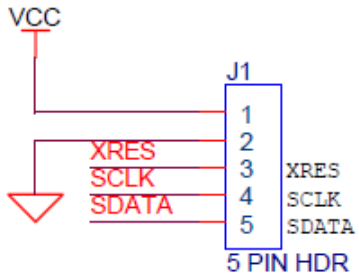
Figure 4-14. Schematic View of W681360 Codec



4.2.1.4 *ISSP Header*

In-system serial programmer (ISSP) is used to program the device. Programming can be done using the MiniProg device.

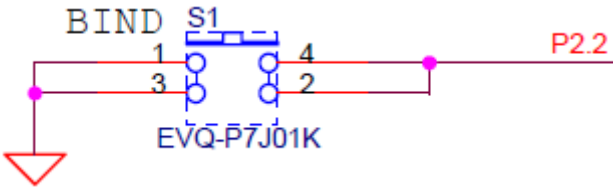
Figure 4-15. Schematic View of ISSP Header



4.2.1.5 *Channel Switch*

The S1 switch on the remote manually changes channels; 26 channels are available spaced 3 MHz apart.

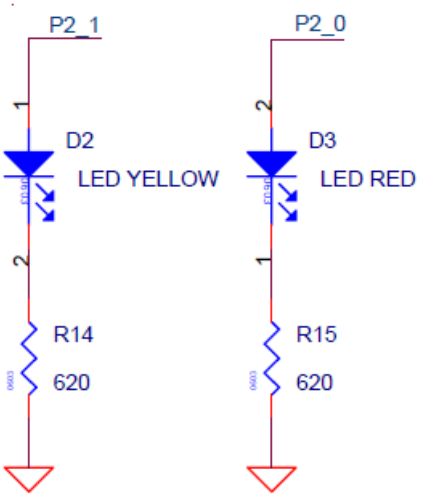
Figure 4-16. Schematic View of Switch



4.2.1.6 LEDs

The yellow LED begins blinking when the battery voltage falls to 3.65 V and the red LED when the voltage falls to 3.45 V. When the battery falls to 3.15 V, only the red LED blinks and the unit hibernates to avoid over-discharge of the Li-Ion battery.

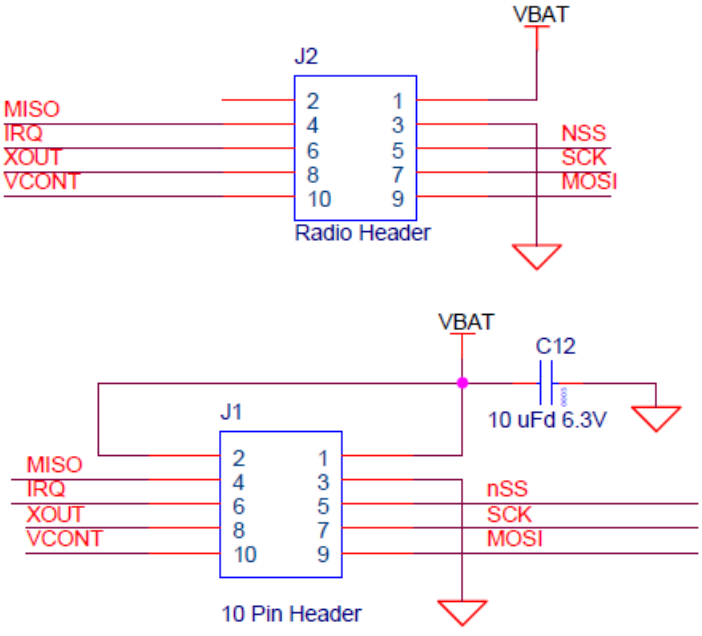
Figure 4-17. Schematic View of LEDs



4.2.1.7 Radio Header

The remote board has a 10-pin radio header J2, to which the radio with CYRF6936 is connected for radio transmission. The radio transmitter board has a 10-pin header J1 to connect to J2.

Figure 4-18. Schematic View of Radio Header and 10-Pin Header



4.2.2 Power Supply System

The CY4638 headset board has power sources from the battery supply terminal and ISSP on the board.

Figure 4-19. Power Supply System Structure for Remote

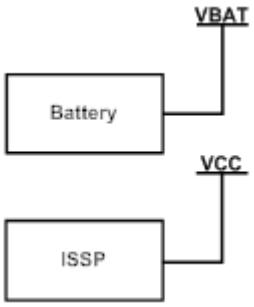
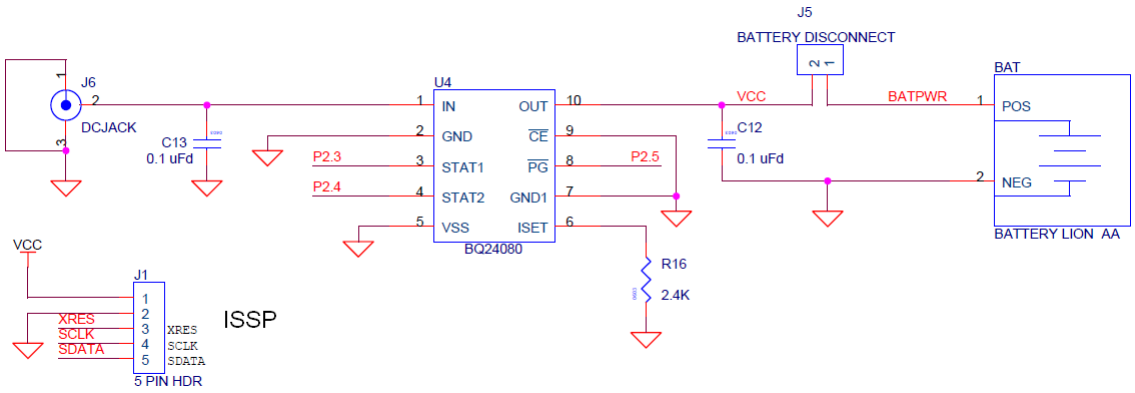


Figure 4-20. Schematic View of Remote Power Supply System



5. Code Examples

All code examples are available at `<Install_Directory>:\Cypress\CY4638 VoIP Demo\<version>\Firmware\`.

5.1 Bridge and Remote

5.1.1 Project Description

This project demonstrates the various features offered by the bridge dongle and the remote in WirelessUSB LP VoIP operation. The bridge enumerates as an audio device to which the remote is connected through wireless connection. The CYRF6936 is used for radio transmission between the bridge and the remote. The ISR flow is explained in Firmware Architecture on page 39.

5.1.2 Device Configurations

The bridge and remote use the enCoRe III chip. The enCoRe III is configured using the Device Editor in PSoC Designer. The bridge uses the SPI master, USB device, and the 16-bit PWM user modules. The remote uses two 8-bit PWMs, SPIM Radio, and Comparator user modules.

The SPIM User Module is a serial peripheral interconnect master. It performs full duplex synchronous 8-bit data transfers. SCLK phase, SCLK polarity, and LSB first can be specified to accommodate most SPI clocking modes. The clock is synchronized to SysClk.

The USBFS User Module gives a USB full-speed Chapter 9 compliant device framework. This user module gives a low-level driver for the control endpoint that decodes and dispatches requests from the USB host.

The PWM User Module uses two digital PSoC blocks, each contributing eight bits to the total resolution. To form a 16-bit pulse-width modulator (PWM), the two consecutive blocks are linked so their internal carry, terminal count, and compare signals are synchronously chained. Select compare function type as Less Than or Equal To. Enter 374 in the Period field of the PWM16 in the Device Editor. The clock is synchronized to SysClk and the pulse width is 1.

The CT block gives a simple comparator, which is at the heart of this user module. The comparator has two inputs: a positive and a negative. Both these inputs have identical connection options at their input multiplexes. This allows creating any combination of inputs with either negative or positive polarity. Positive input is selected as AnalogColumn_InputMUX_0 and negative input is VBG.

The 8-bit PWM User Module is a pulse-width modulator with programmable period and pulse width. The clock and enable signals can be selected from several sources.

Figure 5-1. Device Configuration for Bridge

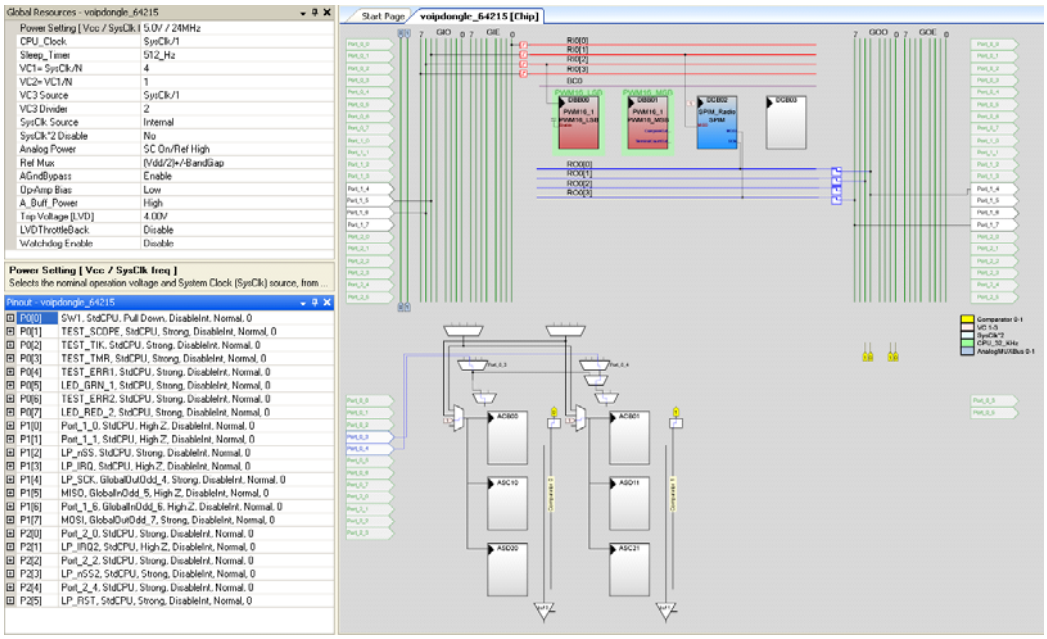
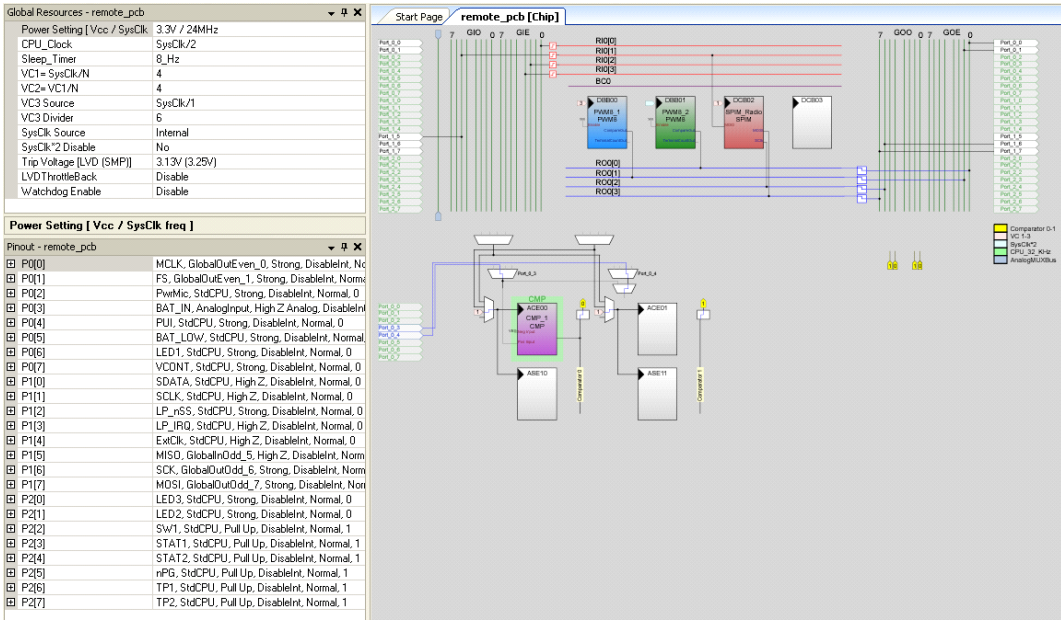


Figure 5-2. Device Configuration for Remote



5.1.3 Firmware Architecture

The most critical firmware feature is the 8-kHz interrupt. Because this ISR must minimize latency, it is the only interrupt allowed during voice traffic.

At the 24-MHz bridge, this means USB In and Out are polled and must be serviced within 1 ms of their arrival. There is a crude 4800, n, 8, 1 firmware UART within the 8-kHz ISR that is available for diagnostics.

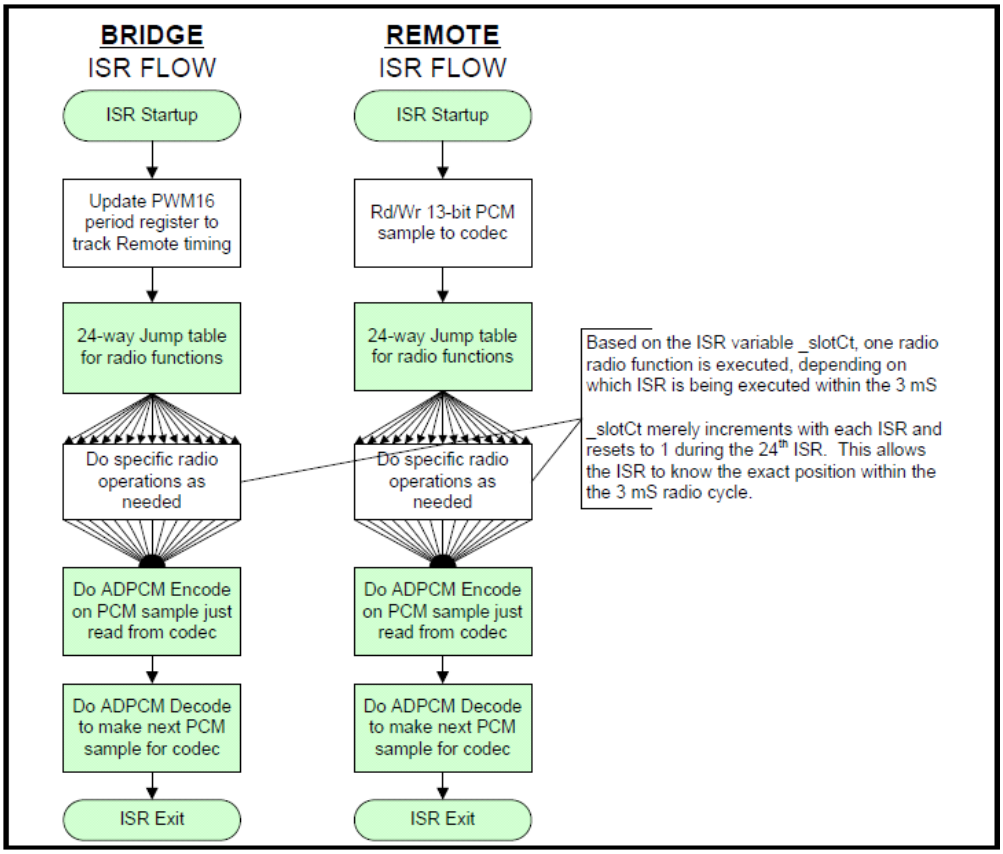
At the 12-MHz remote, this means the codec servicing is within the ISR (in addition to the basic radio slot timing). Other functions, such as channel quality decisions and any non-VoIP packet processing, are handled outside the ISR.

Both the bridge and remote use the PSoC "Large Memory Model" to access RAM pages beyond the 256 Byte Page 0. The bridge uses all four pages of RAM, while the remote uses two pages of RAM.

5.1.3.1 Outline of 8-kHz ISR

Figure 5-3 shows the bridge and remote 8-kHz ISR flow. Some operations are exactly the same (ADPCM), some vary slightly (the remote switches the antenna), and some are completely different (the bridge adjusts its ISR rate to track the remote).

Figure 5-3. 8-kHz ISR Flowchart



5.1.3.2 Radio Slot Timing

For both remote and bridge, the 8-kHz ISR establishes slot timing for the radio Tx/Rx cycling. The main difference is that the bridge adjusts its timing to track the remote. This allows the remote's codec to run at an undisturbed 8 Ksps.

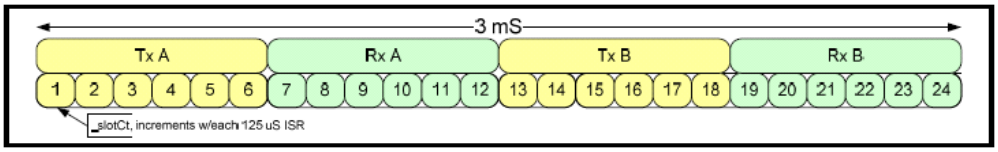
The bridge adjusts its timing using an early/late detector driven by the SOP indication from packets sent by the remote. The bridge increases or decreases its divider by 1 count from the nominal, depending on whether the SOP arrived before or after the target time. No adjustment is made if SOP fails to arrive.

The bridge also acquires and synchronizes to the remote stream. It does this by looking for two identical VoIP packets in succession. The arrival of the second packet establishes an exact reference time to initialize the bridge's 8-kHz ISR divider.

5.1.3.3 Radio Control

Each 3-ms voice packet consists of 24 individual interrupts every 125 µs. During each 750 µs, receive or transmit "slot" 6 ISRs are serviced. The 8-kHz ISR uses a state variable _slotCt to know the ISR number and what should be done to the radio during each ISR.

Figure 5-4. Relating slotCt Values to Radio State over 3 ms Interval



Different radio events occur at each _slotCt. The two Tx operations (ISR 1-6, 13-18) are similar, but not identical. The two Rx operations (ISR (7-12, 19-24) are also similar but not identical. Some ISRs do nothing to the radio, so the ISR is brief, while some ISRs use almost the entire 125 µs. The most time-critical radio timing event is writing TX_GO during ISR 1 and ISR 13. The TX_GO timing establishes exactly when the RF power begins, and thus affects the far side timing.

During some interrupts, it is possible to do many things and exceed the 125 µs interval. For example, the radio Rx buffer is partly unloaded during one ISR and partly unloaded during a subsequent ISR. This can be shared between the various 24 ISRs to some extent.

5.1.3.4 ADPCM Encode/Decode

During each ISR, ADPCM encode for one voice sample and decode for one voice sample is performed. This ensures voice processing remains synchronized with the arriving/departing radio packets. Although ADPCM can be done outside the ISR, it is deterministic and repetitive MIPS load and is cleaner inside the ISR. Storing audio samples as ADPCM rather than PCM also minimizes RAM requirements.

5.1.3.5 Self-timed Radio SPI Routines

Based on the standard radio driver, special radio SPI routines are provided for use within the ISR. These are optimized and use a "self-timing" feature of the SPI interface, whereby when a byte is written to the SPI, there is a known constant relationship between the CPU clock and the SPI clock, such that after a given number of CPU cycles, it is always true that the SPI operation has completed. This allows the SPI clock to remain at 3 MHz without any discontinuities between byte transfers, resulting in faster SPI traffic and faster ISR completion.

Note that although the bridge CPU runs at 24 MHz, its SPI runs at 3 MHz and some ISRs can have extensive SPI activity to the radio (writing 15 bytes for example). Thus, the bridge has its own set of "optimized ISR Radio SPI" functions.

5.1.3.6 Lowpass Filtered Statistics

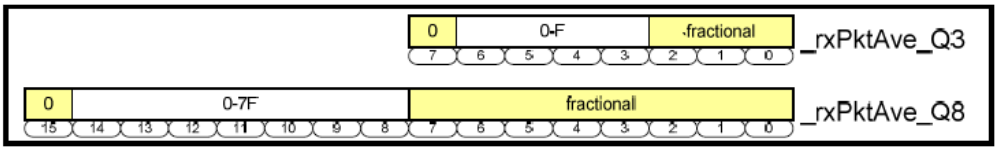
Both the bridge and remote maintain voice packet error filters. Slow and fast response filters are provided. These filters are driven with TRUE when a valid 3-ms audio set is available and FALSE when no audio samples are available. The filters are updated every 3 ms with the TRUE/FALSE result.

The fast filter variable (_rxPktAve_Q3) has a rise time of about 50 ms. When evaluating the filter, only bits [6:3] are used.

The slow filter variable (_rxPktAve_Q8) has a rise time of about 1.5 seconds. When evaluating this filter, only the upper byte is used (this is analogous to a right-shift-8). The filter maximum is 0x7F and results when there has been no lost audio for several seconds.

The Q notation indicates an implied decimal point. For example, if the value 0x18 is interpreted in Q4 format, it represents 1.5 (1 + ½). In Q0 format, 0x18 represents 24. In Q5 format, it represents 0.75 (½+ ¼). The Q notation suggests how the variable should be rendered.

Figure 5-5. Lowpass _rxPktAve Filter RAM Structure



Other filtered statistics for RSSI are maintained, but are currently unused. Also, some statistics are maintained to measure differences between antenna quality (it varies depending on multipath).

5.1.3.7 Channel Change Execution

Both sides change channels within the ISR, allowing the channel change to be synchronized with the radio state and the overall slot timing. The radio state is also known and easily controlled.

5.1.3.8 Remote Specific ISR Functions

For the remote, the 8-kHz ISR establishes the codec ADC/DAC read/write timing over the 3-wire SPI. This is among the first things done in the remote's ISR to minimize sampling. The codec read and write are simultaneous using 16 clocks.

5.1.3.9 Bridge Specific ISR Functions

The bridge adjusts its ISR to track the SOP of frames from a remote. The bridge ISR also produces a 4800, n, 8, 1 serial stream that can be used for diagnostic data.

5.1.3.10 Outline of Non-ISR Functions

Most of the non-ISR functions are written in 'C' for maintenance simplicity, although a few simple functions that consume MIPS are implemented as assembly calls.

5.1.3.11 Channel Change Determination

The fast and slow packet averages are monitored. When the fast average reaches a threshold (~20% success), the channel is immediately changed. The far side eventually recognizes the change (via its fast filter) and reacquires. The slow packet average thresholds are set much higher (~95%) because they attempt to measure occasional disruptions to the audio stream. This threshold should change the channel when the audio remains coherent, but becomes "annoying".

The non-ISR routine only "requests" that the ISR change the channel. The ISR changes the channel at the next convenient point in the 3-ms cycle.

5.1.3.12 Remote Non-ISR Functions

Li-Ion Battery Gauge

The remote monitors the Li-Ion battery voltage using a comparator and an external resistor network. When battery voltage is very low, the processor shuts down to minimize battery drain and prevent damage to the Li-Ion battery. The comparator can detect three different voltage points to establish four levels (depending on whether R7 is pulled Low, Tristate, or High). Using the standard 82.5-K, 49.4-K, and 511-K resistors, these voltage points are 3.65 V, 3.45 V, and 3.15 V. The maximum charge voltage for the Li-Ion battery is 4.20 V.

Li-Ion Charging

The remote monitors the Li-Ion charger to determine Li-Ion charging progress. When charging starts, the radio is stopped to minimize power so the charge circuit can measure charge current more accurately. When the charger completes, a charge complete indication is given. At below 4.20 V, the charger provides a constant charging current to the battery. When the battery voltage reaches 4.20 V, the charger provides a constant voltage to the battery (it reduces current it provides to maintain 4.2 V). When the charge current reduces to about 30 mA, the charger considers the battery fully charged.

5.1.3.13 Bridge Non-ISR Functions

USB Polling

The bridge monitors the USB endpoints and services them as needed. USB packets contain eight 16-bit signed PCM samples and arrive/depart every 1 ms.

Audio Sample Rate Matching

Buffering and rate matching is done as needed between the USB/PC such that the sample stream traversing the RF link (based on the remote radio's 12 MHz crystal) tracks the sample stream traversing the USB link. Samples are inserted or duplicated as needed to avoid buffer underflow/overflow.

5.1.3.14 *Detailed Radio Operations during the 24 ISR Counts*

The _slotCt determines which radio operations occur during each ISR.

_slotCt	Unique Remote Functions
Tx_1a/b	Changes antennas. Confirm Radio has exited RX_GO and it's possible to issue a TX_GO. Write TX_GO, Tx Length, and EndState.
Tx_2a/b	Read result of prior RX_GO If valid Rx data, read Length field. Read and average the RSSI from the antenna (not used for anything currently) Determine whether Rx packet disposition.
Tx_3a/b	Unload about part of Rx packet (if it was pending in radio buffer)
Tx_4a/b	Unload remainder of Rx packet (if it was pending in radio buffer) If Tx GO was skipped (because radio RX_GO was overtime), manually set radio in RX_SYNTH or preparation for Rx slot (because RX_GO always ends in TX_SYNTH).
Tx_5a/b	NONE
Tx_6a/b	NONE
Rx_1a/b	If channel change is requested, divert here because the radio state is known Issue RX_GO, clear false SOP hardware bug, EndState is TX_SYNTH
Rx_2a/b	If SOP failed to arrive, begin Rx Abort. If SOP arrived, clear SOP to expose RXC/RXE on radios IRQ line.
Rx_3a/b	If Rx Abort is issued, continue Rx Abort process.
Rx_4a/b	NONE
Rx_5a/b	Prepare to preload radio Tx buffer with data. The "b" slot clears the radio's Tx buffer. The "a" slot usually leaves the prior VoIP data in the radio's Tx buffer for reuse. Although occasionally clear the radio's Tx buffer to preload non-VoIP control data instead.
Rx_6a/b	Preload radio Tx buffer with data. The "b" slot copies the VoIP packet to the radio's Tx buffer and begins gathering the next VoIP packet by recording the ADPCM state snapshot for the new packets ADPCM samples. The "a" slot usually does nothing ad could occasionally send non-VoIP control data instead.

Figure 5-6 shows an overview of the remote radio operation over a 3-ms cycle. The following signals are shown:

D15: SS SPI Slave Select to radio (active LOW)

D14: CK SPI Clock

D13: MO SPI Master Out

D12: MI SPI Master In

D11: IRQ Radio IRQ line (active HIGH)

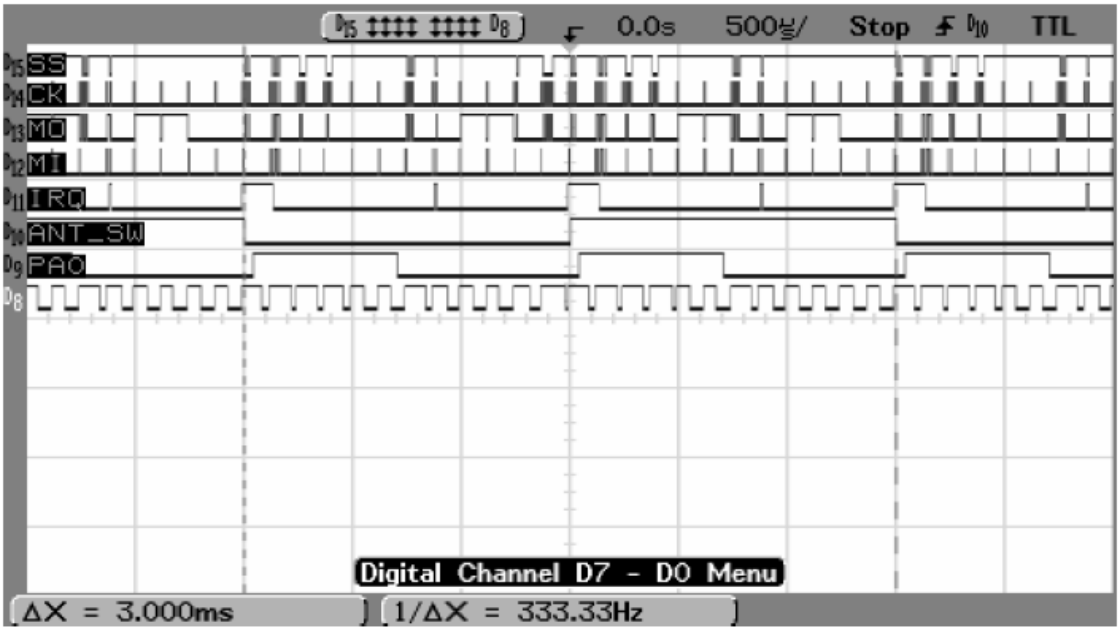
D10: ANT_SW Selects antenna A or B

D9: PA0 Radio PACTL signal

D8: Indicates ISR active time (set High upon ISR entry, Low on ISR exit).

The time-cursors enclose a 3.000 ms window. This window begins with ANT_SW Low for 1.5 ms and ends with ANT_SW High for 1.5 ms (each antenna is used to send and receive one 750 µs packet).

Figure 5-6. Remote Timing Overview



Note the SPI transfer to the codec at the start of each 125 µs interrupts (low pulses on D8). This is indicated by SPI clocking on CK when the radio is not selected (SS is high). This is periodic, occurring at the same offset from the 8-kHz ISR.

The ISR execution time varies greatly, depending on the SPI activity to the radio. This load varies from ISR to ISR over the 24 ISR (3 ms) interval. Many radio operations can be shifted around slightly to level the ISR load, such that no ISR ever exceeds its 125 µs allotment (delaying a subsequent ISR).

Figure 5-7 shows timing relationships between the remote and bridge. This figure adds the bridge timing (lower half) to the remote timing (upper half) introduced in Figure 5-6. The following additional signals are shown:

D7: Indicates ISR active time (set High upon ISR entry, Low on ISR exit).

D6: PA0 Radio PACTL signal

D5: Unused

D4: IRQ Radio IRQ line (active HIGH)

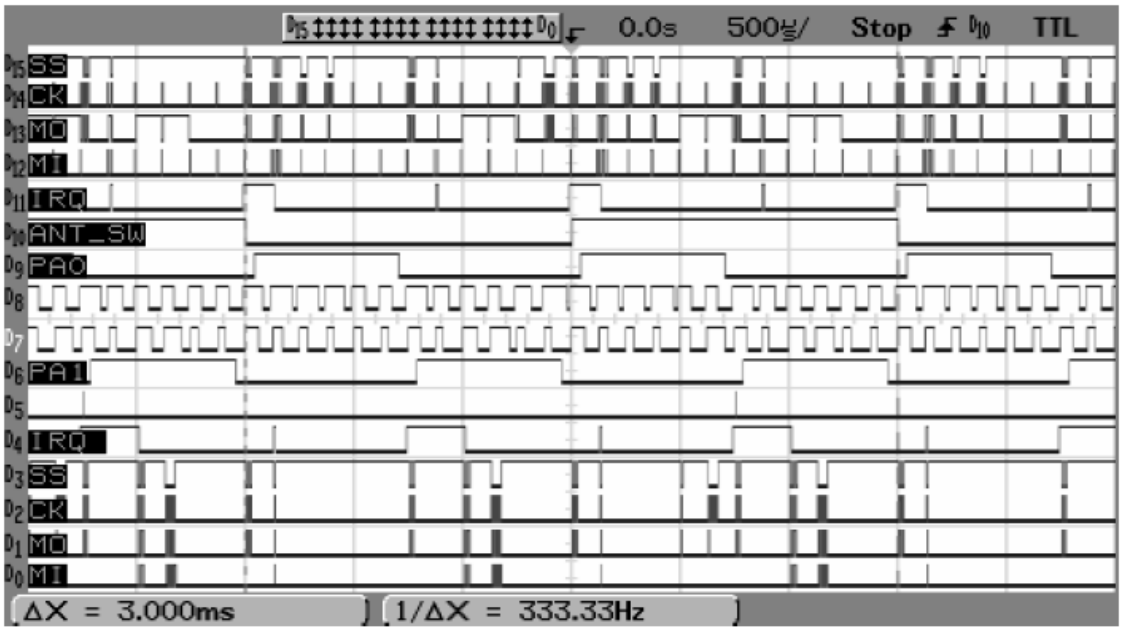
D3: SS SPI Slave Select to radio (active LOW)

D2: CK SPI Clock

D1: MO SPI Master Out

D0: MI SPI Master In

Figure 5-7. Combined Remote and Bridge Timing Overview



Comparing D8 and D7 shows that the 24-MHz bridge ISR completes faster than the 12-MHz remote, although the 3-MHz SPI transactions take about the same time.

The narrow pulse on the IRQ is the SOP detection, while the wider pulses are the delay between Rx Complete and the packet starting to be unloaded from the radio's Rx FIFO. The SOP detection at the bridge is the timing tracking point.

Figure 5-8 illustrates the six interrupts that comprise the Remote Tx packet. Before the first interrupt (off the screen to the left), the Tx data is loaded into the Tx FIFO. The first interrupt writes Tx GO to the radio. Then (at the left-cursor), PA0 goes active (PACTL) indicating RF power is being emitted. Subsequent interrupts begin the Rx FIFO unload process - the actual data unload is spread over the third and fourth interrupts. The fifth and sixth interrupts have no radio SPI activity.

Note that the bridge's PA1 goes active 750 µs after the remote's PA0; thus, packets are spaced by 750 µs. There is an 85 µs window when both PA1 and PA0 are inactive.

The D4:IRQ at the bridge indicates SOP about 90 µs after the remote begins transmitting the packet (D9:PA0 goes high). The SPI write at the bridge clears the SOP IRQ and exposes the RXC/RXE IRQ (which happens about 50 µs after the packet actually arrives inside the radio).

Figure 5-8. Remote Tx Cycle Bridge Rx Cycle

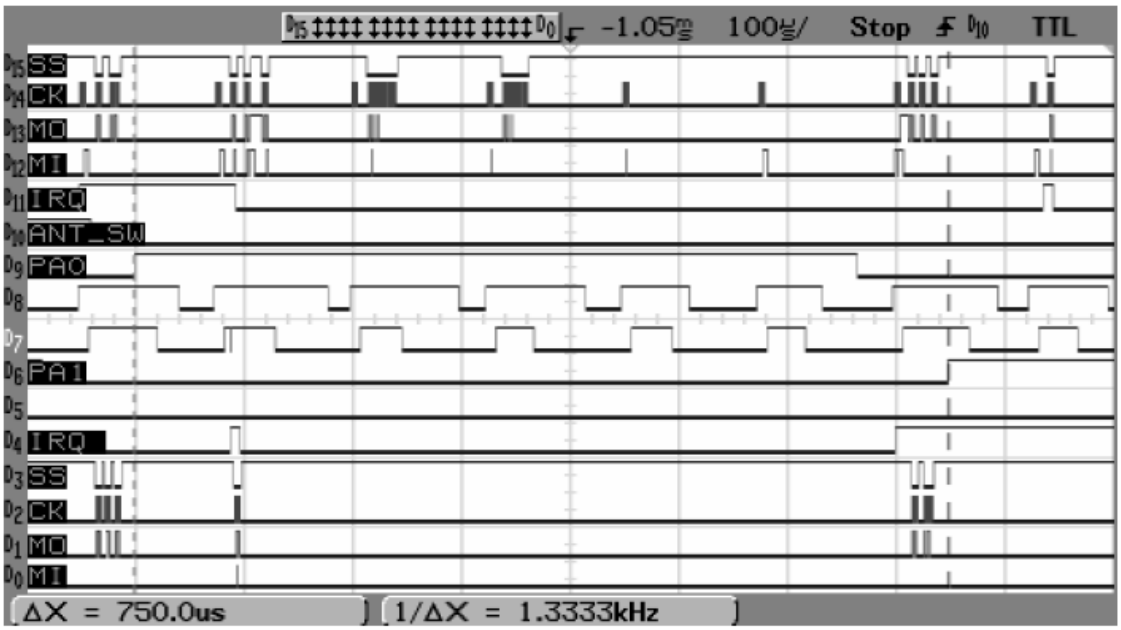
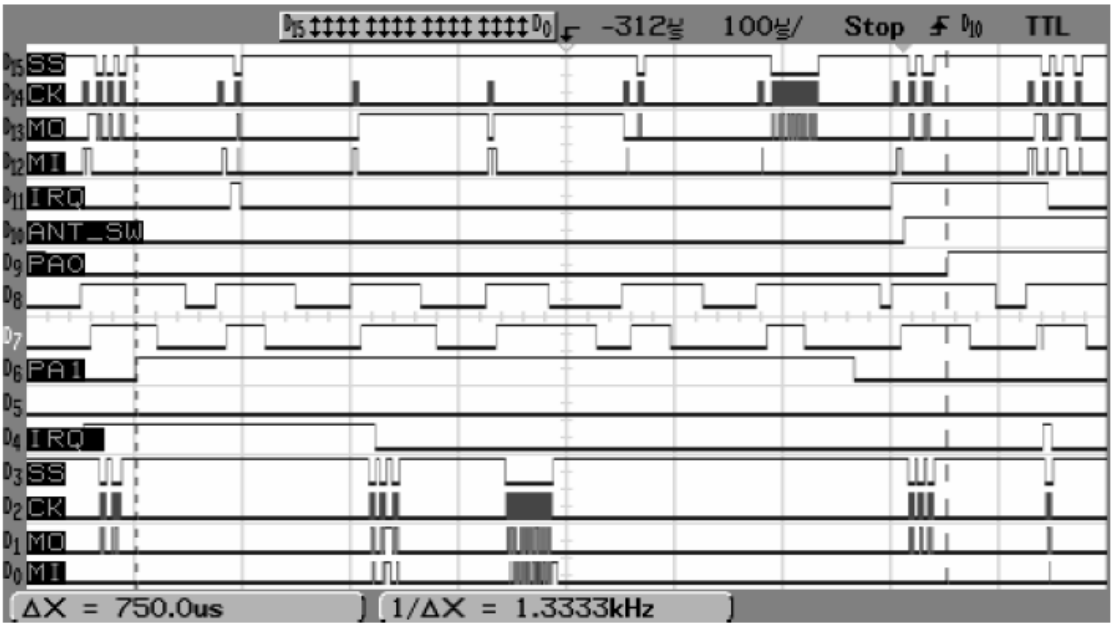


Figure 5-9 illustrates the six interrupts that comprise the Bridge Tx packet. Timing is similar to the Remote Tx cycle shown in Figure 5-8. A minor difference is that the Rx data unloaded from the previous Remote Tx cycle is completely unloaded in the fourth interrupt because the bridge runs at 24 MHz; all 15 bytes can be unloaded together.

Because the bridge has no SPI activity to support a codec, the bridge ISR is even faster than the remote.

Figure 5-9. Bridge Tx Cycle, Remote Rx Cycle



5.1.4 Verify Output

1. Connect the bridge dongle to the PC and wait for the dongle to enumerate (the bridge enumerates as a USB audio device); after the bridge is enumerated, the remote can be used with the dongle.
2. Connect the microphone and the speaker to the remote and start using the CY4638 WirelessUSB LP VoIP Demo kit.
3. Start using the bridge and the remote headset for duplex wireless audio transmission.
4. To check the VoIP kit, make a call on the Skype or Google Talk or play any music file.
5. The red LED blinks indicating USB-out traffic from the PC.

A. Appendix

A.1 Schematic

Figure A-1. Bridge

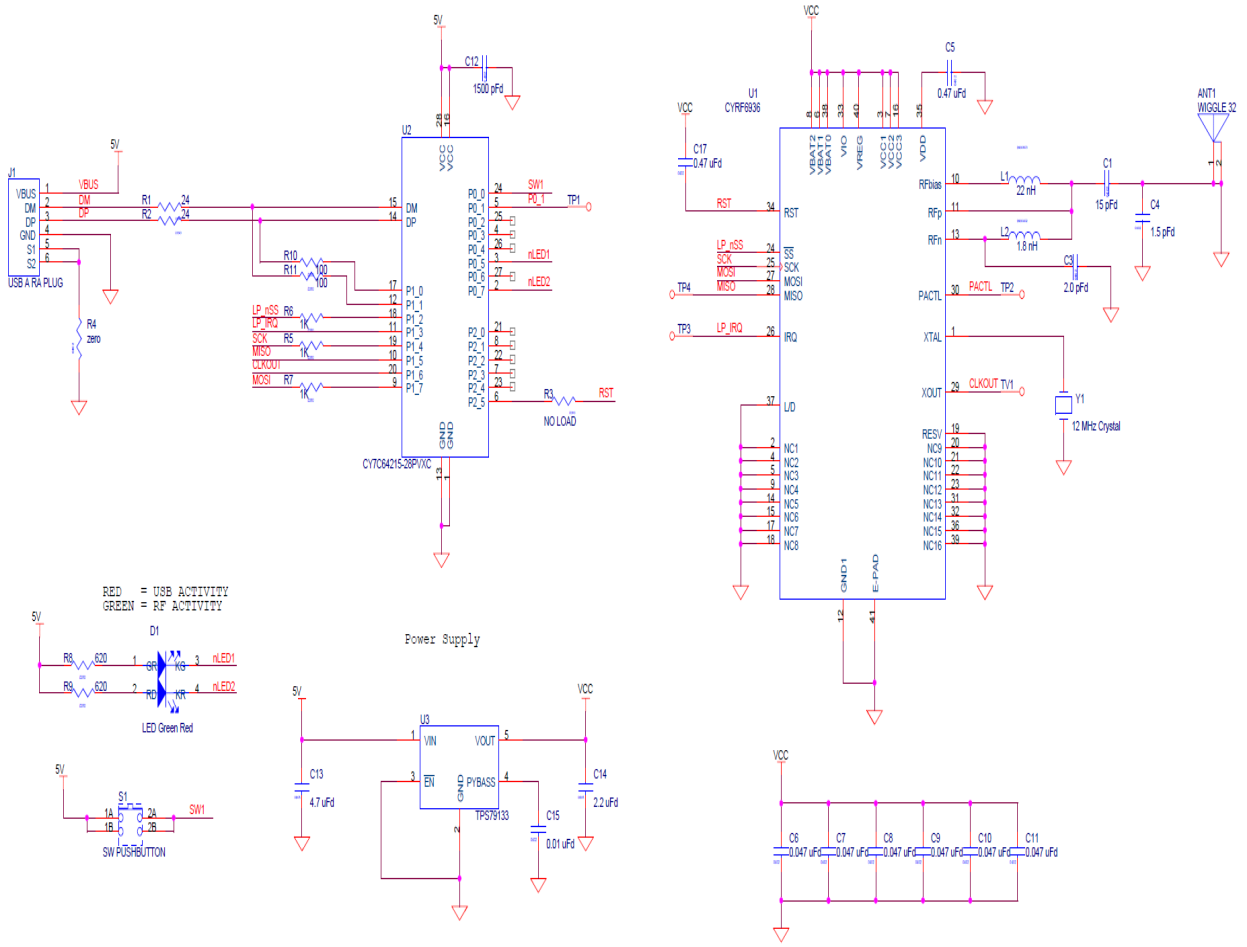


Figure A-2. Remote

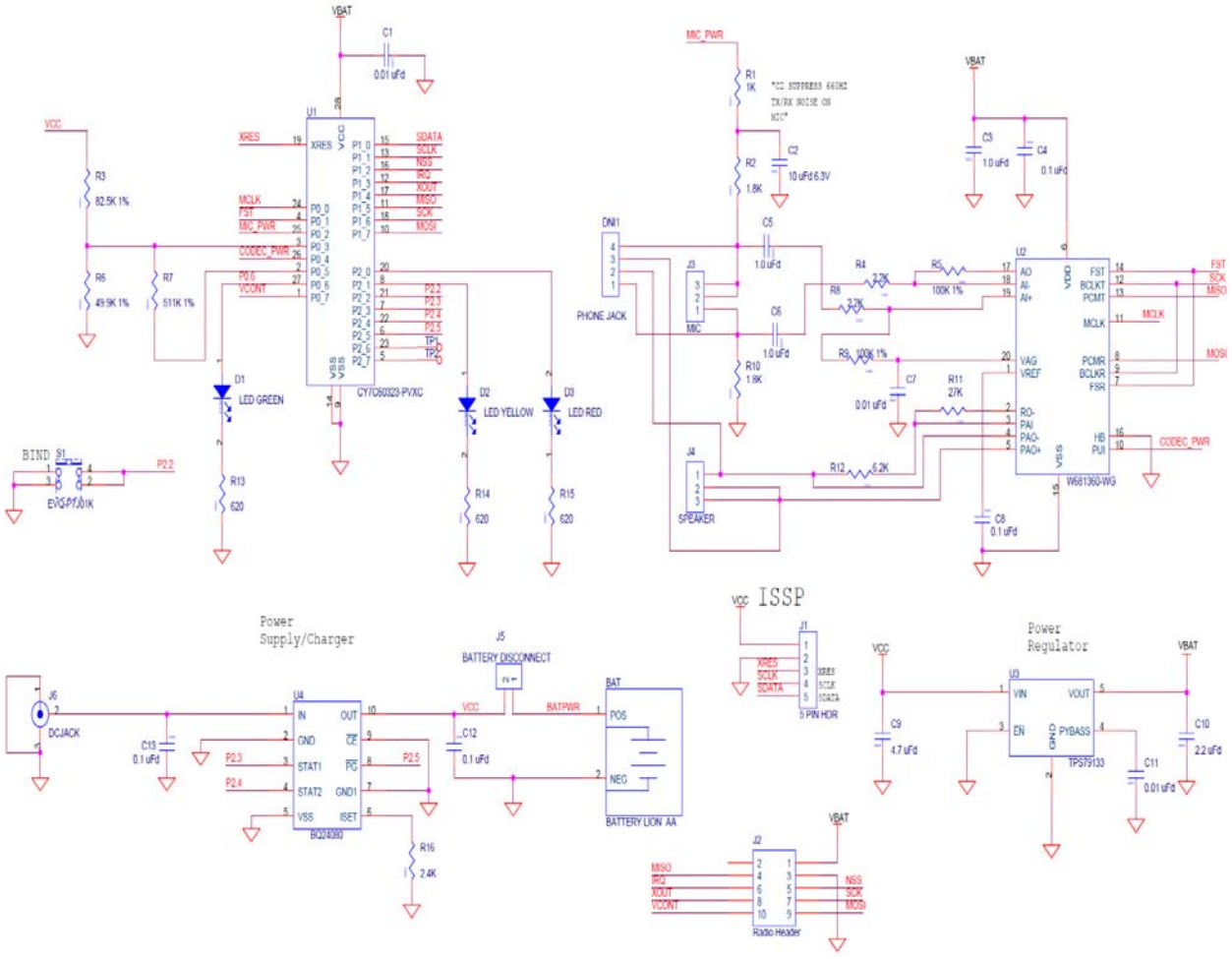
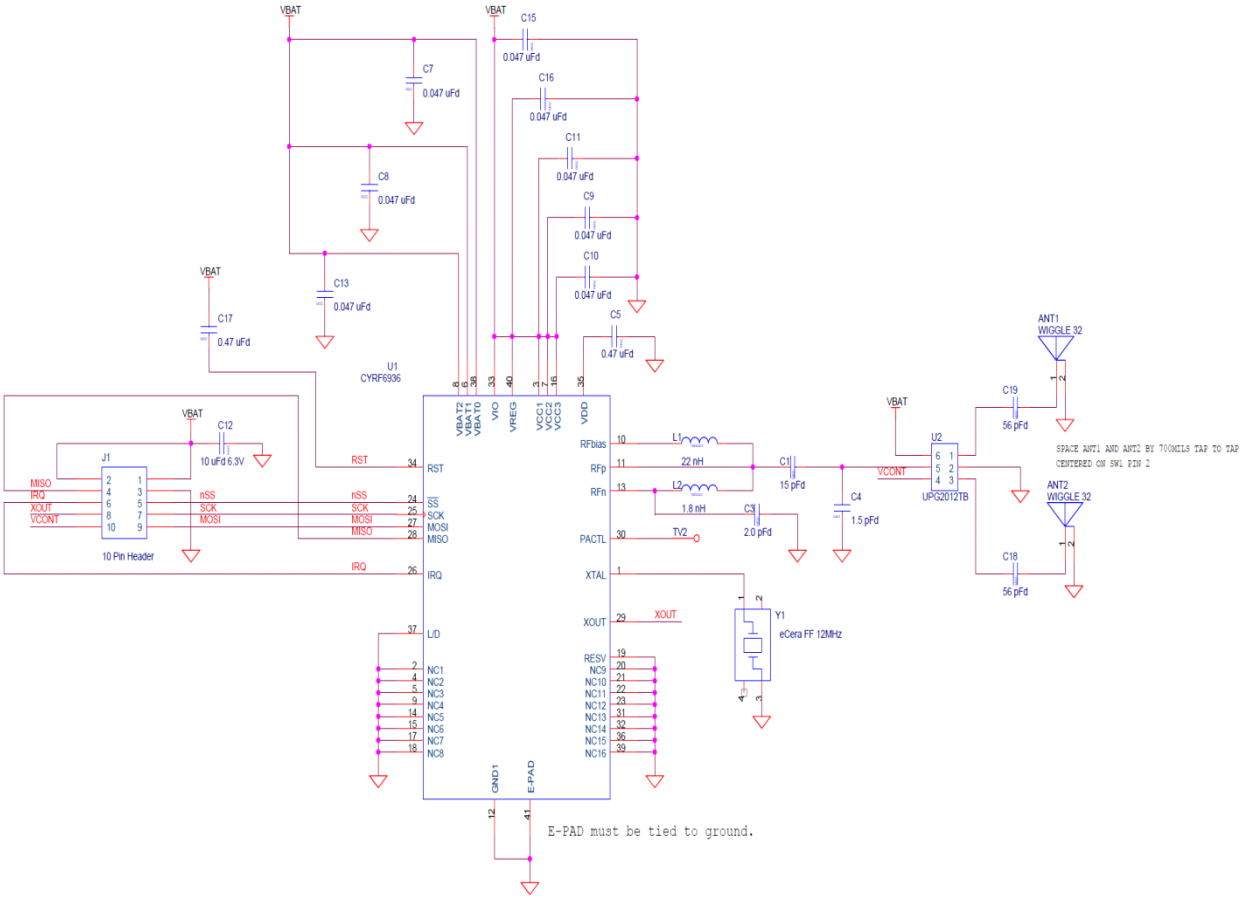


Figure A-3. Radio



A.2 Board Layout

Figure A-4. Bridge Top

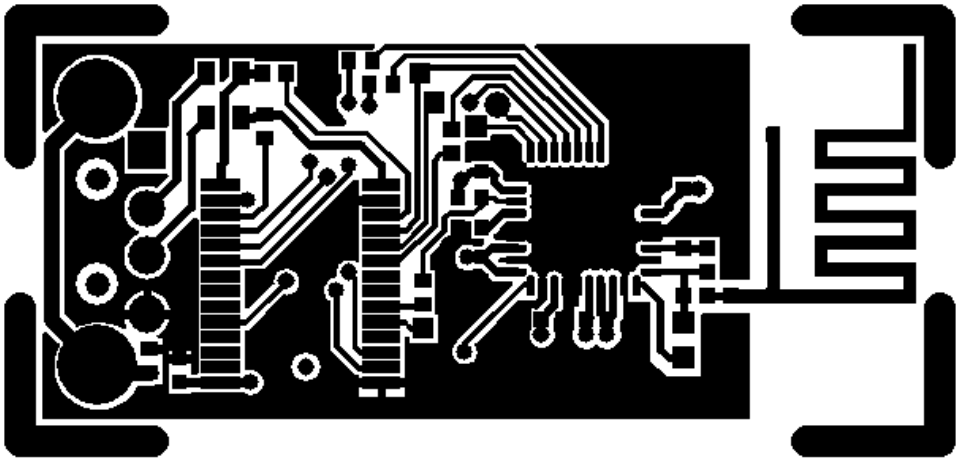


Figure A-5. Bridge Bottom

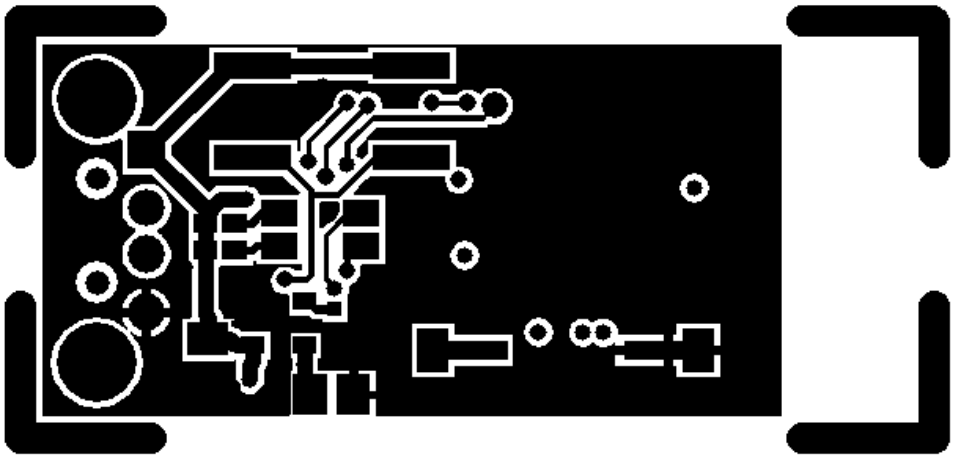


Figure A-6. Remote Top

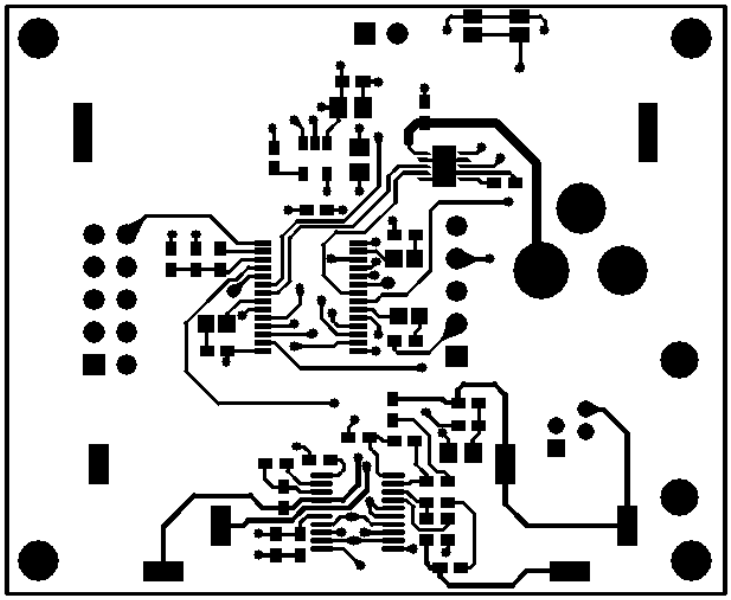


Figure A-7. Remote Bottom

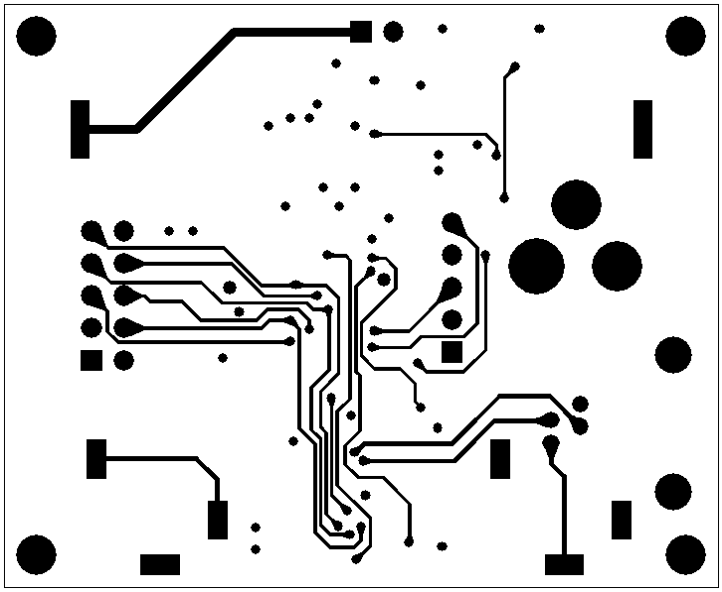
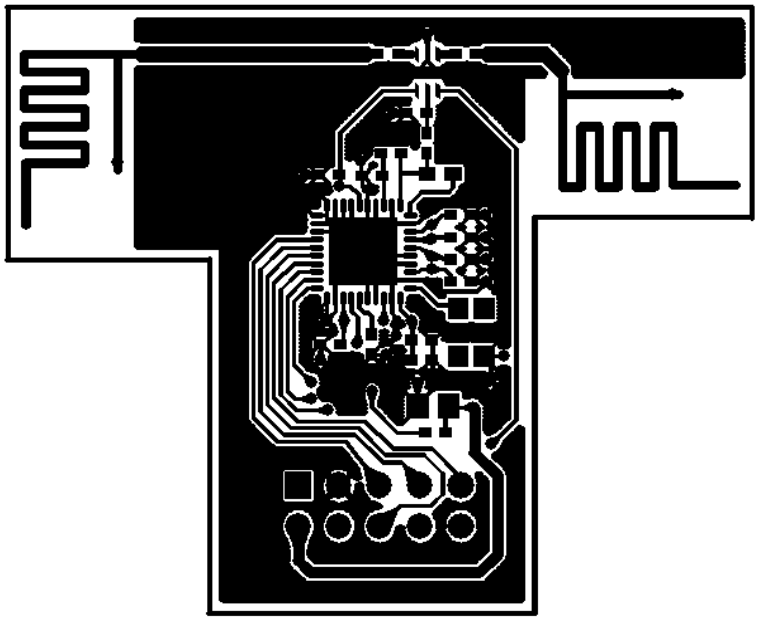


Figure A-8. Radio Top



A.3 Bill of Materials (BOM)

A.3.1 LP RDK Dongle III

No.	Qty.	Reference	Description	Manufacturer	Mfr Part Number
1	1	C1	CAP 15PF 50 V CERAMIC NPO 0402	Panasonic	ECJ-0EC1H150J
2	1	C3	CAP 2.0 PF 50 V CERAMIC NPO 0402	Kemet	C0402C209C5GACTU
3	1	C4	CAP 1.5PF 50 V CERAMIC NPO 0402 SMD	Panasonic	ECJ-0EC1H1R5C
4	2	C17,C5	CAP CER .47UF 6.3 V X5R 0402	Murata	GRM155R60J474KE19D
5	6	C6,C7,C8,C9, C10,C11	CAP CERM .047UF 10% 16 V X5R 0402	AVX	0402YD473KAT2A
6	1	C12	CAP 1500PF 50 V CERAMIC X7R 0402	Kemet	C0402C152K5RACTU
7	1	C13	CAP CERAMIC 4.7UF 6.3 V X5R 0805	Kemet	C0805C475K9PACTU
8	1	C14	CAP CER 2.2UF 10 V 10% X7R 0805	Murata Electronics North America	GRM21BR71A225KA01L
9	1	C15	CAP 10000PF 16 V CERAMIC 0402 SMD	Panasonic - ECG	ECJ-0EB1C103K
10	1	D1	LED GREEN/RED BICOLOR 1210 SMD	LITEON	LTST-C155KGJRKT
11	1	J1	CONN USB PLUG TYPE A PCB TH	ACON	UAR10-4W5100
12	1	L1	INDUCTOR 22NH 2% FIXED 0603 SMD	Panasonic - ECG	ELJ-RE22NGF2
13	1	L2	INDUCTOR 1.8NH +-.3NH FIXED 0402 SMD	Panasonic - ECG	ELJ-RF1N8DF
14	2	R1,R2	RES 24 OHM 1/16W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ240V
15	1	R4	RES ZERO OHM 1/16W 0402 SMD	Panasonic - ECG	ERJ-2GE0R00X
16	3	R5,R6,R7	RES CHIP 1K OHM 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ102X
17	2	R9,R8	RES CHIP 620 OHM 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ621X
18	2	R10,R11	RES CHIP 100 OHM 1/16W 1% 0402 SMD	Phycomp USA Inc	9C1A04021000FLHF3
19	1	S1	LT SWITCH 6MM 160GF H=2.5MM SMD	Panasonic - ECG	EVQ-QWS02W
20	1	U1	IC, LP 2.4 GHz RADIO SoC QFN-40	Cypress Semicon-ductor	CYRF6936-40LFXC
21	1	U2	IC FULL-SPEED USB ENCORE III CONTROL-LER SSOP28	Cypress Semicon-ductor	CY7C64215-PVXC
22	1	U3	IC LDO RGLTR 3.3 V LN SOT-23-5	Texas Instruments	TPS79133DBVR
23	1	Y1	CRYSTAL 12.00MHZ HC49 SMD	eCERA	GF-1200008
24	1	PCB	PRINTED CIRCUIT BOARD	Cypress Semicon-ductor	PDC-9267-*C
25	1	LABEL1	Serial Number		
26	1	LABEL2	PCA #		121-26703 *B
No Load Components - Do Not Install					
27	1	R3	NO LOAD		
28	1	ANT1	2.5GHZ H-STUB WIGGLE ANTENNA FOR 32MIL PCB	NA	NA
29	4	TP1,TP2,TP3, TP4	TEST PAD 30 SMT	NA	NA
30	1	TV1	TEST VIA 40 HOLE 20 PLATED	None	

A.3.2 VoIP Remote

No.	Qty.	Reference	Description	Manufacturer	Mfr Part Number
1	1	BAT1	BATTERY, Li-Ion, 350 mAh, AAA size w/tabs	BatterySpace.com	LC10440
2	3	C1,C7,C11	CAP 0.01UF 50 V CERAMIC X7R 0603	Panasonic	ECJ-1VB1H103K
3	1	C2	CAP CERAMIC 10UF 6.3 V X5R 0805	Kemet	C0805C106K9PACTU
4	3	C3,C5,C6	CAP CERAMIC 1.0UF 10 V X5R 0603	Kemet	C0603C105K8PACTU
5	4	C4,C8,C12,C13	CAP .1UF 50 V CERAMIC Y5V 0603	Panasonic - ECG	ECJ-1VF1H104Z
6	1	C9	CAP CERAMIC 4.7UF 6.3 V X5R 0805	Kemet	C0805C475K9PACTU
7	1	C10	CAP CER 2.2UF 10 V 10% X7R 0805	Murata Electronics	GRM21BR71A225KA01L
8	1	D1	LED GREEN CLEAR 0603 SMD	Lite-On Inc.	LTST-C190GKT
9	1	D2	LED YELLOW CLEAR 0603 SMD	Lite-On Inc.	LTST-C190YKT
10	1	D3	LED RED CLEAR 0603 SMD	Lite-On Inc.	LTST-C190CKT
11	1	J1	CONN HDR BRKWAY 5POS STR AU PCB	AMP Division of Tyco	103185-5
12	1	J2	CONN RCPT VERT 10POS DUAL .100 GOLD	3M/ESD	929975-01-05-RK
13	2	J4,J3	CONN JACK STEREO R/A 3PIN 3.5MM	CUI Inc	SJ1-3513N
14	1	J5	HEADER 2 POS 0.318 mm HT MODII SRST B/A	AMP Division of Tyco	103321-2
15	1	J6	CONN 2.1MM PWRJACK RT ANGLE PCB	Switchcraft Inc.	RAPC722
16	1	R1	RES 1.0K OHM 1/16W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ102V
17	2	R2,R10	RES 1.8K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ182V
18	2	R9,R5	RES CHIP 100K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-07100KL
19	1	R6	RES 49.9K OHM 1/10W 1% 0603 SMD	Panasonic - ECG	ERJ-3EKF4992V
20	1	R3	RES 82.5K OHM 1/10W 1% 0603 SMD	Panasonic - ECG	ERJ-3EKF8252V
21	2	R8,R4	RES CHIP 2.2K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ222V
22	1	R7	RES 511K OHM 1/10W 1% 0603 SMD	Panasonic - ECG	ERJ-3EKF5113V
23	1	R11	RES 27K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ273V
24	1	R12	RES 6.2K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ622V
25	3	R13,R14,R15	RES 620 OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ621V
26	1	R16	RES 2.4K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ242V
27	1	S1	SWITCH LT 3.5MMX2.9MM 160GF SMD	Panasonic - ECG	EVQ-P7J01K
28	2	TP2,TP1	TEST POINT	NA	NA
29	1	U1	IC WIRELESS MICROCONTROLLER SSOP28	Cypress Semiconductor	CY7C60323-PVXC
30	1	U2	IC, CODEC 13-BIT, TSSOP20	WINDBOND	W681360-WG
31	1	U3	IC LDO RGLTR 3.3 V LN SOT-23-5	Texas Instruments	TPS79133DBVR
32	1	U4	IC LI-ION PWR MGMT 1CELL 10-SON	Texas Instruments	BQ24080DRCR
33	4		NUT, 4-40 NYLON		H616-ND
34	4		STANDOFF, 4-40, M/F, NYLON, .500"		4802K-ND
35	1	PCB	PRINTED CIRCUIT BOARD	Cypress Semiconductor	PDC-9373-*A
36		LABEL1	Serial Number		XXXXXXXX
37	1	LABEL2	PCA #		121-37300 *A
No Load Components - Do Not Install					
1	1	DNI1	Connector, modular, handset, RJ-9	Hirose	TM3RA-44

A.3.3 LP Diversity Radio Module

No.	Qty.	Reference	Description	Manufacturer	Mfr Part Number
1	2	ANT2,ANT1	2.5 GHZ H-STUB WIGGLE ANTENNA 32MIL PCB	NA	NA
2	1	C1	CAP 15PF 50 V CERAMIC NPO 0402	Panasonic	ECJ-0EC1H150J
3	1	C3	CAP 2.0 PF 50 V CERAMIC NPO 0402	Kemet	C0402C209C5GACTU
4	1	C4	CAP 1.5PF 50 V CERAMIC NPO 0402 SMD	PANASONIC	ECJ-0EC1H1R5C
5	2	C19,C18	CAP 56PF 50 V CERAMIC 0402 SMD	Panasonic	ECJ-0EC1H560J
6	2	C17,C5	CAP 0.47 uF 6.3 V CERAMIC X5R 0402	Murata	GRM155R60J474KE19D
7	1	C12	CAP CERAMIC 10UF 6.3 V X5R 0805	Kemet	C0805C106K9PACTU
8	8	C7,C8,C9,C10,C11,C13,C15,C16	CAP CERM .047UF 10% 16 V X5R 0402	AVX	0402YD473KAT2A
9	1	J1	CONN HDR VERT 10POS .100 GOLD	Molex/GC/Waldom Inc.	10-89-1101
10	1	L1	INDUCTOR 22NH 2% FIXED 0603 SMD	Panasonic - ECG	ELJ-RE22NGFA
11	1	L2	INDUCTOR 1.8NH +-.3NH FIXED 0402 SMD	Panasonic - ECG	ELJ-RF1N8DFB
12	1	U1	IC, LP 2.4 GHz RADIO SoC QFN-40	Cypress Semiconductor	CYRF6936-40LFXC
13	1	U2	LP BAND SPDT RF SWITCH	NEC/CEL	UPG2012TB
14	1	Y1	Crystal 12 Mhz 10pf 4025 SMD	eCERA	FX1200030
15	1	PCB	PRINTED CIRCUIT BOARD	Cypress Semiconductor	PDC-9372-**
16	1	LABEL1	Serial Number		XXXXXXXX
17	1	LABEL2	PCA #		121-34600 **