Dual, Current-Output, Serial-Input, 16-/14-Bit DAC

AD5545/AD5555

FEATURES

16-bit resolution AD5545
14-bit resolution AD5555
±1 LSB DNL monotonic
±2 LSB INL AD5545
2 mA full-scale current ±20%, with V_{REF} = 10 V
0.5 µs settling time
2Q multiplying reference-input 4 MHz BW
Zero or midscale power-up preset
Zero or midscale dynamic reset
3-wire interface
Compact TSSOP-16 package

APPLICATIONS

Automatic test equipment
Instrumentation
Digitally controlled calibration
Industrial control PLCs
Programmable attentuator

PRODUCT OVERVIEW

The AD5545/AD5555 are 16-bit/14-bit, current-output, digital-to-analog converters designed to operate from a single 5 V supply with bipolar output up to ±15 V capability.

An external reference is needed to establish the full-scale output-current. An internal feedback resistor (R_{FB}) enhances the resistance and temperature tracking when combined with an external op amp to complete the I-to-V conversion.

A serial data interface offers high speed, 3-wire microcontroller compatible inputs using serial data in (SDI), clock (CLK), and chip select ($\overline{CS}$). Additional $\overline{LDAC}$ function allows simultaneous update operation. The internal reset logic allows power-on preset and dynamic reset at either zero or midscale, depending on the state of the MSB pin.

The AD5545/AD5555 are packaged in the compact TSSOP-16 package and can be operated from –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

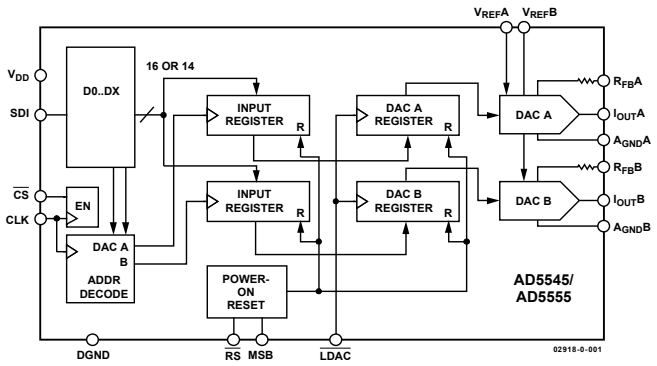

Figure 1.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

AD5545/AD5555—ELECTRICAL CHARACTERISTICS

Table 1. V_{DD} = 5 V ± 10%, I_{OUT} = Virtual GND, GND = 0 V, V_{REF} = 10 V, T_A = Full Operating Tempearture Range, unless otherwise noted.

Parameter	Symbol	Conditions	5 V ± 10%	Units
STATIC PERFORMANCE[1]				
Resolution	N	AD5545, 1 LSB = $V_{REF}/2^{16}$ = 153 µV when V_{REF} = 10 V	16	Bits
Resolution	N	AD5555, 1 LSB = $V_{REF}/2^{14}$ = 610 µV when V_{REF} = 10 V	14	Bits
Relative Accuracy	INL	AD5545	±2	LSB max
Relative Accuracy	INL	AD5555	±1	LSB max
Differential Nonlinearity	DNL	Monotonic	±1	LSB max
Output Leakage Current	I_{OUT}	Data = 0x0000, T_A = 25°C	10	nA max
Output Leakage Current	I_{OUT}	Data = 0x0000, T_A = T_A Max	20	nA max
Full-Scale Gain Error	G_{FSE}	Data = Full Scale	±1/±4	mV typ/max
Full-Scale Temperature Coefficient[2]	TCV_{FS}		1	ppm/°C typ
REFERENCE INPUT				
V_{REF} Range	V_{REF}		−12/+12	V min/V max
Input Resistance	R_{REF}		5	kΩ typ[3]
Input Capacitance[2]	C_{REF}		5	pF typ
ANALOG OUTPUT				
Output Current	I_{OUT}	Data = Full Scale	2	mA typ
Output Capacitance[2]	C_{OUT}	Code Dependent	200	pF typ
LOGIC INPUTS AND OUTPUT				
Logic Input Low Voltage	V_{IL}		0.8	V max
Logic Input High Voltage	V_{IH}		2.4	V min
Input Leakage Current	I_{IL}		10	µA max
Input Capacitance[2]	C_{IL}		10	pF max
INTERFACE TIMING[2, 4]				
Clock Input Frequency	f_{CLK}		50	MHz
Clock Width High	t_{CH}		10	ns min
Clock Width Low	t_{CL}		10	ns min
$\overline{CS}$ to Clock Setup	t_{CSS}		0	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		10	ns min
Data Setup	t_{DS}		5	ns min
Data Hold	t_{DH}		10	ns min
$\overline{LDAC}$ Setup	t_{LDS}		5	ns min
Hold	t_{LDH}		10	ns min
$\overline{LDAC}$ Width	t_{LDAC}		10	ns min
SUPPLY CHARACTERISTICS				
Power Supply Range	V_{DD} Range		4.5/5.5	V min/V max
Positive Supply Current	I_{DD}	Logic Inputs = 0 V	10	µA max
Power Dissipation	P_{DISS}	Logic Inputs = 0 V	0.055	mW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	%/% max

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP1177 I-to-V converter amplifier. The AD5545 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All ac characteristic tests are performed in a closed-loop system using an O42 I-to-V converter amplifier.
[4] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

Parameter	Symbol	Conditions	5 V ± 10%	Units
AC CHARACTERISTICS				
Output Voltage Setting Time	t_S	To ±0.1% Full Scale, Data = Zero Scale to Full Scale to Zero Scale	0.5	µs typ
Reference Multiplying BW	BW	V_{REF} = 5 V p-p, Data = Full Scale	4	MHz typ
DAC Glitch Impulse	Q	V_{REF} = 0 V, Data = Zero Scale to Midscale to Zero Scale	7	nV-s typ
Feedthrough Error	V_{OUT}/V_{REF}	Data = Zero Scale, V_{REF} = 100 mV rms, f = 1 kHz, Same Channel	–65	dB
Digital Feedthrough	Q	$\overline{CS}$ = Logic High and f_{CLK} = 1 MHz	7	nV-s typ
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, Data = Full Scale, f = 1 kHz to 10 kHz	–85	dB typ
Analog Crosstalk	C_{TA}	V_{REFB} = 0 V, Measure V_{OUTB} with V_{REFA} = 5 V p-p Sine Wave, Data = Full Scale, f = 1 kHz to 10 kHz	–95	dB typ
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz	12	nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 2. AD5545/AD5555 Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	–0.3 V, +8 V
V_{REF} to GND	–18 V, +18 V
Logic Inputs to GND	–0.3 V, +8 V
V(I_{OUT}) to GND	–0.3 V, V_{DD} + 0.3 V
Input Current to Any Pin except Supplies	±50 mA
Package Power Dissipation	(T_J max – T_A)/ θ_{JA}
Thermal Resistance θ_{JA}	
16-Lead TSSOP	150°C/W
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature	
RU-16 (Vapor Phase, 60 sec)	215°C
RU-16 (Infrared, 15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

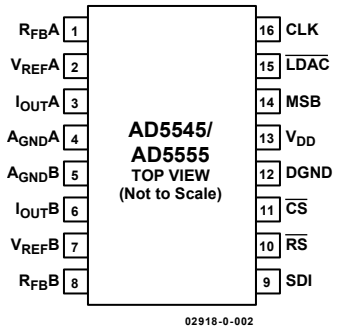

Figure 2. 16-Lead TSSOP

Table 3. Pin Function Descriptions—16-Lead TSSOP

Pin No.	Mnemonic	Function
1	$R_{FB}A$	Establish voltage output for DAC A by connecting to external amplifier output.
2	$V_{REF}A$	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. Pin can be tied to V_{DD} pin.
3	$I_{OUT}A$	DAC A Current Output.
4	$A_{GND}A$	DAC A Analog Ground.
5	$A_{GND}B$	DAC B Analog Ground.
6	$I_{OUT}B$	DAC B Current Output.
7	$V_{REF}B$	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. Pin can be tied to V_{DD} pin.
8	$R_{FB}B$	Establish voltage output for DAC B by connecting to external amplifier output.
9	SDI	Serial Data Input. Input data loads directly into the shift register.
10	$\overline{RS}$	RESET Pin, Active Low Input. Input registers and DAC registers are set to all 0s or midscale. Register Data = 0x0000 when MSB = 0. Register Data = 0x8000 for AD5545 and 0x2000 for AD5555 when MSB = 1.
11	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}$/$\overline{LDAC}$ returns high. This does not affect $\overline{LDAC}$ operation.
12	DGND	Digital Ground Pin.
13	V_{DD}	Positive Power Supply Input. Specified range of operation 5 V ± 10% or 3 V ± 10%.
14	MSB	MSB bit sets output to either 0 or midscale during a RESET pulse ($\overline{RS}$) or at system power-on. Output equals zero scale when MSB = 0 and midscale when MSB = 1. MSB pin can also be tied permanently to ground or V_{DD}.
15	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input. See Table 4 and Table 5 for operation.
16	CLK	Clock Input. Positive edge clocks data into shift register.

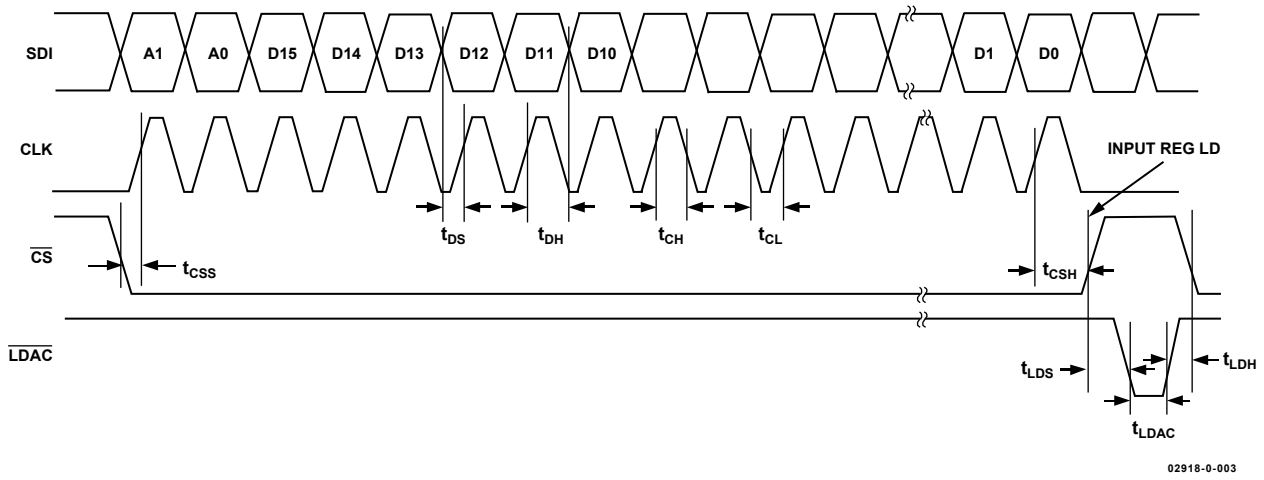

Figure 3. AD5545 18-Bit Data Word Timing Diagram

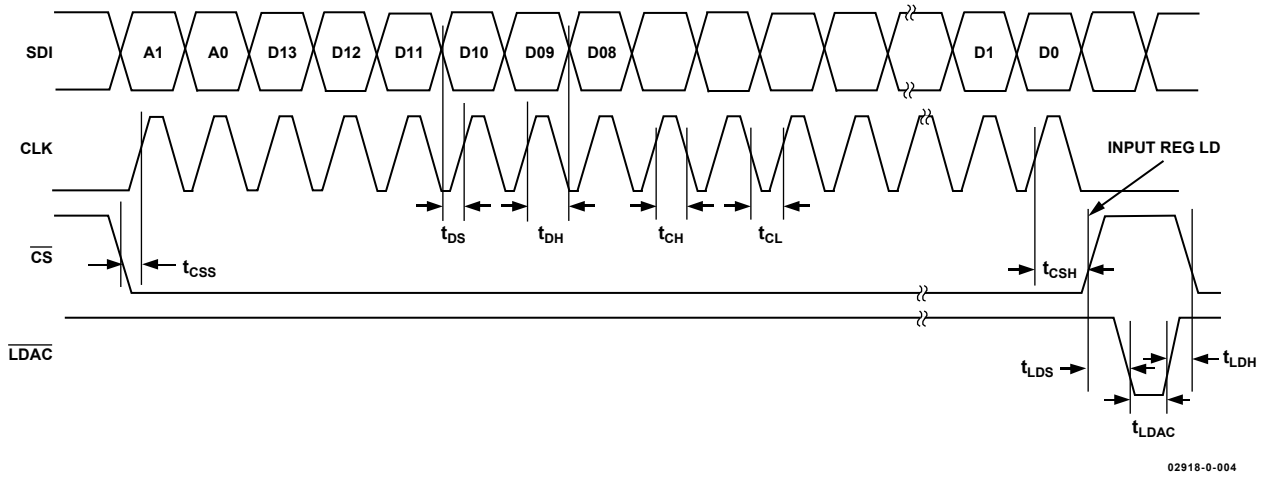

Figure 4. AD5555 16-Bit Data Word Timing Diagram

Table 4. AD5545 Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	↑+	H	H	X	Shift Register Data Advanced One Bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
↑+	L	H	H	X	No Effect	Selected DAC Updated with Current SR Current	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	↑+	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0x0000	Latched Data = 0x0000
H	X	H	L	H	No Effect	Latched Data = 0x8000	Latched Data = 0x8000

NOTES

1. SR = Shift Register, ↑+ = Positive Logic Transition, and X = Don't Care.
2. At power-on, both the input register and the DAC register are loaded with all 0s.

Table 5. AD5555 Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	↑+	H	H	X	Shift Register Data Advanced One Bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
↑+	L	H	H	X	No Effect	Selected DAC Updated with Current SR Current	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	↑+	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0x0000	Latched Data = 0x0000
H	X	H	L	H	No Effect	Latched Data = 0x2000	Latched Data = 0x2000

NOTES

1. SR = Shift Register, ↑+ = Positive Logic Transition, and X = Don't Care.
2. At power-on, both the input register and the DAC register are loaded with all 0s.

Table 6. AD5545 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

	MSB																	LSB
Bit Position	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note that only the last 18 bits of data clocked into the serial register (Address + Data) are inspected when the $\overline{CS}$ line's positive edge returns to logic high. At this point, an internally generated load strobe transfers the serial register data contents (Bits D15–D0) to the decoded DAC input register address determined by Bits A1 and A0. Any extra bits clocked into the AD5545 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 7. AD5555 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

	MSB															LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note that only the last 16 bits of data clocked into the serial register (Address + Data) are inspected when the $\overline{CS}$ line's positive edge returns to logic high. At this point, an internally generated load strobe transfers the serial register data contents (Bits D13–D0) to the decoded DAC input register address determined by Bits A1 and A0. Any extra bits clocked into the AD5555 shift register are ignored; only the last 16 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 8. Address Decode

A1	A0	DAC Decoded
0	0	None
0	1	DAC A
1	0	DAC B
1	1	DAC A and DAC B

TYPICAL PERFORMANCE CHARACTERISTICS

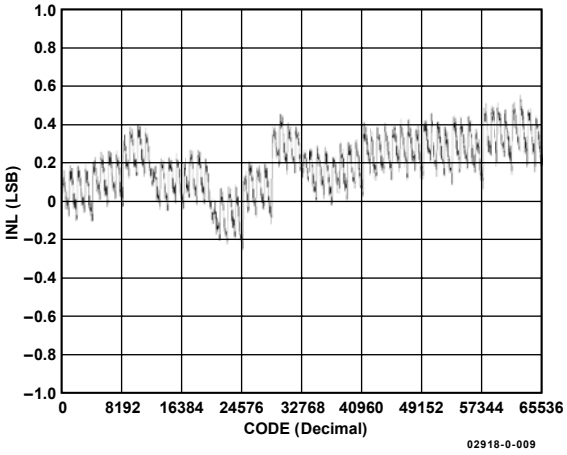

Figure 5. AD5545 Integral Nonlinearity Error

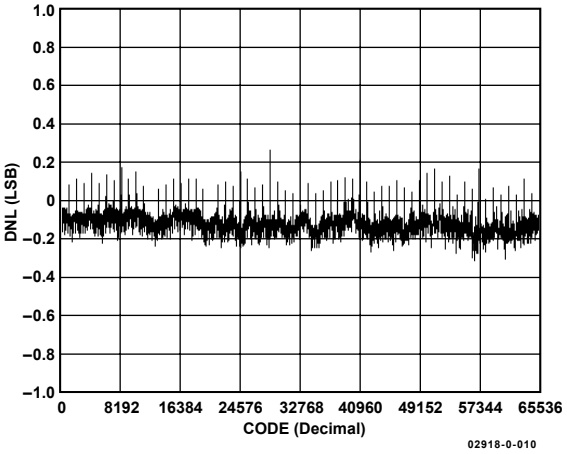

Figure 6. AD5545 Differential Nonlinearity Error

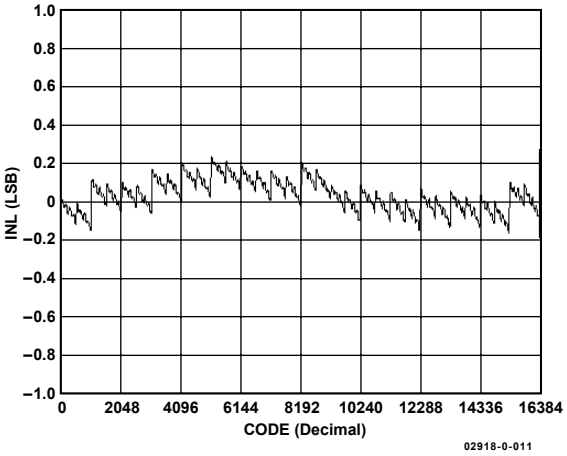

Figure 7. AD5555 Integral Nonlinearity Error

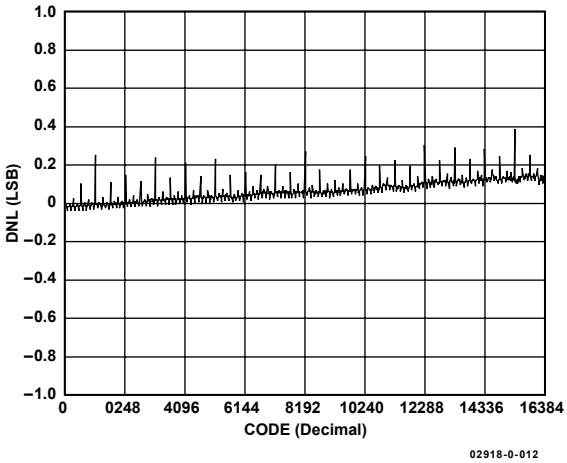

Figure 8. AD5555 Differential Nonlinearity Error

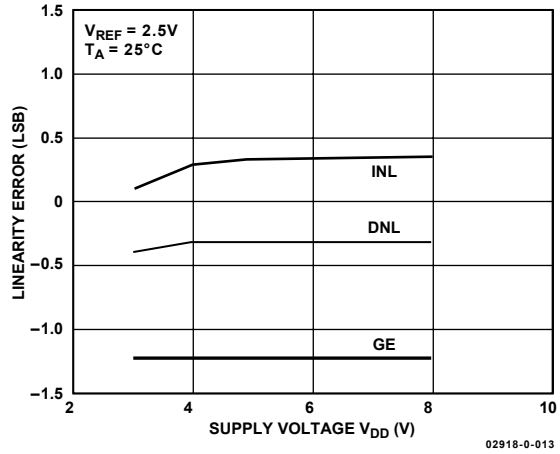

Figure 9. Linearity Errors vs. V_{DD}

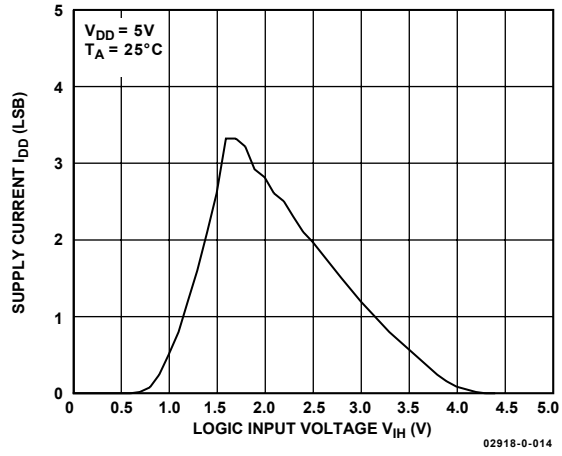

Figure 10. Supply Current vs. Logic Input Voltage

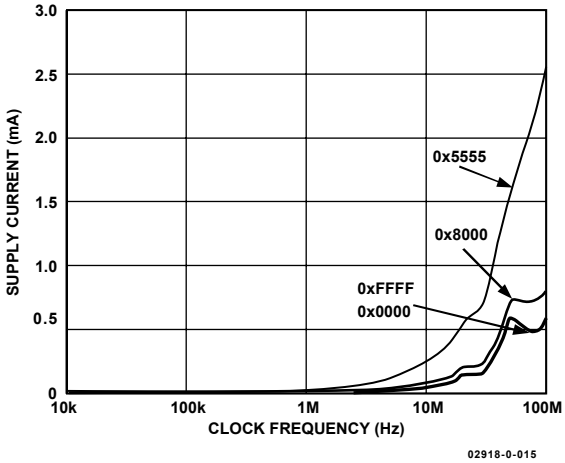

Figure 11. Supply Current vs. Clock Frequency

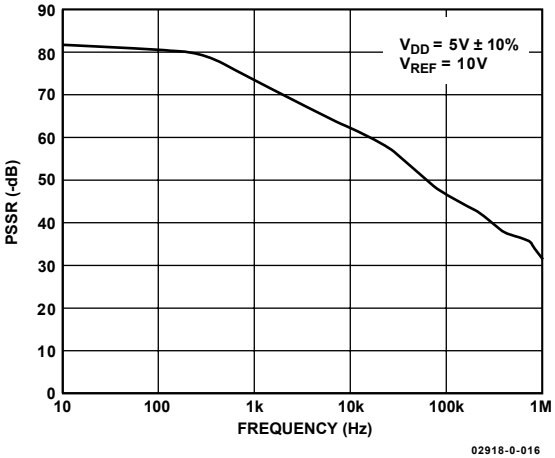

Figure 12. Power Supply Rejection Ration vs. Frequency

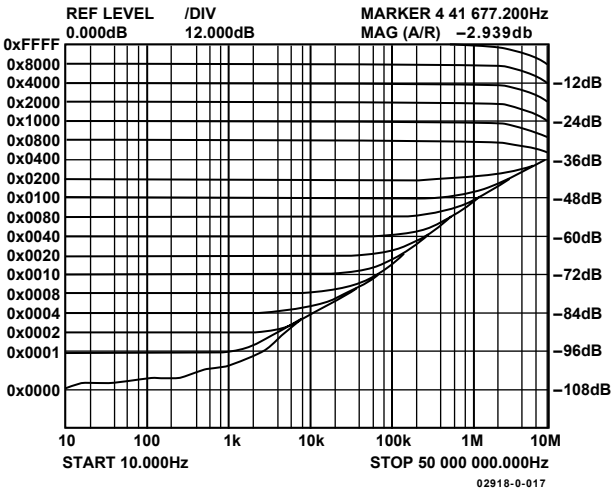

Figure 13. Reference Multiplying Bandwidth

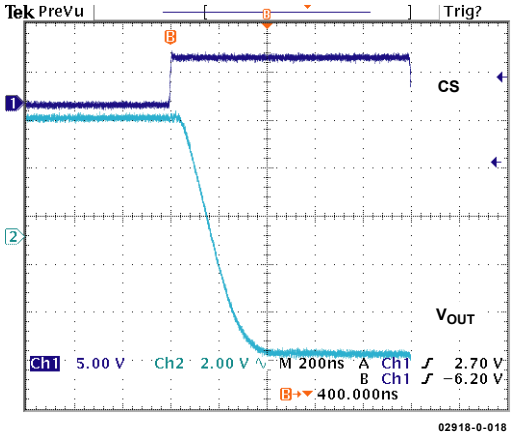

Figure 14. Settling Time

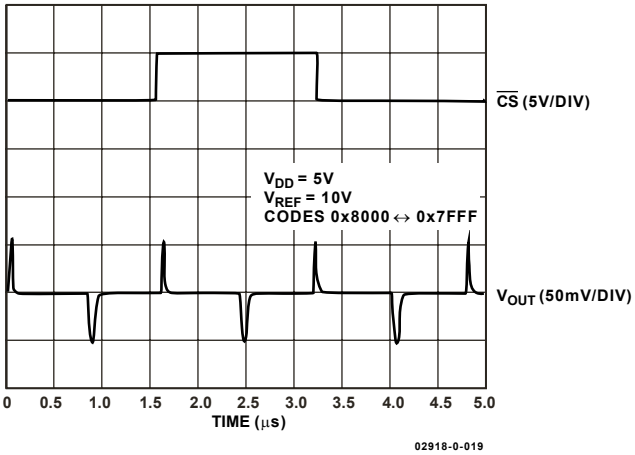

Figure 15. Midscale Transition and Digital Feedthrough

CIRCUIT OPERATION

The AD5545/AD5555 contain a 16-/14-bit, current-output, digital-to-analog converter, a serial-input register, and a DAC register. Both parts require a minimum of a 3-wire serial data interface with additional $\overline{\text{LDAC}}$ for dual channel simultaneous update.

D/A CONVERTER SECTION

The DAC architecture uses a current-steering R-2R ladder design. Figure 16 shows the typical equivalent DAC. The DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The R_{FB} pin is connected to the output of the external amplifier. The I_{OUT} terminal is connected to the inverting input of the external amplifier. These DACs are designed to operate with both negative or positive reference voltages. The V_{DD} power pin is used only by the logic to drive the DAC switches ON and OFF. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users attempt to measure the R_{FB} value, power must be applied to V_{DD} to achieve continuity. The V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register, according to Equation 1 and Equation 2, determine the DAC output voltage.

$$V_{OUT} = -V_{REF} \times D/65{,}536 \quad (1)$$

$$V_{OUT} = -V_{REF} \times D/16{,}384 \quad (2)$$

Note that the output full-scale polarity is the opposite of the V_{REF} polarity for dc reference voltages.

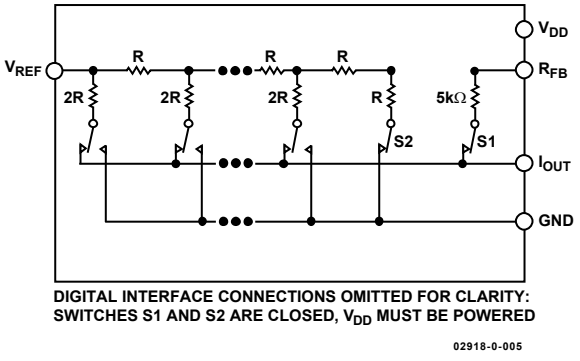

Figure 16. Equivalent R-2R DAC Circuit

These DACs are also designed to accommodate ac reference input signals. The AD5545/AD5555 will accommodate input reference voltages in the range of –12 V to +12 V. The reference voltage inputs exhibit a constant nominal input-resistance value of 5 kΩ, ±30%. The DAC output (I_{OUT}) is code dependent, producing various output resistances and capacitances. When choosing an external amplifier, the user should take into account the variation in impedance generated by the AD5545/AD5555 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise.

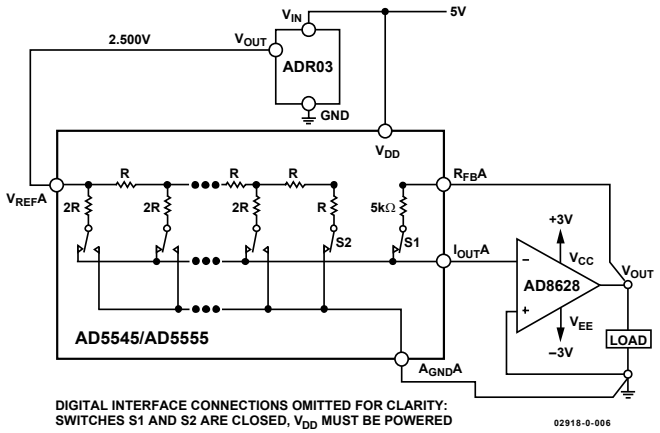

Figure 17. Recommended System Connections

SERIAL DATA INTERFACE

The AD5545/AD5555 use a minimum 3-wire ($\overline{\text{CS}}$, SDI, CLK) serial data interface for single channel update operation. With Table 4 as an example (AD5545), users can tie $\overline{\text{LDAC}}$ low and $\overline{\text{RS}}$ high, then pull $\overline{\text{CS}}$ low for an 18-bit duration. New serial data is then clocked into the serial-input register in an 18-bit data-word format with the MSB bit loaded first. Table 5 defines the truth table for the AD5555. Data is placed on the SDI pin and clocked into the register on the positive clock edge of CLK. For the AD5545, only the last 18-bits clocked into the serial register will be interrogated when the $\overline{\text{CS}}$ pin is strobed high, transferring the serial register data to the DAC register and updating the output. If the applied microcontroller outputs serial data in different lengths than the AD5545, such as 8-bit bytes, three right justified data bytes can be written to the AD5545. The AD5545 will ignore the six MSB and recognize the 18 LSB as valid data. After loading the serial register, the rising edge of $\overline{\text{CS}}$ transfers the serial register data to the DAC register and updates the output; during the $\overline{\text{CS}}$ strobe, the CLK should not be toggled.

If users want to program each channel separately but update them simultaneously, they need to program $\overline{\text{LDAC}}$ and $\overline{\text{RS}}$ high initially, then pull $\overline{\text{CS}}$ low for an 18-bit duration and program DAC A with the proper address and data bits. $\overline{\text{CS}}$ is then pulled high to latch data to the DAC A register. At this time, the output is not updated. To load DAC B data, pull $\overline{\text{CS}}$ low for an 18-bit duration and program DAC B with the proper address and data, then pull $\overline{\text{CS}}$ high to latch data to the DAC B register. Finally, pull $\overline{\text{LDAC}}$ low and then high to update both the DAC A and DAC B outputs simultaneously.

Table 8 shows that each DAC A and DAC B can be individually loaded with a new data value. In addition, a common new data value can be loaded into both DACs simultaneously by setting Bit A1 = A0 = high. This command enables the parallel combination of both DACs, with $I_{OUT}A$ and $I_{OUT}B$ tied together, to act as one DAC with significant improved noise performance.

ESD Protection Circuits

All logic input pins contain back-biased ESD protection Zeners connected to digital ground (DGND) and V_{DD} as shown in Figure 18.

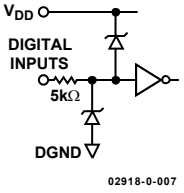

Figure 18. Equivalent ESD Protection Circuits

POWER-UP SEQUENCE

It is recommended to power-up V_{DD} and ground prior to any reference voltages. The ideal power-up sequence is $A_{GND}X$, DGND, V_{DD}, $V_{REF}X$, and digital inputs. A noncompliance power-up sequence can elevate reference current, but the device will resume normal operation once V_{DD} is powered.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The input leads should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 μF to 0.1 μF disc or chip ceramic capacitors. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at V_{DD} to minimize any transient disturbance and to filter any low frequency ripple (see Figure 19). Users should not apply switching regulators for V_{DD} due to the power supply rejection ratio degradation over frequency.

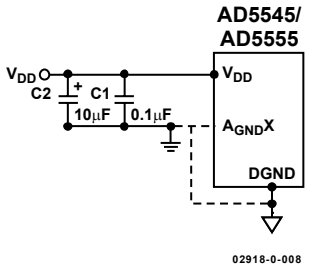

Figure 19. Power Supply Bypassing and Grounding Connection

GROUNDING

The DGND and $A_{GND}X$ pins of the AD5545/AD5555 refer to the digital and analog ground references. To minimize the digital ground bounce, the DGND terminal should be joined remotely at a single point to the analog ground plane (see Figure 19).

APPLICATIONS

STABILITY

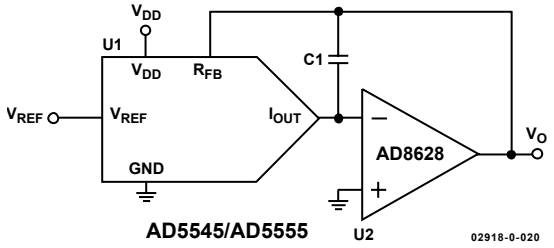

Figure 20. Operational Compensation Capacitor for Gain Peaking Prevention

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP, and if there is excessive parasitic capacitance at the inverting node.

An optional compensation capacitor, C1, can be added for stability as shown in Figure 20. C1 should be found empirically, but 20 pF is generally more than adequate for the compensation.

POSITIVE VOLTAGE OUTPUT

To achieve the positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistors' tolerance errors. To generate a negative reference, the reference can be level shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and –2.5 V, respectively (see Figure 21).

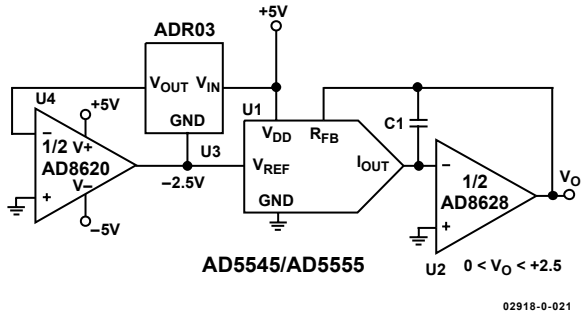

Figure 21. Positive Voltage Output Configuration

BIPOLAR OUTPUT

The AD5545/AD5555 is inherently a 2-quadrant multiplying D/A converter. It can easily set up for unipolar output operation. The full-scale output polarity is the inverse of the reference input voltage.

In some applications, it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished by using an additional external amplifier, U4, configured as a summing amplifier (see Figure 22). In this circuit, the second amplifier, U4, provides a gain of +2, which increases the output span magnitude to 5 V. Biasing the external amplifier with a 2.5 V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created because the input data (D) is incremented from code zero (V_{OUT} = –2.5 V) to midscale (V_{OUT} = 0 V) to full scale (V_{OUT} = +2.5 V).

$$V_{OUT} = (D/32{,}768 - 1) \times V_{REF} \quad (AD5545) \tag{3}$$

$$V_{OUT} = (D/16{,}384 - 1) \times V_{REF} \quad (AD5555) \tag{4}$$

For the AD5545, the external resistance tolerance becomes the dominant error that users should be aware of.

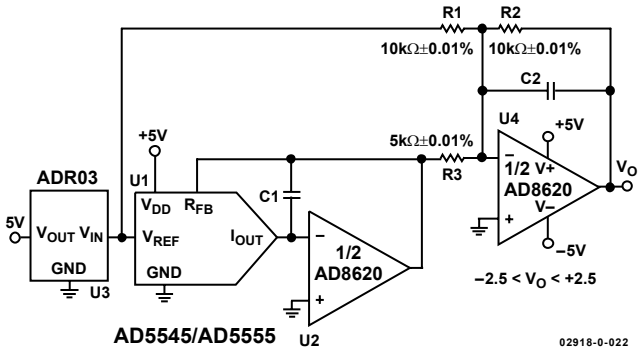

Figure 22. Four-Quadrant Multiplying Application Circuit

PROGRAMMABLE CURRENT SOURCE

Figure 23 shows a versatile V-to-I conversion circuit using improved Howland Current Pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. This circuit can be used in a 4 mA to 20 mA current transmitter with up to a 500 Ω of load. In Figure 23, it shows that if the resistor network is matched, the load current is

$$I_L = \frac{\frac{(R2+R3)}{R1}}{R3} \times \mathrm{V_{REF}} \times \mathrm{D} \tag{5}$$

$R3$, in theory, can be made small to achieve the current needed within the U3 output current driving capability. This circuit is versatile such that the AD8510 can deliver ±20 mA in both directions, and the voltage compliance approaches 15 V, which is mainly limited by the supply voltages of U3. However, users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes

$$Z_O = \frac{R1'R3(R1+R2)}{R1(R2'+R3') - R1'(R2+R3)} \tag{6}$$

If the resistors are perfectly matched, Z_O is infinite, which is desirable, and the resistors behave as an ideal current source. On the other hand, if they are not matched, Z_O can be either positive or negative. The latter can cause oscillation. As a result, C1 is needed to prevent the oscillation. For critical applications, C1 could be found empirically but typically falls in the range of a few pF.

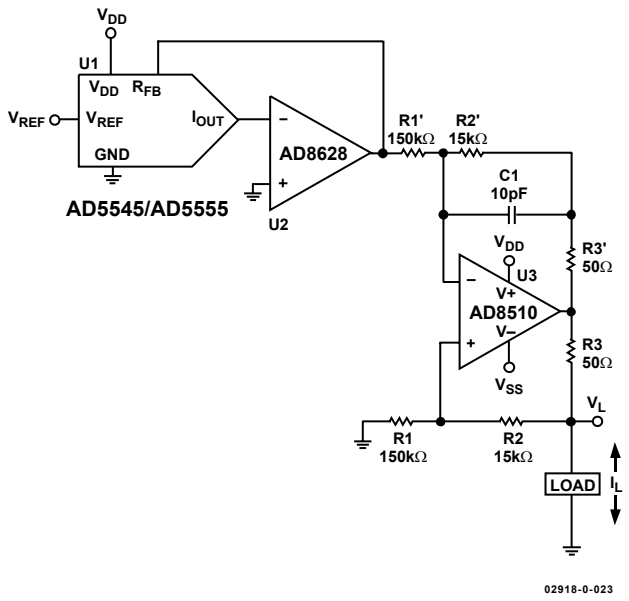

Figure 23. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities

DAC WITH PROGRAMMABLE INPUT REFERENCE RANGE

Since high voltage references can be costly, users may consider using one of the DACs, a digital potentiometer, and a low voltage reference to form a single-channel DAC with a programmable input reference range. This approach optimizes the programmable range as well as facilitates future system upgrades with just software changes. Figure 24 shows this implementation. $V_{REF}AB$ is in the feedback network, therefore,

$$V_{REF}AB = V_{REF} \times \left(1 + \frac{R_{WB}}{R_{WA}}\right) - \left(-V_{REF\_AB} \times \frac{D_A}{2^N} \times \frac{R_{WB}}{R_{WA}}\right) \quad (7)$$

where:

$V_{REF}AB$ = Reference Voltage of V_{REF}A and V_{REF}B

V_{REF} = External Reference Voltage

D_A = DAC A Digital Code in Decimal

N = Number of Bits of DAC

R_{WB} and R_{WA} are digital potentiometer 128-step programmable resistances and are given by

$$R_{WB} \approx \frac{D_C}{128} R_{AB} \quad (8)$$

$$R_{WA} \approx \frac{128 - D_C}{128} R_{AB} \quad (9)$$

$$\frac{R_{WB}}{R_{WA}} \approx \frac{D_C}{128 - D_C} \quad (10)$$

where D_C = Digital Potentiometer Digital Code in Decimal ($0 \le D_C \le 127$).

By putting Equations 7 through 10 together, the following results:

$$V_{REF}AB = V_{REF} \times \frac{\left(1 + \frac{D_C}{128 - D_C}\right)}{1 - \frac{D_A}{2^N} \times \frac{D_C}{128 - D_C}} \quad (11)$$

Table 9 shows a few examples of V_{REF}AB of the 14-bit AD5555.

Table 9. V_{REF}AB vs. D_B and D_C of the AD5555

D_C	D_A	V_{REF}AB
0	X	V_{REF}
32	0	1.33 V_{REF}
32	8192	1.6 V_{REF}
64	0	2 V_{REF}
64	8192	4 V_{REF}
96	0	4 V_{REF}
96	8192	−8 V_{REF}

The output of DAC B is, therefore,

$$V_{OB} = -V_{REF}AB \frac{D_B}{2^N} \quad (12)$$

where D_B is the DAC B digital code in decimal.

The accuracy of $V_{REF}AB$ will be affected by the matching of the input and feedback resistors and, therefore, a digital potentiometer is used for U4 because of its inherent resistance matching. The AD7376 is a 30 V or ±15 V, 128-step digital potentiometer. If 15 V or ±7.5 V is adequate for the application, a 256-step AD5260 digital potentiometer can be used instead.

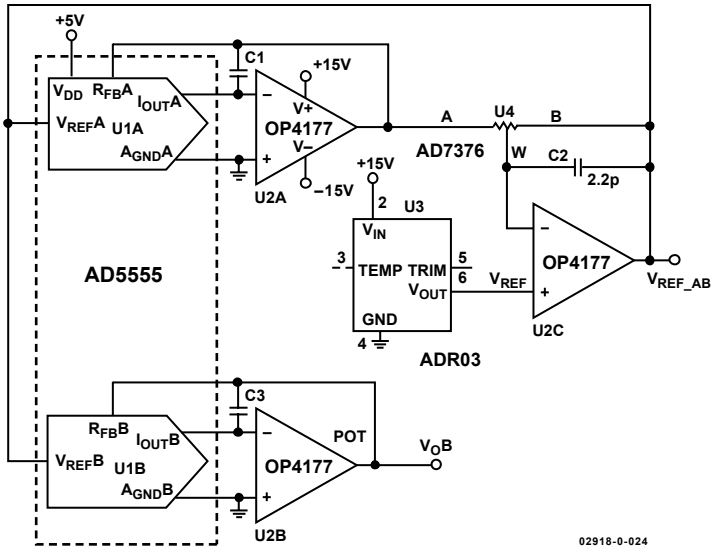

Figure 24. DAC with Programmable Input Reference Range

OUTLINE DIMENSIONS

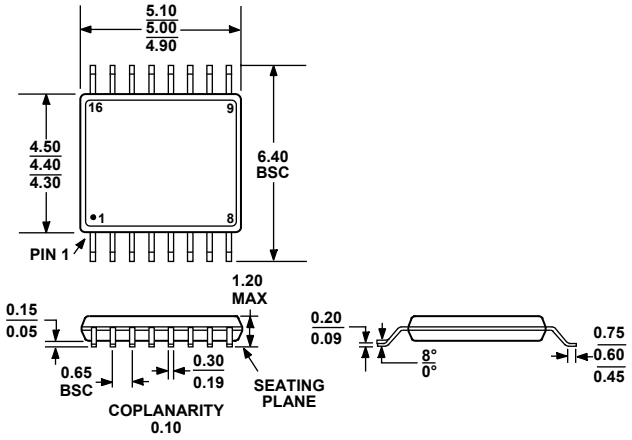

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)—Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

AD5545/AD5555 Products	INL LSB	DNL LSB	RES (Bits)	Temperature Range	Package Description	Package Outline	Qty
AD5545BRU*	±2	±1	16	–40°C to +85°C	TSSOP-16	RU–16	96
AD5545BRU–REEL7	±2	±1	16	–40°C to +85°C	TSSOP-16	RU–16	1000
AD5555CRU	±1	±1	14	–40°C to +85°C	TSSOP-16	RU–16	96
AD5555CRU–REEL7	±1	±1	14	–40°C to +85°C	TSSOP-16	RU–16	1000

*The AD5545/AD5555 contain 3131 transistors. The die size measures 71 mil. × 96 mil., 6816 sq. mil.