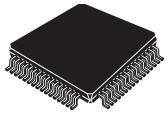
STLC5048

Fully programmable four-channel codec and filter

Features

- Fully programmable monolithic 4-channel codec/filter
- Single +3.3 V supply
- A/m law programmable
- Linear coding (16 bits) option
- PCM highway format automatically detected: 1.536 or 1.544 MHz, 2.048, 4.096, 8192 MHz
- Two PCM ports available
- TX gain programming: 33 dB range; <0.01 dB step
- RX gain programming: 42 dB range; <0.01 dB step
- Programmable SLIC input impedance
- Programmable transhybrid balance filter
- Programmable equalization (frequency response)
- Programmable time slot assignment
- Digital and analog loopbacks
- SLIC control port static (16 I/Os), dynamic (12 I/Os + 4 CS)
- Built-in test mode with tone generation, MCU access to PCM data
- 64 TQFP (10x10mm) package
- Programmable SLIC line current limitation
- Programmable SLIC off-hook detection threshold



TQFP64 (10x10x1.4mm)

Description

The STLC5048 is a monolithic fully programmable 4-channel codec and filter. It operates with a single +3.3V supply.

The analog interface is based on a receive output buffer driving the SLIC RX input and on an amplifier input stage normally driven by the SLIC TX output. Due to the single supply voltage a mid-supply reference level is generated internally by the device and all analog signals are referred to this level (AGND). The PCM interface uses one common 8 kHz frame sync. pulse for transmit and receive direction. The bit clock is automatically detected between four standards: 1.563/1.544 MHz, 2.048 MHz, 4.096 MHz, 8192 MHz.

Two PCM port are provided: the channels can be connected to port A or/and B.

Device programmability is achieved by means of several registers and commands allowing to set the different parameters like TX/RX gains, line impedance, transhybrid balance, equalization (frequency response), encoding law (A/m), time slot assignment, independent channels power up/down, loopbacks, PCM bits offset.

The STLC5048 can be programmed via serial interface running up to 8 MHz. One interrupt output pin is also provided.

A GUI interface is also available to emulate and program the coefficients for impedance synthesis, echo cancelling and channel filtering.

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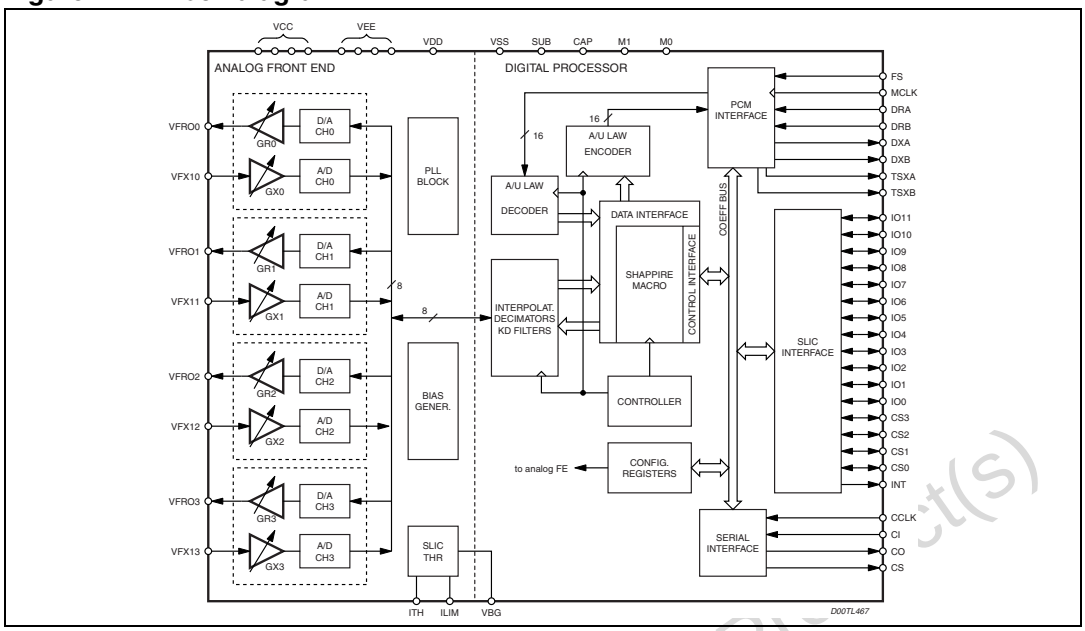
Figure 1. Block diagram



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to V_{EE}	4.6	V
V_{DD}	V_{DD} to V_{SS}	4.6	V
VD_{IN}	Digital input pin voltage	5.5	V
VAin	Analog input pin voltage (V_{DD}=V_{CC}; V_{EE}=V_{SUB})	V_{CC} + 0.5; V_{EE} - 0.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{LEAD}	Lead temperature (soldering, 10s)	300	°C

Table 2. Operating range

Symbol	Parameter	Value	Unit
V_{CC} , V_{DD}	Supply voltage	3.3 +/- 5%	V
T_{OP}	Operating temperature range	-40 to +85	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	70	°C/W

3 Pin assignments and descriptions

Figure 2. Pin assignments (top view)

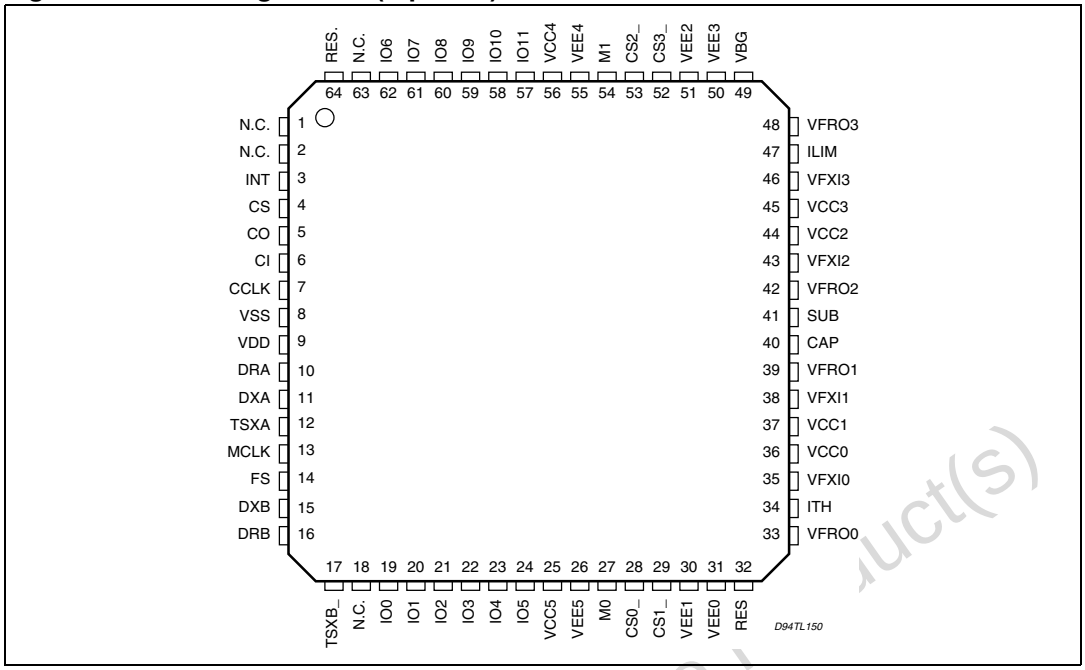


Table 4. I/O definitions

Type	Definition
AI	Analog input
AO	Analog output
ODO	Open drain output
DI	Digital input
DO	Digital output
DIO	Digital input / output
DTO	Digital tristate output
DPS	Digital power supply
APS	Analog power supply

Table 5. Pin descriptions

No.	Name	Type	Description
Analog pins			
33	VFRO0	AO	Receive analog amplifier output channel 0. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
39	VFRO1	AO	Receive analog amplifier output channel 1. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
42	VFRO2	AO	Receive analog amplifier output channel 2. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
48	VFRO3	AO	Receive analog amplifier output channel 3. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
35	VFXI0	AI	TX input amplifier channel 0. Typ 1MΩ input impedance
38	VFXI1	AI	TX input amplifier channel 1. Typ 1MΩ input impedance
43	VFXI2	AI	TX input amplifier channel 2. Typ 1MΩ input impedance
46	VFXI3	AI	TX input amplifier channel 3. Typ 1MΩ input impedance
40	CAP		AGND voltage filter pin: a 100 nF capacitor must be connected between ground and this pin.
34	ITH	AO	SLIC off-hook detection threshold.
47	ILIM	AO	SLIC line current limitation.
49	VBG	AI	SLIC VBG reference for DC characteristics programmability.
Power supply			
25,36, 37,44, 45,56	VCC0..5	APS	Total 6 pins: 3.3 V analog power supplies, should be shorted together, require 100 nF decoupling capacitor to VEE.
26,30, 31,50, 51,55	VEE0..5	APS	Total 6 pins: analog ground, should be shorted together.
9	VDD	DPS	Digital power supply 3.3 V, require 100 nF decoupling capacitor to VSS.
8	VSS	DPS	Digital ground.
41	SUB	DPS	Substrate connection. Must be shorted together with VEE and VSS pins.
Digital pins			
27 54	M0 M1	DI	Mode select: M1 M0 Mode select 0 0 Reset status 1 0 Normal operation 0 1 Not allowed 1 1 Not allowed
14	FS	DI	Frame sync. Pulse. A pulse or a square waveform with an 8 kHz repetition rate is applied to this pin to define the start of the receive and transmit frame. Effective start of the frame can be then shifted of up to 7 clock pulses independently in receive and transmit directions by proper programming of the PCMSH register.

Table 5. Pin descriptions (continued)

No.	Name	Type	Description
13	MCLK	DI	Master clock input. Four possible frequencies can be used: 1.536/1.544 MHz; 2.048 MHz; 4.096 MHz; 8.192 MHz. The device automatically detect the frequency applied. This signal is also used as bit clock and it is used to shift data into and out of the DRA/B and DXA/B pins.
12	TSXA	ODO	Transmit time slot (open drain output, 3.2mA). Normally it is floating in high impedance state except when a time slot is active on the DXA output. In this case TSXA output pulls low to enable the backplane line driver.
11	DXA	DTO	Transmit PCM interface A. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.
10	DRA	DI	Receive PCM interface A. It remains inactive except during the assigned receive time slots during which the PCM data byte is shifted in on the falling edge of MCLK.
24	IO5	DIO	General control I/O pin #5. Can be programmed as input or output via DIR register. Depending on content of CONF register can be a static input/output or a dynamic input/output synchronized with the CSn output signals controlling the SLICs.
62	IO6	DIO	General control I/O pin #6. (see IO5 description).
61	IO7	DIO	General control I/O pin #7. (see IO5 description).
60	IO8	DIO	General control I/O pin #8. (see IO5 description).
59	IO9	DIO	General control I/O pin #9. (see IO5 description).
58	IO10	DIO	General control I/O pin #10. (see IO5 description).
57	IO11	DIO	General control I/O pin #11. (see IO5 description).
19	IO0	DIO	General control I/O pin #0. (see IO5 description).
20	IO1	DIO	General control I/O pin #1. (see IO5 description).
21	IO2	DIO	General control I/O pin #2. (see IO5 description).
22	IO3	DIO	General control I/O pin #3. (see IO5 description).
23	IO4	DIO	General control I/O pin #4. (see IO5 description).
28	CS0	DIO	SLIC CS control #0. Depending on CONF reg. content can be a CS output for SLIC #0 or a static I/O. When configured as CS output it is automatically generated by the CODEC with a repetition time of 31.25ms. In this mode also the IO0..11 are synchronized and carry proper data in and out synchronous with CS. When configured as static I/O, the direction is defined by CSDIR register content.
29	CS1	DIO	SLIC CS control #1, (see CS0 description).
53	CS2	DIO	SLIC CS control #2, (see CS0 description).
52	CS3	DIO	SLIC CS control #3, (see CS0 description).

Table 5. Pin descriptions (continued)

No.	Name	Type	Description
4	CS	DI	Chip select input, when this pin is low control information can be written to or read from the device via the CI and CO pins.
7	CCLK	DI	Clock of serial control bus. this clock shifts serial control information into or out of CI or CO when CS input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks.
6	CI	DI	Control data input of serial control bus. Control data is shifted in the device when CS is low and clocked by CCLK. Depending on the addressed register different numbers of consecutive bytes can be loaded.
5	CO	DI	Control data output of serial control bus. Control data is shifted out the device when CS is low and clocked by CCLK. Depending on the addressed register different numbers of consecutive bytes can be shifted out.
3	INT	ODO	Interrupt output (open drain), goes low when a data change has been detected in the I/O pins or another interrupt source is active. One mask register allows to mask any I/O pin. Interrupt is reset when the I/O register is read.
17	TSXB	ODO	Transmit time slot (open drain output, 3.2 mA). Normally it is floating in high impedance state except when a time slot is active on the DXB output. In this case TSXB output pulls low to enable the backplane line driver.
15	DXB	DTO	Transmit PCM interface B. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.
16	DRB	DI	Receive PCM interface B. It remains inactive except during the assigned receive time slots during which the PCM data byte is shifted in on the falling edge of MCLK.
Not connected			
2, 18, 63, 1	N.C.		Not connected, must be left open
32, 64	RES		Reserved pins, must be connected to ground

4 Functional description

The STLC5048 is a fully programmable device with embedded ROM and RAM. The ROM is used to contain the default state coefficients for the programmable filters, while the RAM is used to load the desired coefficient values.

4.1 Power on initialization

When power is first applied it is recommended to reset the device (M1=M0=0) in order to set all the internal registers to the reset value (see *Chapter 5: Register description*; this means also power down mode for all the four channels and SW reset bit (RES) set in the CONF register.

When the RES bit is set, the only instructions allowed are the one that disable this bit and the REACOM instruction: all other instructions are ignored. It is not possible to disable the RES bit and write the other bits of the CONF register with the same instruction.

Of course, RESET mode can be programmed also by writing the RES bit of the CONF register.

See *Appendix C: Power sequences* for the power up sequence.

During RESET condition all the I/On and CSn pins are set as inputs, DX is in high impedance and all VFROn are set to AGND. After the reset all registers are loaded with the reset value.

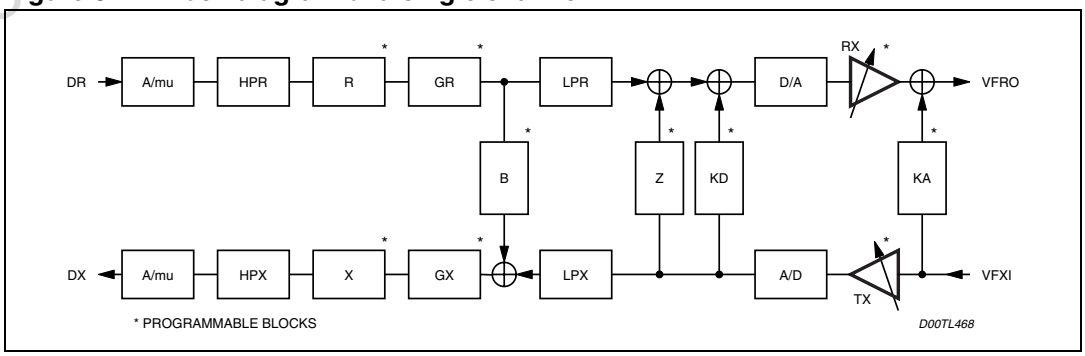
It means that the PCM interface and all the VFRO outputs are configured as described in the power down state, while no transmit or receive time slot are set.

Then, filters and gain blocks are configured with the coefficient defined in the default state.

4.2 Power down state

Each of the four channel may be put into power down mode by setting the appropriate bit in the CONF register. In this mode the eventual programmed DX channel is set in high impedance while the VFRO outputs are forced to AGND. When all the channels are set in power down mode the device enters the power down state: all the blocks related to the data processing are turned off, while the RAM is On or Off according to the PDR bit value in the COMEN register.

Figure 3. Block diagram of a single channel



4.3 Ringing state

This state can be used during the ringing phase in order to transmit a low frequency ringing signal (25-50 Hz). In order to obtain a 1 Vrms ringing signal at VFRO output a digital signal DR equal to -0.78 dBm0 must be provided.

This state means B, Z, X, KD and KA blocks equal to open circuits and the R block configured in order to obtain the maximum gain at the frequency of 25-50 Hz. During the ringing state if the TX time slot is enabled the idle PCM code is forced to DX.

To switch to this state, a bit (FR0..3) in the COEFST register must be set for every channel.

The programmed values for the previous blocks become active only when the FR and FD bits are reset.

If both FR and FD bits of a channel are set, the selected coefficient will be those of the ringing state.

4.4 Impedance synthesis

The impedance synthesis is performed by fully digital filters (Z and KD) and by an analog path (KA).

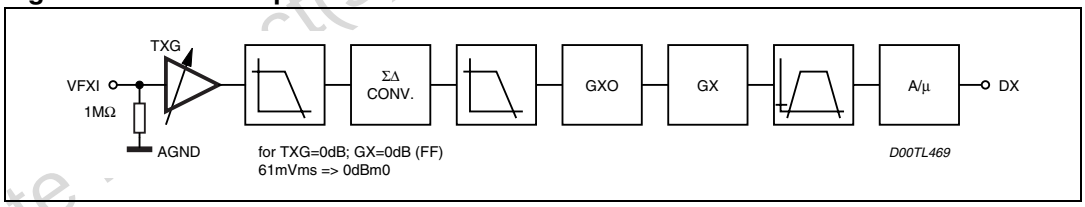
The Z, KD and KA filters report to the receive path the feedback signal coming from the transmit path. The coefficients of the Z, KD and KA filters are programmed via the ZFC, KD and AFE_CFF commands respectively.

4.5 Echo canceling

The trans-hybrid balance is performed by the digital programmable filter B.

The B filter reports to the transmit path the signal coming from the receive path. The coefficient of the B filter are programmed via the BFC command.

Figure 4. Transmit path



4.6 Transmit path

The transmit section input consist of the input amplifier, the A/D converter, the equalization filter X, the gain block GX, the encoder and the channel filters (LPX and HPX).

The input amplifier is provided of a programmable gain with a typical input impedance of 1MΩ The amplifier gain can be programmed with two different values (0 dB, +3.52dB) by means of the TXG register.

VFXI input must be AC coupled to the signal; the voltage swing allowed is 1.4 Vpp when the preamplifier gain is set to 0 dB and 0.93 Vpp when the gain is 3.52 dB; higher levels must be reduced through proper dividers.

Following the input amplifier the signal is converted into digital domain and a X filter block is programmed to equalize together with the HPX and LPX filters the frequency response. The coefficients of the X filter are programmed via the XFC command.

A gain block (GX) allows to set the transmit level in a 30 dB range, with steps <0.01 dB. This block can be programmed via the GTX command.

The needed TX gain can be set by proper programming of the GX block in combination with the TX amplifier.

Setting GTX=00h, the transmitted signal is muted and an idle PCM signal is generated on DX.

Concerning the CODING function, A/m law can be selected writing the CONF register (bit 5 AMU). In addition, via the CONF register (bit 6 LIN) the coding law can be set to linear mode (16 bits). In this case the signal sent on the DX will take two adjacent PCM channels, proper care has to be taken in the time slot selection programming (DXTS register).

The intrinsic non-programmable gain GX0 set the TX path gain to 22.07 dB. The absolute gain level (see *Chapter 9: Electrical characteristics*) refers to this intrinsic gain.

4.7 Receive path

The receive path of the STLC5048 consists of the decoder section, the gain block GR, the R filter, the channel filters (LPR, HPR) the D/A converter and the output amplifier.

Concerning the DECODING function, A/m law can be selected writing the CONF register (bit 5 AMU). In addition via the CONF register (bit 6 LIN) the coding law can be set to linear mode (16 bits).

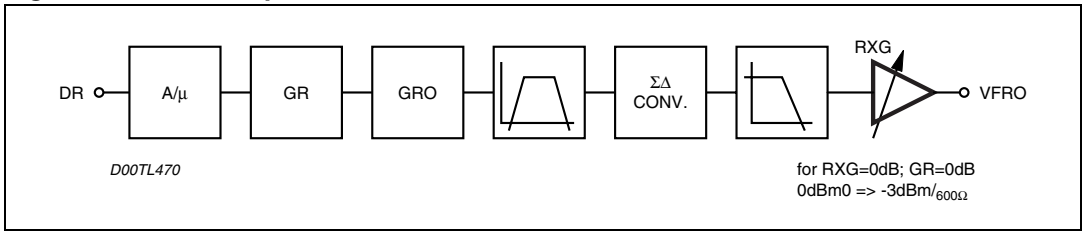
In this case the signal received on the DR input will take two adjacent PCM channels, proper care has to be taken in the time slot selection programming (DRTS register).

The gain block GR is controlled by the GRX command allowing 30 dB gain range in 0.01 dB steps.

The R filter together the channel filters (LPR and HPR) performs the line equalization. The coefficients of the R filter are programmed via the RFC command.

The signal is converted in the analog domain and amplified by the RX amplifier that can be programmed with four different values (mute, 0 dB, -6 dB and -12 dB) by means of RXG register.

Figure 5. Receive path



VFRO output, referred to AGND must be AC coupled to the load, referred to VSS, to prevent a DC current flow.

In order to get the best noise performances it is recommended to keep GRX value as close as possible to the maximum (FFh) setting properly the additional attenuation by means of RXG.

The intrinsic non programmable gain GR0 set the RX path gain to -3.15dB. The absolute gain level (see *Chapter 9: Electrical characteristics*) refers to this intrinsic gain.

4.8 PCM interface

The STLC5048 dedicates eight pins to the interface with the PCM highways.

MCLK represents the bit clock and is also used by the device as a source for the clock of the internal PLL.

Five possible frequencies can be used: 1.536/1.544 MHz (24-channel PCM frame); 2048 MHz (32-channel PCM frame); 4.096 MHz (64-channel PCM frame); 8.192 MHz (128 channels PCM frame). The operating frequency is automatically detected by the device the first time both MCLK and FS are applied and becomes active after the second FS period. MCLK synchronizes both the transmit data (DXA/B) and the receive data (DRA/B).

The Frame Synchronization signal FS is the common time base for all the four channels.

Transmit and receive programmable time-slots are framed by an internal synchronization signal that can be coincident with FS or delayed of 1 or 7 MCLK cycles depending on the programming of PCMSH register.

Two PCM ports are available: every channel can be connected to a different PCM port by means of PCMCOM register.

DXA/B represents the transmit PCM interface. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising/falling edge of MCLK according to the TE bit of PCMCOM register. The four channels can be shifted out in any possible time slot as defined by the DXTS registers. The assigned time slot (transmit and receive) takes place in the 8 MCLK cycles following the rising edge of FS.

The data can be shifted out on port A and/or B according to PCMCOM register.

If one codec is set in power down by software programming, the corresponding time slot is set in high impedance. When linear coding mode is selected by CONF register programming, the output channel will need two consecutive time slots (see *Chapter 5: Register description*).

DRA/B represents the receive PCM interface. It remains inactive except during the assigned time slots during which the PCM data byte is shifted in on the falling edge of MCLK. The four channels are shifted in any possible time slot as defined by the DRTS registers.

If one codec is set in power down by software programming, the corresponding time slot is not loaded and the VFRO output is kept at steady AGND level.

Table 6. Instruction byte structure

First byte (address or command ID)								Following bytes (data)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
R/W	I6	I5	I4	I3	I2	I1	I0	D7	D6	D5	D4	D3	D2	D1	D0

R/$\overline{W}$=0: Write operation

R/$\overline{W}$=1: Read operation

I6..I0: Instruction identifier: it can be a register address or a command identifier.

The number of data bytes depends on the instruction type. The first bit of a byte is the MSB, the first byte of an instruction is the LSByte.

When linear coding mode is selected by CONF register programming the input channel will need two consecutive time slots (see *Chapter 5: Register description*).

The data can be shifted in from port A or B according to the PCMCOM register.

TSXA/B represents the transmit time slot (open drain output, 3.2 mA). Normally it is floating in high impedance state except when a time slot is active on the DXA/B output. In this case TSXA/B output pulls low to enable the backplane line driver. Should be strapped to VSS when not used.

Finally by means of the LOOPB register it is possible to implement a digital or analog loopback on any of the selected channels.

4.9 MCU control interface

The MCU serial control interface consists of the following four pins:

- CCLK: control clock
- CI: serial data in
- CO: serial data out
- CS: chip select input

Control instructions require at least two bytes: however two single byte instructions are also provided.

In the multiple byte instructions the first one specifies the command or the register address and the access type (read or write).

The following bytes contain the data to be loaded into the internal RAM (on CI wire) or carry out the RAM content (on CO wire) depending on the R/W bit of the first byte. CO wire is normally in high impedance and goes to low impedance only after the first byte in case of read operation. This allows to use a common wire for both CI/CO.

CS, normally high, is set low during the transmission/reception of a byte, lasting 8 CCLK pulses. Between two consecutive access, the CS must be set high.

The CCLK can be a continuous or a gated clock.

The result of any instruction (read/write operation), if negative, can generate an interrupt (maskable). The interrupt register (INT) contains the cause information of the generated interrupt and it is cleared every time that it is read.

Depending on the instruction specified in the first byte, the STLC5048 waits a defined number of data bytes. If the STLC5048 doesn't receive the data byte within a predefined

period specified by means of T_OUT command, an internal time out rejects the instruction. The time-out time is verified between two consecutive MCU interface access (between the falling edge of the CS and the following rising edge).

This feature is used to verify the synchronization of the MCU interface: however it can be disabled if not desired (see T_OUT register description). To check this synchronization is provided a specific register (SYNCK) that returns always a predefined value: if the returned value is different the MCU interface is in out of sync state (the device is waiting a data byte while the MCU is writing an address or vice versa). In this case, it is possible to realign it by means of the execution of a specific single byte instruction (REACOM) from 1 to 53 times, depending on the instructions.

Every time an illegal operation (access to not allowed address, time-out violation or clock pulse different than 8 inside a CS active) is performed the MCU interface is put on an error state: to resume it from this state a single REACOM instruction can be used.

Anyway after a REACOM instruction a successful SYNC instruction guarantees the correct synchronization.

One additional wire provided to the control interface is an open drain interrupt output (INT) that goes low when a change of status is detected on the I/O pins or other interrupt source are active (see *Section 5.7: Interrupt register (INT)*). INT is automatically reset after reading of the register corresponding the cause that has generated the interrupt (see INT register description).

A particular register (COMEN) allows to enable a command on different channel at the same time. Every time a command operation is performed at least one channel must be enabled in this register.

This feature is useful when all channels must be configured in the same condition. When a command is used to perform a read operation only one channel can be enabled at the same time.

To check the configuration of the device a checksum value is provided. This value is calculated on all coefficient parameters entered (coefficients of KD, AFE_CFF, GRX, GTX, RFC, XFC, BFC, ZFC blocks; see the CKSUM register description). Two commands are required to get this value: the first one (CKSTART) starts the internal checksum calculation, the second one (CKSUM) returns the calculated value. Between this two commands no other operation are allowed. The checksum value is available within 400us the CKSTART command.

Coefficient checksum is defined by the following algorithm: $X^{16} + X^{12} + X^5 + 1$

This algorithm guarantees a fault coverage of $1 - 2^{-16}$.

4.10 Programming the device

After the power up, the filters and gain blocks can be programmed also with all the channels set in power down. in this case the PDR bit of the COMEN register must be set to 0.

With the proper setting of the COMEN register, the commands can be applied to more than one channel at the same time.

To read the coefficient values loaded in the RAM, only one channel per time must be enabled in the COMEN register.

4.11 SLIC control interface

The device provides 12 I/O pins and 4 CS signals. The interface can work in dynamic or static mode. This can be selected by means of STA bit of the CONF register:

- Dynamic mode: the I/O pins are configured as input or output by means of DIR register. The CS signals are used to select the different SLIC interface. In this case the I/O pin can be multiplexed. The data loaded from SLIC #n via I/O pins configured as input can be read in the DATAn register. The data written in a DATAn register will be loaded on the I/O pins configured as output when the CSn signal will be active.
- Static mode: The CS signal can be used as I/O pins. They can be configured as input or output I/O by means of DATA1 register. The data corresponding to the CS signal can be read or written by means of DATA2 register. All data related to the other I/O pins can be read or written by means of DATA0 register.

4.12 DC SLIC programmability

Three additional pins are used to select the on-hook/off-hook detection threshold and the line card limitation of the STLC3080 SLIC. This two values are programmed by ILIM and ITH registers. The programming of these two registers must be done before the filter coefficients download.

The VBG input pin must be connected to the IREF pin of the STLC3080.

When the L3235N is used in kit with STLC5048 the ILIM, ITH and VBG pin must be not connected.

4.13 Built-in test

By means of TONEG register it is possible to inject a tone of variable frequency (25 Hz, 1 and 3 kHz) and 0 dBm0 amplitude into the receive path, replacing any signal coming from the PCM interface. This test can be performed on every channel.

Setting the proper bit of the PCMCOM register is also possible to read/write the PCM data coming from the transmit path via the MCU interface (PCMRD/PCMWD registers). This feature can be enabled only on one channel per time.

These two features can be used to test the line interface operation.

Table 7. Register addresses

Addr	Name	Description
00h	DIR-L	I/O direction (bit 7-0)
01h	DIR-H	I/O direction (bit 11-8)
02h	DATA0-L	I/O data ch#0 (bit 7-0)
03h	DATA0-H	I/O data ch #0 (bit 11-8)
04h	DATA1-L	I/O data ch#1 (bit 7-0)
05h	DATA1-H	I/O data ch #1 (bit 11-8)
06h	DATA2-L	I/O data ch#2 (bit 7-0)
07h	DATA2-H	I/O data ch #2 (bit 11-8)

Table 7. Register addresses (continued)

Addr	Name	Description
08h	DATA3-L	I/O data ch#3 (bit 7-0)
09h	DATA3-H	I/O data ch #3 (bit 11-8)
0Ah	PCHK-A	Persistency check time for input A
0Bh	PCHK-B	Persistency check time for input B
10h	INT	Interrupt register
11h	DMASK-L	Int. mask I/O port (03h)
12h	DMASK-H	Int. mask I/O port (04h)
13h	IMASK	Interrupt mask reg.
14h	ALARM	Alarm register
20h	CONF	Configuration register
21h	COMEN	Command enable reg.
23h	SYNCCK	Synchronous check reg.
25h	CTRLACK	DSP status register
26h	CKSUM-L	Checksum register L
27h	CKSUM-H	Checksum register H
2Ah	LOOPB	Loopback register
2Bh	TXG	Transmit preamp. gain
2Ch	RXG	Receive preamp. gain
2Dh	ILIM	SLIC line current lim.
2Eh	ITH	SLIC off-hook threshold
50h	PCMSH	PCM shift register
51h	PCMCOM	PCMCOM register
52h	DXTS0	Transmit time slot ch #0
53h	DXTS1	Transmit time slot ch #1
54h	DXTS2	Transmit time slot ch #2
55h	DXTS3	Transmit time slot ch #3
56h	DRTS0	Receive time slot ch #0
57h	DRTS1	Receive time slot ch #1
58h	DRTS2	Receive time slot ch #2
59h	DRTS3	Receive time slot ch #3
5Ah	PCMWD-L	PCMW data register
5Bh	PCMWD-H	PCMW data register
5Ch	PCMRD-L	PCMR data register
5Dh	PCMRD-H	PCMR data register
5Eh	PCMCTRL	PCM control register

Table 7. Register addresses (continued)

Addr	Name	Description
60h	TONEG	Tone generation reg.
61h	COEFST	Coefficient state reg.
70h	SWRID	Software rev. ID code
71h	HWRID	Silicon revision ID code

5 Register description

5.1 I/O direction register (DIR)

Addr=00h; reset value=00h
Addr=01h; reset value=X0h

Table 8. I/O direction register (DIR) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	0	0
IO_7	IO_6	IO_5	IO_4	IO_3	IO_2	IO_1	IO_0

Table 9. I/O direction register (DIR) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	0	1
				IO_{11}	$IO_{10}0$	IO_9	IO_8

IO11..0=0 I/O pin 11..0 is an input, data on the I/O input is written in DATAn register bit 11..0.
IO11..0=1 I/O pin 11..0 is an output, data contained in DATAn register bit 11..0 is transferred to the I/O output.

5.2 I/O data register channel #0 (DATA0)

Addr=02h; reset value=00h
Addr=03h; reset value=X0h
If bit 4 of CONF register (STA)=0 dynamic I/O mode:

Table 10. Dynamic I/O data register channel #0 (DATA0) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	0
$D0_7$	$D0_6$	$D0_5$	$D0_4$	$D0_3$	$D0_2$	$D0_1$	$D0_0$

Table 11. Dynamic I/O data register channel #0 (DATA0) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	1
				$D0_{11}$	$D0_{10}$	$D0_9$	$D0_8$

When CS0 is active D011..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D011..0 will be written by the values applied to those pins while CS0 is low.

If bit 4 of CONF register (STA)=1 static I/O mode:

Table 12. Static I/O data register channel #0 (DATA0) bits

BIt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	0
DS_7	DS_6	DS_5	DS_4	DS_3	DS_2	DS_1	DS_0

Table 13. Static I/O data register channel #0 (DATA0) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	1
				DS_{11}	DS_{10}	DS_9	DS_8

DS11..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding DS11..0 will be written by the values applied to those pins.

5.3 I/O data register channel #1 (DATA1)

Addr=04h; reset value=00h
Addr=05h; reset value=X0h

If bit 4 of CONF register (STA)=0 dynamic I/O mode:

Table 14. Dynamic I/O data register channel #1 (DATA1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	0	0
$D1_7$	$D1_6$	$D1_5$	$D1_4$	$D1_3$	$D1_2$	$D1_1$	$D1_0$

Table 15. Dynamic I/O data register channel #1 (DATA1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	0	1
				$D1_{11}$	$D1_{10}$	$D1_9$	$D1_8$

When $\overline{CS1}$ is active D111..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D111..0 will be written by the values applied to those pins while $\overline{CS1}$ is low.

If bit 4 of CONF register (STA)=1 static I/O mode:

In static mode CS pins are used as additional I/O pins. The CIO0..3 bits are used to define the direction of these pins.

Table 16. Static I/O data register channel #1 (DATA1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	0	0
				CIO_3	CIO_2	CIO_1	CIO_0

CIO0..3=0 The $\overline{CS0..3}$ is a static input, DATA is written in DATA2 register bits 0..3.
CIO0..3=1 The $\overline{CS0..3}$ is a static output, DATA is taken from DATA2 register bits 0..3.

5.4 I/O data register channel #2 (DATA2)

Addr=06h; reset value=00h
Addr=07h; reset value=X0h

If bit 4 of CONF register (STA)=0 dynamic I/O mode:

Table 17. Dynamic I/O data register channel #2 (DATA2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	1	0
$D2_7$	$D2_6$	$D2_5$	$D2_4$	$D2_3$	$D2_2$	$D2_1$	$D2_0$

Table 18. Dynamic I/O data register channel #2 (DATA2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	1	1
				$D2_{11}$	$D2_{10}$	$D2_9$	$D2_8$

When $\overline{CS2}$ is active D211..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D211..0 will be written by the values applied to those pins while $\overline{CS2}$ is low.

If bit 4 of CONF register (STA)=1 static I/O mode:

Table 19. Static I/O data register channel #2 (DATA2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	1	0
				CD_3	CD_2	CD_1	CD_0

CD0..3 are transferred to the corresponding CS pin if configured as static output (see DATA1 register). For the CS pins configured as static inputs the corresponding CD0..3 will be written by the values applied to those pins.

5.5 I/O data register channel #3 (data3)

Addr=08h; reset value=00h
Addr=09h; reset value=X0h

Used only if bit 4 of CONF register (STA)=0; dynamic I/O mode:

Table 20. Dynamic I/O data register channel #3 (data3) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	1	0	0	0
$D3_7$	$D3_6$	$D3_5$	$D3_4$	$D3_3$	$D3_2$	$D3_1$	$D3_0$

Table 21. Dynamic I/O data register channel #3 (data3) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	1	0	0	1
				$D3_{11}$	$D3_{10}$	$D3_9$	$D3_8$

When $\overline{CS3}$ is active D311..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D311..0 will be written by the values applied to those pins while $\overline{CS3}$ is low.

If bit4 of CONF register (STA) = 1
Static I/O mode:

- $D3_{3..0}$=1: The corresponding CSn cannot generate interrupt.
- $D3_{3..0}$=0: The corresponding I/O (programmed as input) can generate interrupt if a change of status is detected.

5.6 Persistency check register (PCHK-A/B)

Addr=0Ah; reset value=00h
Addr=0Bh; reset value=00h

Two input signal per channel, labelled A and B, are submitted to persistency check.

In dynamic mode (STA=0), A and B inputs of the four channels are sampled on the multiplexed lines IO0 (pin 13) and IO1 (pin 14).

In static mode (STA=1) persistency check is performed on four pairs of lines, assigned to each channel according to the table:

Table 22. A and B inputs of persistency check register in static mode

CHAN #	Input A	Input B
0	IO_0 (pin 19)	IO_1 (pin 14)
1	IO_4 (pin 17)	IO_5 (pin 18)
2	IO_6 (pin 48)	IO_7 (pin 47)
3	IO_{10} (pin 44)	IO_{11} (pin 43)

Table 23. Persistency check register (PCHK-A/B) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	1	0	1	0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

Table 24. Persistency check register (PCHK-A/B) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	1	0	1	1
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

TA7..0 and TB7..0, contents of PCHKA and PCHKB registers, define the minimum duration of input A and B to generate interrupt; spurious transitions shorter than the programmed value are ignored.

The time width can be calculated according to the formula:

Time - Width A = (TA7..0)*64µs

Time - Width B = (TB7..0)*64µs

If PCHKA/B is programmed to 00h the persistency check is not performed and any detected transition will generate interrupt.

All the inputs, with or without persistency check, are sampled with a repetition rate of 32 µs.

5.7 Interrupt register (INT)

Addr=10h; reset value=00h
Read-only

Table 25. Interrupt register (INT) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	0	1	0	0	0	0
	ITV	IPCM	ICKF	ID3	ID2	ID1	ID0

In dynamic I/O configuration the ID3..0 bits latch the interrupt request from the related channel (SLIC). Any single bit IDn is cleared after reading related I/O register or by setting MCn bit high (that is, when channel n is disabled to generate interrupt).

In static I/O configuration ID0 and ID2 bits latch the interrupt request from I/O11..0 and CS3..0 respectively:

- ID0: is set High when the interrupt is requested from any the I/O11..0 lines.
- ID2: is set High when the interrupt is requested from any the CS3..0 (configured as I/O).
- ID0 and ID2 are cleared after reading related I/O register.
- ID1 and ID3 are don't care.
- ITV = 1: If the interrupt has been generated by time-out violation on the MCU serial interface.
- IPCM = 1: When transmit PCM data reading/writing test is enabled an interrupt is generated every time valid data are available (RRD bit set to 1) or must be written (WRD bit set to 1). The interrupt is cleared after reading/writing the data in the PCMRD/PCMWD register via the MCU interface.
- ICKF = 1: If the interrupt has been generated by a clock failure on PCM port (MCLK).

The INT register is cleared after reading operation only if signals (alarm cause) are inactive.

5.8 Interrupt mask register for I/O port (DMASK)

Addr=11h; reset value=FFh
Addr=12h; reset value=XFh

Table 26. Interrupt mask register for I/O port (DMASK) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	1	0	0	0	1
MD_7	MD_6	MD_5	MD_4	MD_3	MD_2	MD_1	MD_0

Table 27. Interrupt mask register for I/O port (DMASK) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	1	0	0	1	0
				MD_{11}	MD_{10}	MD_9	MD_8

- $MD_{11..0}$=1: The corresponding I/O doesn't generate interrupt.
- $MD_{11..0}$=0: The corresponding I/O (programmed as input) generate interrupt if a change of status is detected.

Input lines with persistency check generate interrupt if the changed status remains stable longer than the time programmed in the persistency check register PCHKA/B. Line without persistency check generate an immediate interrupt request.

Mask register has no effect on those pins configured as outputs, those pins will not generate interrupt.

5.9 Interrupt mask register for interrupt (IMASK)

Addr=13h; reset value=FFh

Table 28. Interrupt mask register for interrupt (IMASK) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	1	0	0	1	1
x	MTV	MPCM	MCF	MC3	MC2	MC1	MC0

For dynamic I/O configuration, MCn bits are the disable/enable interrupt related to the channel n.

- MC3..0=1: Any I/O line of the related channel #n is disabled to generate interrupt independently of DMASK setting.
- MC3..0=0: Any I/O line of the related channel #n is enabled to generate interrupt depending on DMASK setting.

For static I/O configuration, MCn bits are the interrupt mask bits related to CSn that are configured as I/O lines.

- MC0=1: The corresponding I/O cannot generate interrupt independently of DMASK setting.
- MC0=0: The corresponding I/O can generate interrupt if a change of status is detected depending of DMASK setting.
- MC2=1: The corresponding I/O cannot generate interrupt independently of DATA3_L setting (bit 3..0).
- MC2=0: The corresponding I/O can generate interrupt if a change of status is detected depending of DATA3_L setting (bit 3..0).

MC3 and MC1 bit are not used in static mode.

Input lines with persistency check generate interrupt if the changed status remains stable longer than the time programmed in the persistency check register PCHKA/B. Line without persistency check generate an immediate interrupt request.

Mask register has no effect on those pins configured as outputs, those pins will not generate interrupt

- MCF=1: The corresponding alarm bit (CKF) doesn't generate interrupt.
- MCF=0: The corresponding alarm bit (CKF) can generate interrupt.
- MTV=1: The corresponding alarm bit (TV) doesn't generate interrupt.
- MTV=0: The corresponding alarm bit (TV) can generate interrupt.
- MPCM =1: The IPCM interrupt is masked (generation disabled).
- MPCM =0: The IPCM interrupt is enabled (generation enabled).

5.10 Alarm register (ALARM)

Addr=14h; reset value=01h
Read-only

Table 29. Alarm register (ALARM) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	0	1	0	1	0	0
0	0	0	0	0	0	0	POR

POR=0: No power on reset is detected during operation.

POR=1: A power on reset is detected during operation.

The ALARM register is cleared after reading operation only if signals (alarm cause) are inactive.

5.11 Configuration register (CONF)

Addr=20h; reset value=BFh

Table 30. Configuration register (CONF) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	0	0	0	0
RES	LIN	AMU	STA	PD3	PD2	PD1	PD0

- RES=0: Normal operation
- RES=1: Device reset: I/0n and Csn are all inputs, DX is H.I. (equivalent to Hw reset).
- LIN=0: A or μ law PCM encoding
- LIN=1: Linear encoding (16 bits), two's complement.
- AMU=0: μ law selection (all bits inverted)
- AMU=1: A law selection (even bits inverted)
- STA=0: CS0 to CS3 scan the four SLICs connected to the I/O control port, each CS has a 31.25 μs repetition time.
- STA=1: I/O are static, CS0 to CS3 are configured as generic static I/O.
- PD3..0=0: Codec 3..0 is active.
- PD3..0=1: Codec 3..0 is in power down. When one codec is in power down the corresponding VFRO output is set to AGND and the corresponding transmit time slot on DX is set in H.I.

5.12 Command enable register (COMEN)

Addr=21h; reset value=80h

Table 31. Command enable register (COMEN) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	0	0	0	1
PDR	0	0	0	E_3	E_2	E_1	E_0

The En bits enable a command on one or more channels. All enabled channels will receive the entered data. At least one channel must be enabled before every command.

- E0..3=0: commands disabled on the corresponding channel 0..3
- E0..3=1: commands enabled on the corresponding channel 0..3
- PDR = 0: RAM is enabled also in power down.
- PDR = 1: RAM is disabled in power down. In this way it's possible to reduce the power consumption in power down.

5.13 Synchronous check register (SYNCK)

Addr=23h; reset value=E4h
Read-only

Table 32. Synchronous check register (SYNCK) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	0	0	0	1	1
1	1	1	0	0	1	0	0

This register contains a fixed code (E4h) that can be read to check the synchronization of the MCU interface.

5.14 DSP status register (CTRLACK)

Addr=25h; reset value=01h
Read-only

Table 33. DSP status register (CTRLACK) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	0	0	1	0	1
0	0	0	0	0	0	INIT	CKEND

CKEND bit is 0 while the checksum calculation is performed: in the other time is always set to 1.

INIT bit becomes active (INIT = 1) after the DSP initialization. Normally it requires 70 µs after the reset to be set to 1.

5.15 Checksum register (CKSUM)

Addr=26h; reset value=00h
Addr=27h; reset value=00h
Read-only

Table 34. Checksum register (CKSUM) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	0	0	1	1	0
CK_7	CK_6	CK_5	CK_4	CK_3	CK_2	CK_1	CK_0

Table 35. Checksum register (CKSUM) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	0	0	1	1	1
CK_{15}	CK_{14}	CK_{13}	CK_{12}	CK_{11}	CK_{10}	CK_9	CK_8

The checksum value is calculated every time the CKSTART instruction is performed and the result is available after a proper delay (max 400 µs).

This register contains the checksum value calculated on the contents of the following coefficient (each of 16 bits):

ZERO

KDF0_0 KDF0_1 KDF0_2 KDF1_0 KDF1_1 KDF1_2 KDF2_0 KDF2_1 KDF2_2 KDF3_0 KDF3_1 KDF3_2 AFE_CFF GRX0 GTX0 RFC0_0 ..... RFC0_16 XFC0_0 ..... XFC0_16 BFC0_0 ..... BFC0_25
ZFC0_0 ..... ZFC0_4 GRX1 GTX1 RFC1_0 ..... RFC1_16 XFC1_0 ..... XFC1_16 BFC1_0 .....BFC1_25 ZFC1_0 ..... ZFC1_4 GRX2 GTX2 RFC2_0 .....RFC2_16 XFC2_0 ..... XFC2_16 BFC2_0 ..... BFC2_25

ZFC2_0 ..... ZFC2_4 GRX3 GTX3 RFC3_0 ..... RFC3_16 XFC3_0 ..... XFC3_16 BFC3_0 ..... BFC3_25 ZFC3_0 .....ZFC3_4

5.16 Loopback register (LOOPB)

Addr=2Ah; reset value=00h

Table 36. Loopback register (LOOPB) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	1	0	1	0
DL3	DL2	DL1	DL0	AL3	AL2	AL11	AL0

- DL3..0=0: Normal operation
- DL3..0=1: Codec #3..0 is set in digital loopback mode, this means that the receive PCM signal applied to the programmed receive time slot is transferred to the programmed transmit time slot.
- AL3..0=0: Normal operation
- AL3..0=1: Codec #3..0 is set in analog loopback mode, this means that the VFRO signal is transferred to the VFXI input internally into the codec.

When loopbacks are enabled the signal appears also at the corresponding VFRO output. It is possible to have no signal on the VFRO output programming the GRX command to 00h in case of digital loopback.

5.17 Transmit pre-amplifier gain register (TXG)

Addr=2Bh; reset value=00h

Table 37. Transmit pre-amplifier gain register (TXG) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	1	0	1	1
				TG3	TG2	TG1	TG0

- TG3..0=0: Transmit preamplifier gain ch. 3..0 = 0dB
- TG3..0=1: Transmit preamplifier gain ch. 3..0 = 3.52dB

Overall transmit gain depends on combination of TXG and GTXn registers.

5.18 Receive amplifier gain register (RXG)

Addr=2Ch; reset value=00h

Table 38. Receive amplifier gain register (RXG) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	1	1	0	0
$R3_1$	$R3_0$	$R2_1$	$R2_0$	$R1_1$	$R1_0$	$R0_1$	$R0_0$

- Rn_0=0,Rn_1=0: Receive amp. gain ch #n = mute
- Rn_0=1,Rn_1=0: Receive amp. gain ch #n = -12dB
- Rn_0=0,Rn_1=1: Receive amp. gain ch #n = -6dB
- Rn_0=1,Rn_1=1: Receive amp. gain ch #n = 0dB

Overall receive gain depends on the receive amplifier gain (R3..0) setting in RXG reg. and digital gain (GRXn reg. setting).

5.19 SLIC line current limit reg (ILIM)

Addr=2Dh; reset value=00h

Table 39. SLIC line current limit reg (ILIM) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	1	1	0	1
0	0	0	D4	D3	D2	D1	D0

- D4..0 = 0: Programmed value is 53
- D4..0 = 1: Programmed value is 2

The step is 1.6 mA.

This register allows to program a line current limitation from 2 to 53 mA with a step equal to 1.6 mA. These values can be obtained using an external 15 kohm resistor in kit with STLC3080.

5.20 SLIC off-hook threshold register (ITH)

Addr=2Eh; reset value=00h

Table 40. SLIC off-hook threshold register (ITH) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	1	1	1	0
0	0	0	En	D3	D2	D1	D0

- D3..0 = 0: Programmed value is 16 mA
- D3..0 = 1: Programmed value is 1 mA

The step is equal to 1 mA.

- En = 1: The DC SLIC programmability block is enabled (ITH and ILIM)
- En = 0: The DC SLIC programmability block is disabled (ITH and ILIM)

This register allows to program a threshold value from 1 to 16 mA with a step equal to 1mA. These values can be obtained using an external 12.5 kohm resistor in kit with STLC3080.

5.21 PCM shift register (PCMSH)

Addr=50h; reset value=00h

Table 41. PCM shift register (PCMSH) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	0	0	0
	XS2	XS1	XS0		RS2	RS1	RS0

- XS2..0: Effective start of the TX frame is the programmed values of clock pulses (0 to 7) after the FS rising edge.
- RS2..0: Effective start of the RX frame is the programmed values of clock pulses (0 to 7) after the FS rising edge.

5.22 PCM command register (PCMCOM)

Addr=51h; reset value=00h

Table 42. PCM command register (PCMCOM) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	0	0	1
RR	WR	PC1	PC0	TE	RPAB	TPB	TPA

TPA/B = These two bits are used to enable the DX outputs of the port A and/or B. According to the combination of these two bits the enabled port will be as follows:

Table 43. PCM command register (PCMCOM) TPB and TPA bit combinations

TPB	TPA	Description
0	0	Both ports disabled
0	1	Port A enabled
1	0	Port B enabled
1	1	Both ports enabled

- RPAB = 0: Port A enabled (DRA input selected)
- RPAB = 1: Port B enabled (DRB input selected)
- TE = 0: Transmit PCM data change on rising edge of MCLK
- TE = 1: Transmit PCM data change on falling edge of MCLK
- PC1-PC0 = Selection of the channel for the PCM access data via MCU.

Table 44. PCM command register (PCMCOM) PC0 and PC1 bit combinations

PC0	PC1	Description
0	0	Channel #0 selected
1	0	Channel #1 selected
0	1	Channel #2 selected
1	1	Channel #3 selected

- WR = 1: Setting this bit, receive PCM data writing via MCU (after A/µ decoding) is enabled on selected channel and IPCM interrupt is generated every time FS signal becomes active, together to the set of the WRD bit in the PCMCTRL register.

  A data byte must be written every 125 µs, if data is not replaced the old value is inserted again but the PMW bit is set to 1 in the PCMCTRL register.
- RR = 1: Setting this bit, transmit PCM data reading (after A/µ encoding) via MCU is enabled on selected channel and IPCM interrupt is generated every time that data are available, together to the set of the RRD bit in the PCMCTRL register.

  A data byte must be read every 125 µS, if data is not read the new value is written in the PCM access register but the POW bit is set to 1 in the PCMCTRL register.

5.23 Transmit time slot ch #0 (DXTS0)

Addr=52h; reset value=00h

Table 45. Transmit time slot ch #0 (DXTS0) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	0	1	0
EN0	T06	T05	T04	T03	T02	T01	T00

- EN0=0: Selected transmit time slot on DX output is in H.I.
- EN0=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI0.
- T06..0: Define time slot number (0 to 127) on which PCM encoded signal of VFXI0 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if T06..T00=00:

Table 46. Transmit time slot ch #0 (DXTS0) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.24 Transmit time slot ch #1 (DXTS1)

Addr=53h; reset value=00h

Table 47. Transmit time slot ch #1 (DXTS1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	0	1	1
EN1	T16	T15	T14	T13	T12	T11	T10

- EN1=0: Selected transmit time slot on DX output is in H.I.
- EN1=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI1.
- T16..0: Define time slot number (0 to 127) on which PCM encoded signal of VFXI1 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if T16..T10=00:

Table 48. Transmit time slot ch #1 (DXTS1) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.25 Transmit time slot ch #2 (DXTS2)

Addr=54h; reset value=00h

Table 49. Transmit time slot ch #2 (DXTS2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	1	0	0
EN2	T26	T25	T24	T23	T22	T21	T20

- EN2=0: Selected transmit time slot on DX output is in H.I.
- EN2=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI2.
- T26..0: Define time slot number (0 to 127) on which PCM encoded signal of VFXI2 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if T26..T20=00:

Table 50. Transmit time slot ch #2 (DXTS2) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.26 Transmit time slot ch #3 (DXTS3)

Addr=55h; reset value=00h

Table 51. Transmit time slot ch #3 (DXTS3) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	1	0	1
EN3	T36	T35	T34	T33	T32	T31	T30

- EN3=0: Selected transmit time slot on DX output is in H.I.
- EN3=1: Selected transmit time slot on DX output is active carrying out the PCM encoded signal of VFXI3.
- T36..0: Define time slot number (0 to 127) on which PCM encoded signal of VFXI3 is carried out.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be carried out as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if T36..T30=00:

Table 52. Transmit time slot ch #3 (DXTS3) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.27 Receive time slot ch #0 (DRTS0)

Addr=56h; reset value=00h

Table 53. Receive time slot ch #0 (DRTS0) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	1	1	0
EN0	R06	R05	R04	R03	R02	R01	R00

- EN0=0: Disable reception of selected time slot.
- EN0=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO0 output.
- R06..0: Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO0 output. If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if R06..R00=00:

Table 54. Receive time slot ch #0 (DRTS0) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.28 Receive time slot ch #1 (DRTS1)

Addr=57h; reset value=00h

Table 55. Receive time slot ch #1 (DRTS1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	0	1	1	1
EN1	R16	R15	R14	R13	R12	R11	R10

- EN1=0: Disable reception of selected time slot.
- EN1=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO1 output.
- R16..0: Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO1 output. If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if R16..R10=00:

Table 56. Receive time slot ch #1 (DRTS1) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.29 Receive time slot ch #2 (DRTS2)

Addr=58h; reset value=00h

Table 57. Receive time slot ch #2 (DRTS2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	1	0	0	0
EN2	R26	R25	R24	R23	R22	R21	R20

- EN2=0: Disable reception of selected time slot.
- EN2=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO2 output.
- R26..0: Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO2 output.

If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if R26..R20=00:

Table 58. Receive time slot ch #2 (DRTS2) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.30 Receive time slot ch #3 (DRTS3)

Addr=59h; reset value=00h

Table 59. Receive time slot ch #3 (DRTS3) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	1	0	0	1
EN3	R36	R35	R34	R33	R32	R31	R30

- EN3=0: Disable reception of selected time slot.
- EN3=1: Selected receive time slot on DR input is PCM decoded and transferred to VFRO3 output.
- R36..0: Define receive time slot number (0 to 127) on carrying the PCM signal to be decoded and transferred to VFRO3 output. If linear mode is selected (LIN=1 of CONF register) the 16 bits will be used as linear code as follows: the 8 most significant bits in the programmed time slot, the 8 least significant bits in the following time slot.

Example: if R36..R30=00:

Table 60. Receive time slot ch #3 (DRTS3) time slots in linear mode

TS0								TS1							
15	14	13	12	11	10	9	8	6	5	4	3	7	2	1	0

5.31 PCMW data register (PCMWD)

Addr=5Ah; reset value=00h
Addr=5Bh; reset value=00h

Table 61. PCMW data register (PCMWD) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	1	0	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 62. PCMW data register (PCMWD) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	1	1	0	1	1
D15	D14	D13	D12	D11	D10	D9	D8

This register is used to write receive PCM data via the MCU interface. Writing this register the IPCM interrupt (if generated only by writing access) is automatically cleared.

In A/μ law only the first 8 bits are used. In linear code option both registers must be used.

5.32 PCMR data register (PCMRD)

Addr=5Ch; reset value=00h
Addr=5Dh; reset value=00h
Read-only

Table 63. PCMR data register (PCMRD) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	1	0	1	1	1	0	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 64. PCMR data register (PCMRD) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	1	0	1	1	1	0	1
D15	D14	D133	D12	D11	D10	D9	D8

This register is used to read transmit PCM data via the MCU interface. Reading this register the IPCM interrupt (if generated only by reading access) is automatically cleared.

In A/μ law only the first 8 bit are used. In linear code option both registers must be read, first the LSB and after the MSB.

5.33 PCM control register (PCMCTRL)

Addr= 5Eh; reset value=00h
Read-only

Table 65. PCM control register (PCMCTRL) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	1	0	1	1	1	1	0
				RRD	WRD	POW	PMW

- PMW = 1: Data is not written every FS while writing PCM access data is enabled.
- POW = 1: Data is not read every FS while reading PCM access data is enabled.
- WRD = 1: Device is waiting for PCM data insertion in PCMWD register. The bit is reset after writing at least one byte.
- RRD = 1: Data are available on PCMRD register. The bit is reset after reading the two bytes of the register (first the LSB and after the MSB).

5.34 Tone generation register (TONEG)

Addr=60h; reset value=00h

Table 66. Tone generation register (TONEG) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	1	0	0	0	0	0
$T3_1$	$T3_0$	$T2_1$	$T2_0$	$T1_1$	$T1_0$	$T0_1$	$T0_0$

- Tn_0=0,Tn_1=0: No tone is generated on ch #n
- Tn_0=1,Tn_1=0: A tone with 25 Hz frequency is generated on ch #n.
- Tn_0=0,Tn_1=1: A tone with 1 kHz frequency is generated on ch #n.
- Tn_0=1,Tn_1=1: A tone with 3 kHz frequency is generated on ch #n.

This register allows the generation of a tone in the RX direction.

5.35 Coefficient state register (COEFST)

Addr= 61h; reset value=F0h

Table 67. Coefficient state register (COEFST) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	1	0	0	0	0	1
FD3	FD2	FD1	FD0	FR3	FR2	FR1	FR0

- FR0..3=1: All channel filters and gain blocks are configured as defined in the ringing state
- FR0..3=0: All channel filters and gain blocks are configured as defined with the programmed value if also the corresponding FD bit is set to 0
- FD0..3=1: All channel filters and gain blocks are configured as defined in the default state if also the corresponding FR bit is set to 0
- FD0..3=0: All channel filters and gain blocks are configured as defined with the programmed value if also the corresponding FR bit is set to 0

5.36 Software revision ID Code (SWRID)

Addr=70h; Read-only.

Table 68. Software revision ID Code (SWRID) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	1	1	1	0	0	0	0
0	0	0	1	0	1	0	0

This register contains the DSP software revision code identifier.

5.37 Hardware revision ID code (HWRID)

Addr=71h; Read-only.

Table 69. Hardware revision ID code (HWRID) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	1	1	1	0	0	0	1
0	0	0	0	0	0	0	1

This register contains the silicon revision code identifier.

6 Single byte instruction

Table 70. Single byte instruction

Name	Description	ID
REACOM	Realignment command	28h
CKSTART	Start checksum	29h

6.1 Realignment command (REACOM)

This single instruction is used to realign the MCU interface in case of out of synchronization. This instruction must be executed N_{max}+1 times to be successful.

Table 71. Realignment command (REACOM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	1	0	0	0

6.2 Start checksum calculation (CKSTART)

This single instruction is used to start the checksum calculation of the entered data used to configure the device.

Table 72. Start checksum calculation (CKSTART)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	1	0	0	1

7 Command list

Table 73. Command list

Name	Description	ID
BLKEN	Block enable	22h
KDF	KD filter	30h
AFECFF	AFE KA coefficient (*)	31h
T_OUT	Timeout value (*)	32h
GRX	Receive gain	40h
GTX	Transmit gain	41h
RFC	R filter coefficient	42h
XFC	X filter coefficient	43h
BFC	B filter coefficient	44h
ZFC	Z filter coefficient	45h

(*) For these two commands, the bit set in the COMEN register are not considered.

8 Command description

Each command is transferred on every channel that has the proper bit in the COMEN register set to 1.

8.1 Block enable command (BLKEN)

Reset value=00h

The command is used to enable/disable the B, Z, R and X blocks.

Table 74. Block enable command (BLKEN) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	0	0	0	1	0
				XE	RE	ZE	BE

- BE=1: The B block is equal to an open circuit
- BE=0: The B block is configured as defined in the Ringing state or with the programmed value
- ZE=1: The Z block is equal to an open circuit
- ZE=0: The Z block is configured as defined in the Ringing state or with the programmed value
- RE=1: The R block is equal to a short circuit
- RE=0: The R block is configured as defined in the Ringing state or with the programmed value
- XE=1: The X block is equal to a short circuit
- XE=0: The X block is configured as defined in the Ringing state or with the programmed value

8.2 KD filter (KDF)

The register is used to set the 3 coefficients (each of 16 bits) of the KD filter of the channel #n.

Table 75. KD filter (KDF) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	1	0	0	0	0
.							
.							

8.3 AFE coefficient (AFE_CFF)

Reset value = AA00h

Table 76. AFE coefficient (AFE_CFF) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	1	0	0	0	1
KA31	KA30	KA21	KA20	KA11	KA10	KA01	KA00
							TTX

KAn0, KAn1 = KA coefficient for Ch #n

According to the value of each couple of bits, the KA block is set in the following condition:

KAn1	KAn0	
0	X	KA block disabled
1	0	KA set for low gain
1	1	KA set for high gain

When the application involves also the metering pulse signal the AFE of the STLC5048 must be adapted in order to manage also this signal. For this purpose is provided the TTX bit.

- TTX = 0: the current application is not using the metering pulse signal
- TTX = 1: the current application is using the metering pulse signal

8.4 Timeout value (T_OUT)

Reset value=FFFFh

Table 77. Timeout value (T_OUT) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	1	1	0	0	1	0
T7	T6	T5	T4	T3	T2	T1	T0
T15	T14	T13	T12	T11	T10	T9	T8

Reset value = Maximum value = FFFFh (2048 µs)

To disable this function the T0 bit must be set to 0.

To enable this function the T0 bit must be set to 1; the time-out value is set by means of T<15..1> bits.

Time_out = (T_OUT[15:1]*62.5 + 31.24) ns

The minimum step is 62.5 ns.

8.5 Receive gain (GRX)

Table 78. Receive gain (GRX) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	0	0	0	0	0

- 00h: Stop any received signal to reach the VFRO0 analog output. In order to open the impedance synthesis feedback it's necessary to mute the RX analog amplifier, as well.
- >00h: Digital gain is inserted in the RX path equal to:

  20Log[prog.value/32768]

  The prog. value must be expressed in 16 bits signed format: maximum prog. value is equal to 7FFFh.

8.6 Transmit gain (GTX)

Table 79. Transmit gain (GTX) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	0	0	0	0	1

- 00h: Stop any transmit signal, null level is transmitted in the corresponding time slot on DX output.
- >00h: Digital gain is inserted in the TX path equal to:

  20Log[prog.value/32768]

  The prog. value must be expressed in 16 bits signed format: maximum prog. value is equal to 7FFFh.

8.7 R filter coefficient (RFC)

The register is used to set the 17 coefficients (each of 16 bits) of the R filter of the channel #n.

Table 80. R filter coefficient (RFC) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	0	0	0	1	0

8.8 X filter coefficient (XFC)

The register is used to set the 17 coefficients (each of 16 bits) of the X filter of the channel #n.

Table 81. X filter coefficient (XFC) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	0	0	0	1	1

8.9 B filter coefficient (BFC)

The register is used to set the 26 coefficients (each of 16 bits) of the B filter of the channel #n.

Table 82. B filter coefficient (BFC) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	0	0	1	0	0

8.10 Z filter coefficient (ZFC)

The register is used to set the 5 coefficients (each of 16 bits) of the Z filter of the channel #n.

Table 83. Z filter coefficient (ZFC) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	1	0	0	0	1	0	1

9 Electrical characteristics

Typical value are for 25°C and nominal supply voltage. Minimum and maximum values are guaranteed over the temperature 0-70°C range by production testing and supply voltage range shown in the operating ranges. Performances over -40 +85°C range are guaranteed by product characterization unless otherwise specified.

Table 84. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Digital interface						
Vil	Input voltage low DI pins		0		0.2Vdd	V
Vih	Input voltage high DI pins		0.8Vdd		5.5	V
Iil	Input current low DI pins		-10		10	µA
Iih	Input current high DI pins		-10		10	µA
Ci	Input capacitance (all dig. inp.)			5		pF
Vol	Output voltage low DX, TSX pins	Iol=3.2 mA (other pins Iol=1mA)	0		0.4	V
Voh	Output voltage high DX pin	Ioh=-3.2 mA (other pins Iol=1mA)	0.85Vdd		Vdd	V
Note: all digital inputs are 5V tolerant.						
Analog interface						
RIX	Transmit input amplifier input impedance (VFXI)			m		MΩ
ROR	Receive output impedance			1		W
Power dissipation						
Idd(pd)	Power down current			10	15	mA
Idd(act)	Active current			55	70	mA
PCM interface timing (see *Figure 6*)						
f_{MCLK}	Master clock frequency			1.536 1.544 2.048 4.096 8.192		MHz
Twmh	Period of MCLK high		38			ns
Twml	Period of MCLK low		38			ns
Trm	MCLK rise time				10	ns
Tfm	MCLK fall time				10	ns

Table 84. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Thbf	Hold time MCLK low to FSX/R high or low		10			ns
Tsfb	Setup time FSX/R high to MCLK low		10			ns
Tdmd	Delay time, MCLK high to data valid				15	ns
Tdmz	Delay time from MCLK(8) low to data output disabled		15		40	ns
Tdfd	Delay time, FSX high to data valid if FSX rises later than MCLK rising edge				15	ns
Tdmt	Delay time, from MCLK and FSX both high to TSX low				20	ns
Tzmt	Delay time from MCLK(8) low to TSX disabled		15		40	ns
Tsdm	Setup time, DR valid to MCLK low		5			ns
Thdm	Hold time, MCLK low to DR invalid		5			ns
Serial control port timing (see *Figure 7*)						
fcclk	Frequency of CCLK				8	MHz
twch	Period of CCLK high	Measured from VIH to VIH	40			ns
twcl	Period of CCLK low	Measured from VIL to VIL	40			ns
trc	Rise time of CCLK	Measured from VIL to VIH			20	ns
tfc	Fall time of CCLK	Measured from VIH to VIL			20	ns
thcs	Hold time, CCLK low to CS low		10			ns
thsc	Hold time, CCLK low to CS high		10			ns
tssc	Setup time, CS transition to CCLK low		10			ns
tdsd	Delay time, CS low to CO data valid				20	ns
tcso	CS off time		5			µs
tsdc	Setup time, CI. data in to CCLK low		10			ns
thcd	Hold time, CCLK low to CI invalid		10			ns
tdcd	Delay time, CCLK low to CO data out valid				30	ns

Table 84. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
tddz	Delay time, CS or CCLK9 high to CO high impedance	Pull up resistor = 1 kohm Cload = 30 pF			30	ns
SLIC control interface timing (dynamic configuration; see *Figure 8*)						
Tcs	Chip select repetition rate			31.25		µs
tcsw	Chip select pulse width			3.9		µs
tdcsl	Data out valid to CS low			1.95		ns
tscsh	Data out held after CS high			1.95		ns
tscsh	Set up time data in to CS high			50		ns
thcsh	Hold time data in to CS high			10		ns
Transmit transfer characteristics (all tests are performed in absolute gain condition (TXG = GTXn = 0 dB) unless otherwise specified).						
	Absolute level at 0 dBm0 are: TXG = 0dB, GTXn = 0dB			60		mVrms
GXA	Transmit gain absolute accuracy		-0.15		0.15	dB
GXAG	Transmit gain variation with programmed gain (within 3 dB from max dig. level)		-0.2		0.2	dB
GFX	Gain variation with frequency (relative to gain at 1004 Hz); 0 dBm0 input signal	50 Hz 60 Hz 200 Hz 300-3000 Hz 3400 Hz 4000 Hz 4600 Hz and above	 -1.8 -0.15 -0.7		-20 -20 0 0.15 0 -14.0 -32.0	dB
GAXT	Gain variation with temperature		-0.10		0.10	dB
GAXE	Gain variation with supplies +/- 5% 0 dBm0 input signal		-0.05		0.05	dB
GTX	Gain tracking with tone (1004 Hz Mu Law, 820 Hz A Law) (1)	GSX = 3 to -40 dBm0 GSX = -40 to -50dBm0 GSX = -50 to -55dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
QDX	Quantization distortion with tone (1004 Hz Mu Law, 820 Hz A Law)	VFXI = +3 dbm0 VFXI = 0 to -30 dBm0 VFXI = -40 dBm0 VFXI = -50 to -55 dBm0	33 36 30 15			dB
NCT	Transmit noise C message weighted (Mu and A Law)				12	dBrnCo

Table 84. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
NPT	Transmit noise psophometric weighted @ 0 dBr, Zadm=600 ohm (2)				-68	dBm0p
DAX	Absolute delay (3)	B = 0, Z = 0, X = R = 1	462		587	µS
DPXM	Single frequency distortion (Mu Law 0 dBm0 sinewave @ 1004 Hz)				-46	dB
DPXA	Single frequency distortion (A Law 0 dBm0 sinewave @ 820 Hz)				-46	dB
GSPX	Out of band spurious noise	61 mVrms at VFXI 4200 Hz to 72 kHz			-39	dBm0
1) VFXI=106 mVrms, TXG=+3.52 dB, GTX=-8.308 dB (levels and gain condition equivalent to 0 dBr with Zadm = 600 ohm on the application) 2) TXG=+3.52 dB, GTX=-8.308 dB (gain condition equivalent to 0 dBr with Zadm = 600 ohm on the application) 3) The max value includes 125 µs for the time slot synchronization.						
Receive transfer characteristics (all tests are performed in absolute gain condition (RXG = GRXn = 0 dB) unless otherwise specified).						
	Absolute levels at 0 dBm0 are: RXG = 0 dB, GRXn = 0 dB			547		mVrms
GRA	Transmit gain absolute accuracy		-0.15		0.15	dB
GRAG	Receive gain variation with programmed gain (within 3 dB from max dig. level)		-0.2		0.2	dB
GFR	Gain variation with frequency (relative to gain at 1004 Hz); 0 dBm0 input signal	Below 200 Hz 200 Hz 300-3000 Hz 3400 Hz 4000 Hz	 -0.25 -0.15 -0.7		0.115 0.15 0.15 0 -14	dB
GART	Gain variation with temperature	0 to 70 °C	-0.10		0.10	dB
GARE	Gain variation with Vcc=Vdd= 3.3 V +/- 5% 0 dBm0 input signal		-0.05		0.05	dB
GTR	Gain tracking with tone (1004 Hz Mu Law, 820 Hz A Law)	DR = 3 to -40 dBm0 DR = -40 to -50 dBm0 DR = -50 to -55 dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
QDR	Quantization distortion with tone (1004 Hz Mu Law, 820 Hz A Law)	DR = 3 dBm0 DR = 0 to -30 dBm0 DR = -40 dBm0 DR = -50 to -55 dBm0	33 36 30 15			dB

Table 84. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
NCR	Receive noise C message weighted (Mu Law)			8	11	dBrnCo
NPR	Receive noise psophometric weighted (A Law)				-79	dBm0p
DAR	Absolute delay (2)	B = Z = 0, X = R = 1	325		450	µs
DPR1	Single frequency distortion (0dBm0 sinewave, 1004 Hz)				-46	dB
GSPR	Out of band spurious noise	0 dBm0 DTMF tone at DR			-60	dB
		0 dBm0 180 to 3600 Hz sinewave at DR			-43	dB
OBN	Out of band noise (1)	Integral measure from 3.4 to 128 kHz $G_{TX} = G_{RX} = 0$ dB $G_{TX} = 0$ dB; $G_{RX} = -7$ dB			-48 -51	dBm dBm
		Spectral measure from 3.4 to 200 kHz in B/W = 30 Hz			-70	dBm
1) Values related to the application including the external filter on RX. The measure is referred to the signal replicas. 2) The max value includes 125 ms for the time slot synchronization.						
Supply rejection and crosstalk						
PSRR	Power supply rejection ratio 1 kHz, 50 mVrms	0 to 70°C	42	65		dB
CTX-R	Transmit to receive crosstalk (input signal 200 Hz to 3450 Hz at 0 dBm0)				-76	dB
CTR-X	Receive to transmit crosstalk (input signal 200 Hz to 3450 Hz at 0 dBm0)				-76	dB
CT-ICH	Inter channel crosstalk, TX and RX direction. Input 200 to 3450 Hz at 0 dBm0 at VFXI of one channel; all other VFXI inputs and all DR inputs receive idle signal. Output is measured at DX of the 3 idle channels. Input of 200 to 3450 Hz at 0 dBm0 PCM at DR on one channel. All other DR inputs and all VFXI inputs receive idle signal. Output is measured at VFRO of the 3 idle channels				-78	dB

Figure 6. PCM interface timing

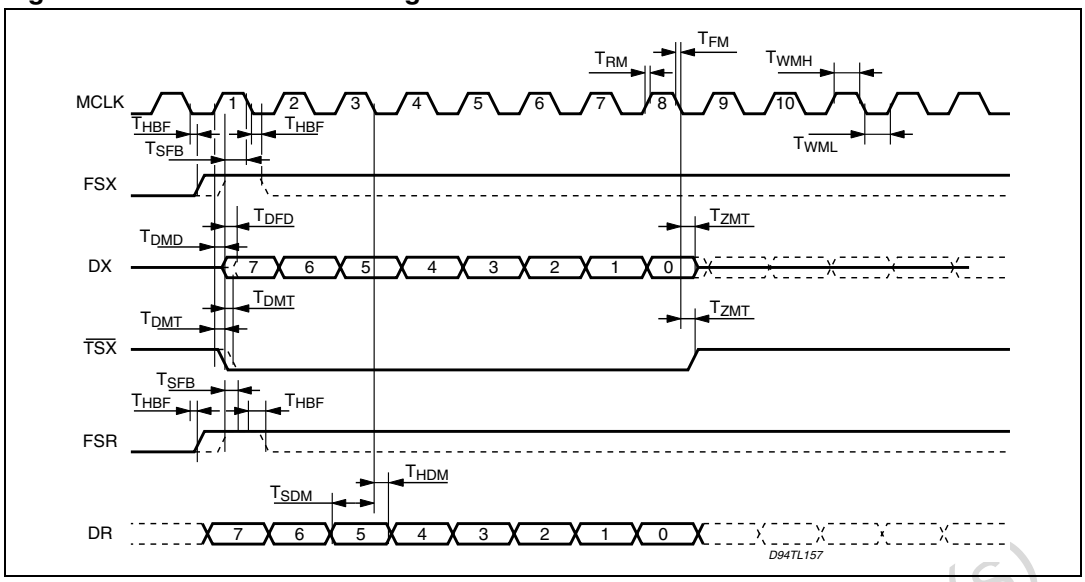


Figure 7. Serial control port timing

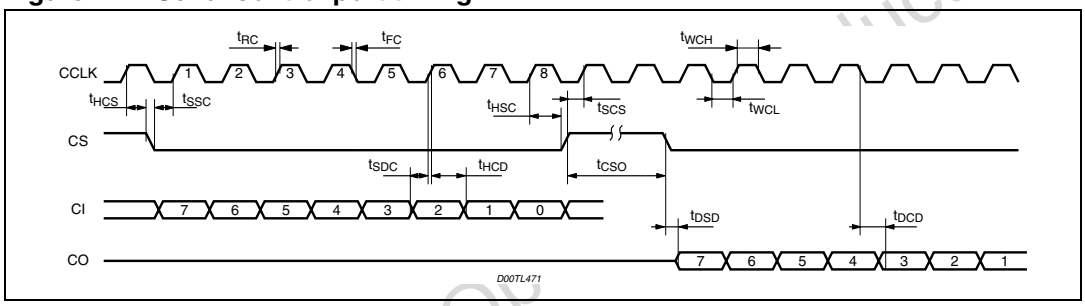


Figure 8. SLIC control port timing

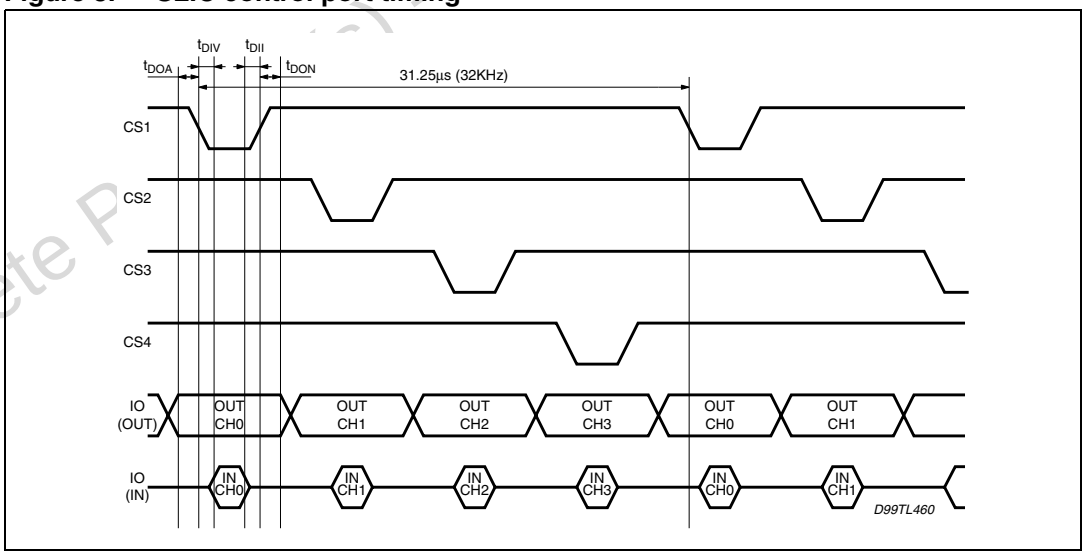
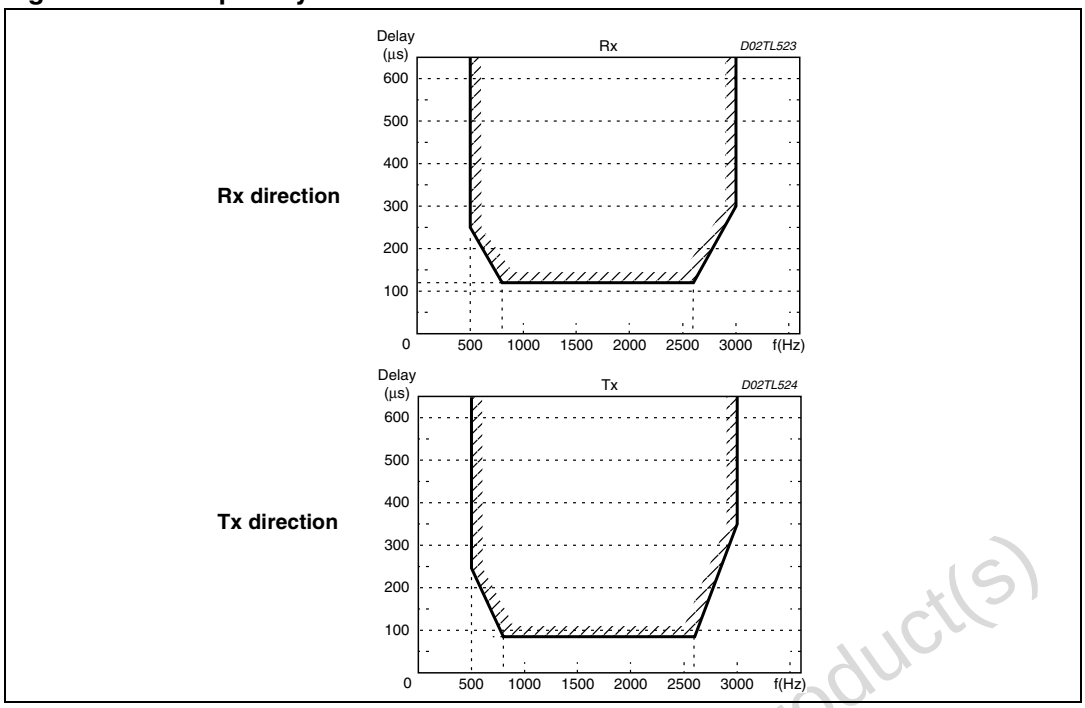


Figure 9. Group delay distortion mask



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97.

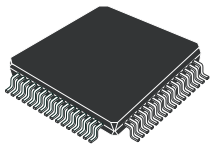
The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

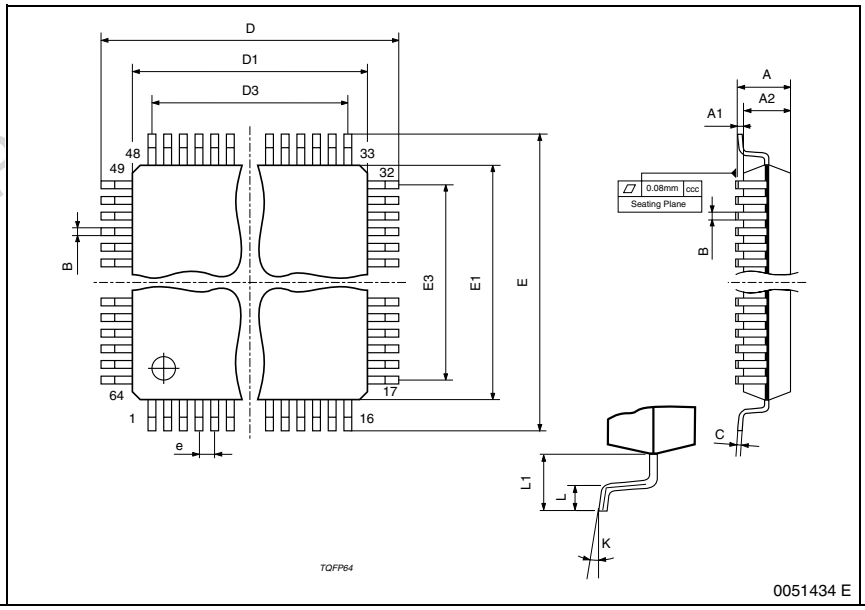
Figure 10. TQFP64 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09			0.0035		
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



TQFP64 (10 x 10 x 1.4mm)



Appendix A Absolute gains in kit with L3235N/STLC3080

Figure 11. STLC5048 in kit with STLC3080 AC application diagram

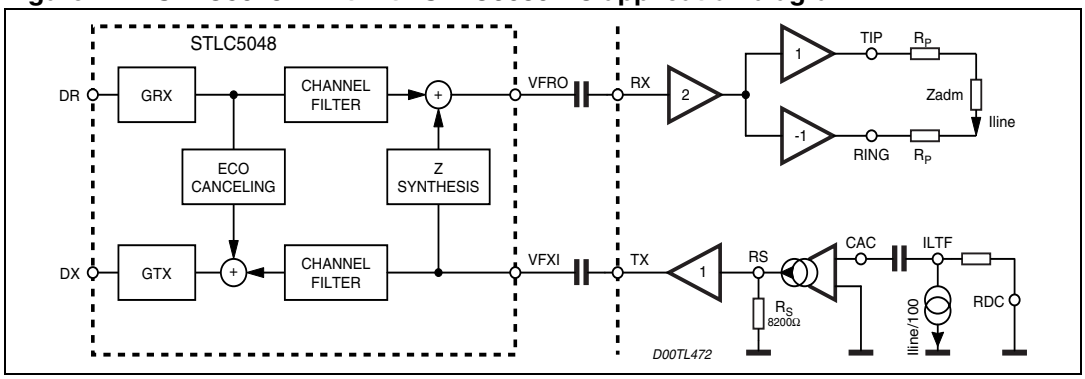
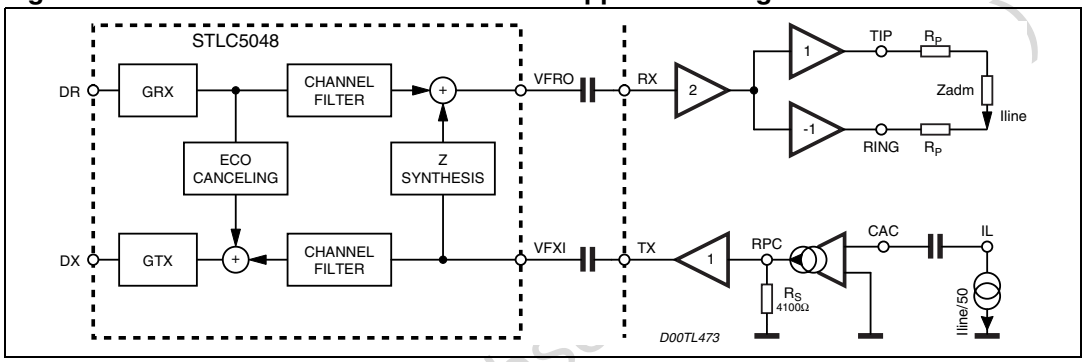


Figure 12. STLC5048 in kit with L3235N AC application diagram



In *Figure 11* is shown the application diagram of the STLC5048 in kit with the STLC3080 SLIC. The figure is related to the AC path as the STLC5048 doesn't perform any DC processing.

The only DC feature performed by STLC5048 is the off-hook and limitation threshold programmability.

The same application diagram for the AC processing can be applied to the kit with the L3235N (as shown in *Figure 12*): the only differences are the following:

- The scaling factor of the Iline is 50.
- Rs value is 4.1 Kohm.
- The impedance synthesis is fully performed by STLC5048; the L3235N SLIC (or the STLC3080) used in kit with the STLC5048 just splits the AC/DC component of Iline, scales it and traduces it into a voltage via RS.

As shown in *Figure 12*, the scaled current is converted into a voltage through the external resistor Rs = 4100 ohm (8200 ohm for the STLC3080): this value is fixed (i.e. independent of the administration): the attenuation between VLINE and VFXI is dependent on the administration.

Considering the TX gain we can proceed as follows for the gain calculation:

- TXG = 0 dB
- GX = 0 dB

  (As reported in the absolute gain levels with 61 Vrms at VFXI and GX=0 dB, the DX output is 0 dBm0).

For instance let's calculate which TX gain to program if +4.2 dBr @ 600 ohm is to be set:
VLINE = 0 dBm @ 600 ohm

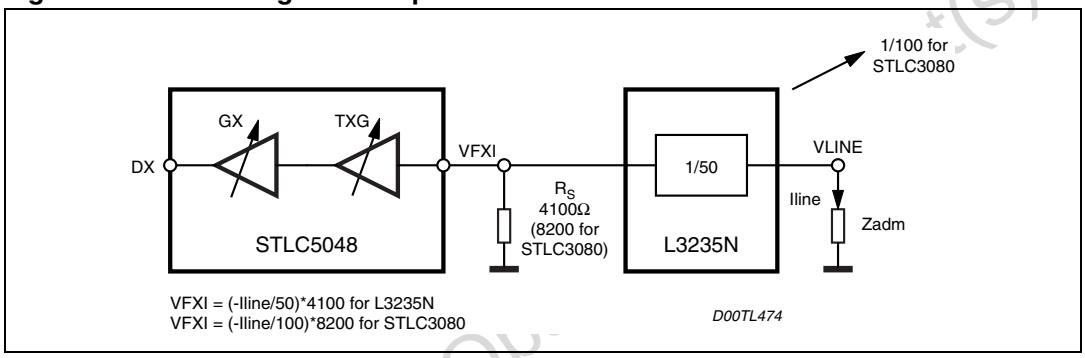
$$VFXI = \frac{VLINE}{600} \cdot \frac{1}{50} \cdot 4100$$

In case of STLC3080 the scaling factor is 100 (instead of 50) while the Rs value is 8200 (instead of 4100) so the result is the same:

$$VFXI = \frac{VLINE}{600} \cdot \frac{1}{100} \cdot 8200$$

Referring to the first formula, to have DX equal to 4.2 dB with VLINE=0 dBm, GX must be set to GX = 4.2 - 4.78 = -0.58 dB.

Figure 13. Absolute gain in TX path



Appendix B STLC5048 application diagrams

Figure 14. STLC5048 plus L3235N/L324 kit application diagram

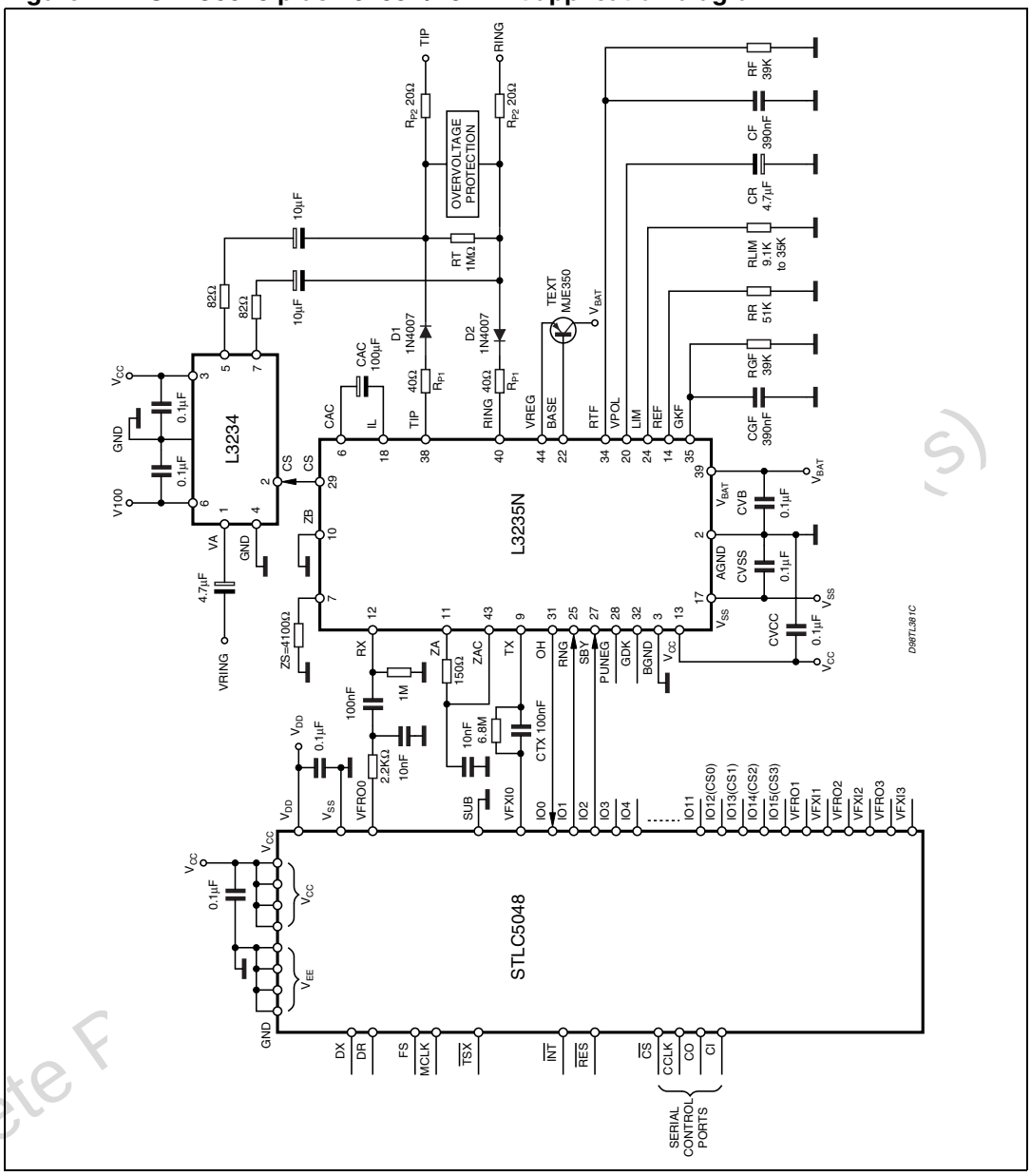
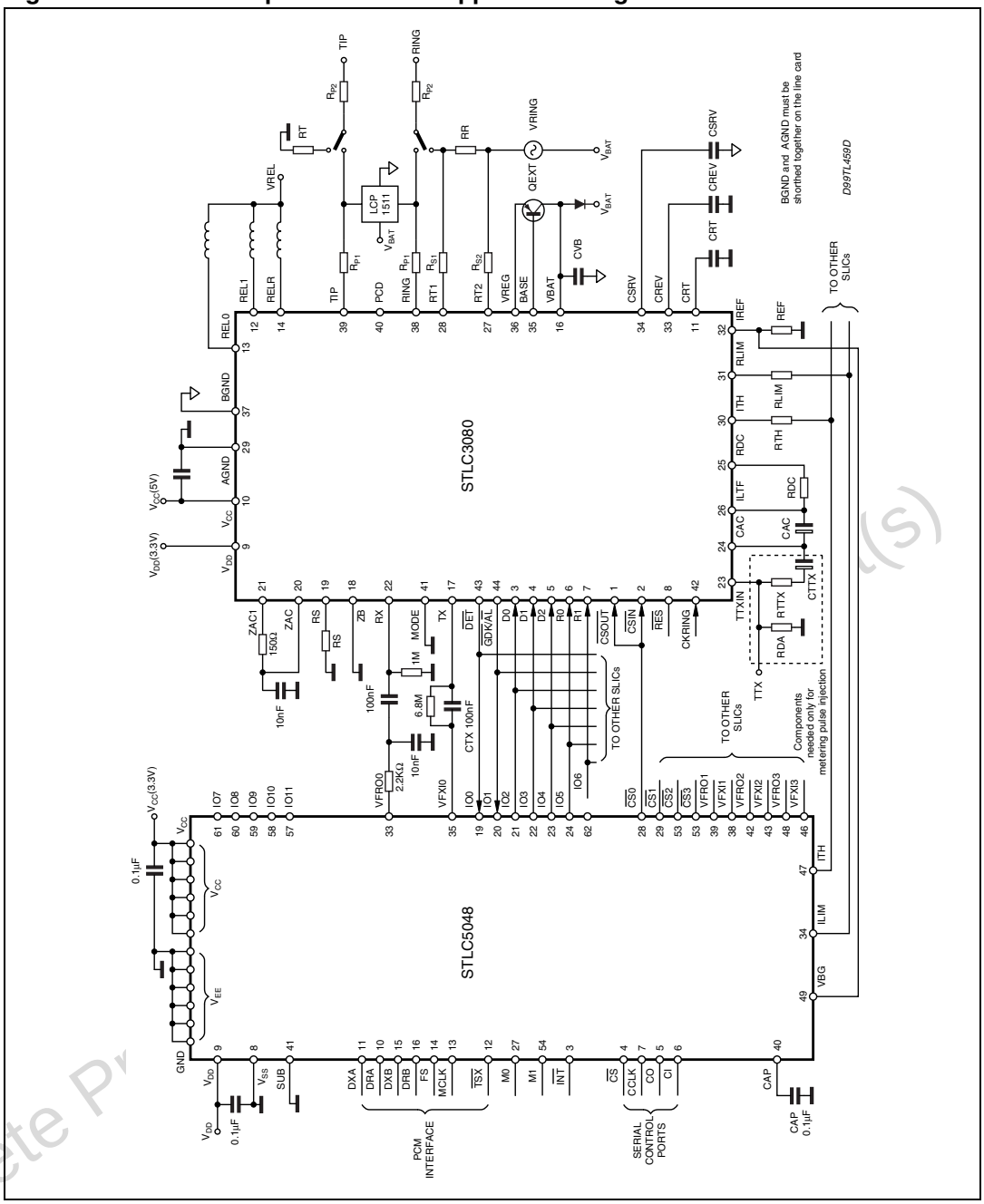


Figure 15. STLC5048 plus STLC3080 application diagram



Appendix C Power sequences

C.1 Power-up sequence

The DSP after an HW (M1=0) or SW reset (CONF[7]=1) or a power-on reset (POR) has to perform the INIT program. To do it at least one channel must be set in active mode.

After that, (2 FS are required), the INIT bit in the CTRLACK register is set to 1 and the RAM can be written and read. It must be noted that to program the device the MCLK and FS signals must be applied to the device.

Following, the correct sequence that must be used in order to program the device.

C.2 Power-on sequence

wait 5 FS signals for PLL locking	
CONF=BF	Sw reset enabled after reset
write CONF=3F	Sw reset disabled
write CONF=30	All channel active
wait 2 FS signals	
read CTRLACK=03	Check INIT bit =1

Before to start the coefficient download, one or more channels must be selected using the COMEN register. The download can be done keeping the device in active mode (at least one channel active) or in power down mode (all channels in power down). If the second choice is selected, the PDR bit in the COMEN register must be set to 0 (internal RAM active also in power down mode).

Ordering information

Table 85. Order codes

Order codes	Package
E-STLC5048[1]	TQFP64
E- STLC5048TR	TQFP64 in Tape & Reel

1. ECOPACK® (see *10: Package mechanical data*)

Revision history

Table 86. Document revision history

Date	Revision	Changes
15-Jan-2003	7	First issue on www.st.com.
02-Apr-2005	8	Changed figures 13 and 14: – Figure 13 added a resistance 6.8 MΩ between pin VFXI0-STLC5048 and pin TX-L3235N – Figure 14 added a resistance 6.8 MΩ between pin VFXI0-STLC5048 and pin TX-STLC3080
28-Nov-2007	9	Added ECOPACK information in *Chapter 10: Package mechanical data* and updated the *Ordering information*.

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