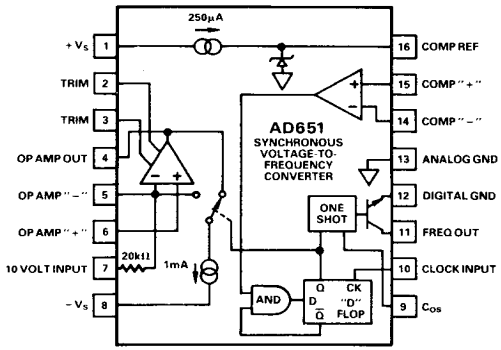
Monolithic Synchronous Voltage-to-Frequency Converter

AD651

FEATURES

- **Full-Scale Frequency (Up to 2MHz) Set by External System Clock**
- **No Critical External Components Required**
- **Extremely Low Linearity Error (0.005% max at 100kHz FS, 0.02% max at 2MHz FS)**
- **Low Drift (25ppm/°C max)**
- **Dual or Single Supply Operation**
- **Voltage or Current Input**
- **Low Cost**

AD651 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD651 Synchronous Voltage-to-Frequency Converter (SVFC) uses a variation of the popular charge-balancing technique to perform the conversion function. The AD651 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external one-shot capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multi-channel systems.

The AD651 is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allows the conversion time and resolution to be optimized for specific applications.

Gain drift is minimized using a precision low-drift buried zener reference and low-TC on-chip thin-film scaling resistors. Furthermore, the initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD651 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD651 is available in three performance grades. The 16-pin cerdip-packaged AQ and BQ grades are specified for operation over the −25°C to +85°C industrial temperature range, and the AD651SQ is available for operation over the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD651 to achieve linearity and stability far superior to any other monolithic VFC. By using the same clock to drive the AD651 and (through a suitable divider) also set the counting period, conversion accuracy is maintained independent of variations in clock frequency.
2. The AD651 Synchronous VFC requires only a single external component (a noncritical integrator capacitor) for operation.
3. The clock input of the AD651 is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
4. The AD651 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.

PRELIMINARY TECHNICAL DATA

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SPECIFICATIONS (typical @ T_A = +25°C, V_S = ±15V, unless otherwise noted)

	AD651AQ/SQ			AD651BQ			
	Min	Typ	Max	Min	Typ	Max	Units
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{OUT} = 100kHz		±0.5	±1		±0.25	±0.5	%
f_{OUT} = 500kHz		±0.5	**±1**		±0.25	**±0.5**	%
f_{OUT} = 2MHz		±0.5	**±1.5**		±0.25	**±0.75**	%
Gain Drift[1]							
f_{OUT} = 100kHz		±25	±50		±15	±25	ppm/°C
f_{OUT} = 500kHz		±25	**±50**		±15	**±25**	ppm/°C
f_{OUT} = 2MHz		±25	**±75**		±15	**±50**	ppm/°C
Power Supply Rejection		0.001	**0.01**		0.001	**0.01**	%/V
Linearity Error							
f_{OUT} = 100kHz		±0.002	±0.02		±0.002	±0.005	%
f_{OUT} = 500kHz		±0.002	**±0.02**		±0.002	**±0.005**	%
f_{OUT} = 1MHz		±0.01	±0.02		±0.002	±0.005	%
f_{OUT} = 2MHz		±0.02	**±0.05**		±0.01	**±0.02**	%
Offset[2]		±1	**±4.5**		±1	**±2.5**	mV
(Transfer Function, RTI)							
Offset Drift		±10	**±50**		±10	**±30**	µV/°C
FREQUENCY-TO-VOLTAGE MODE							
Gain Error							
f_{IN} = 100kHz FS		±0.5	±1		±0.25	±0.5	%
Linearity Error							
f_{IN} = 100kHz FS		±0.002	±0.02		±0.002	±0.01	%
Input Resistor	19.8	20.0	20.2	19.8	20.0	20.2	kΩ
Temperature Coefficient		±20	**±50**		±20	**±50**	ppm/°C
INTEGRATOR OP AMP							
Input Bias Current							
Inverting Input (Pin 5)		±8	**±20**		±8	**±20**	nA
Noninverting Input (Pin 6)		40	**100**		40	**100**	nA
Input Offset Current		40	**120**		40	**120**	nA
Input Offset Voltage		±1	**±4**		±1	**±2**	mV
Open Loop Gain		86			86		dB
Common Mode Input Range	**−10**		**10**	**−10**		**10**	V
Output Voltage Range	**−1**		**(+V_S−4)**	**−1**		**(+V_S−4)**	V
(Referred to Pin 6, R_L > = 5k)							
COMPARATOR							
Input Bias Current		0.5	**5**		0.5	**5**	µA
Common Mode Voltage	$-V_S+4$		$+V_S-4$	$-V_S+4$		$+V_S-4$	V
CLOCK INPUT							
Maximum Frequency	**4**	5		**4**	5		MHz
Threshold Voltage		1.4			1.4		V
T_{min}-T_{max}	**0.8**		**2.0**	**0.8**		**2.0**	V
(Referred to Pin 12)							
Input Current							
($-V_S<V_{CLK}<+V_S$)		5	**20**		5	**20**	µA
Voltage Range	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL}<0.8V			**15**			**15**	mA
V_{OL}<0.4V, T_{min}-T_{max}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**100**	150	**200**	**100**	150	**200**	ns
Fall Time (Load = 500pF and I_{SINK} = 5mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width							
C_{OS} = 300pF	**1**	1.5	**2**	1	1.5	2	µs
C_{OS} = 1000pF	4	5	6	4	5	6	µs

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	AD651AQ/SQ			AD651BQ			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
REFERENCE OUTPUT							
Voltage	5.4	6.8	8.2	5.4	6.8	8.2	V
Drift		50	100		25	50	ppm/°C
POWER SUPPLY							
Rated Voltage		±15			±15		V
Operating Range							
Dual Supplies	±6	±15	±18	±6	±15	±18	V
Single Supply ($-V_S = 0$)	+12		+36	+12		+36	V
Quiescent Current		±9	±15		±9	±15	mA
Digital Common	$-V_S$		$+V_S-4$	$-V_S$		$+V_S-4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
"Q" Package	−25		+85	−25		+85	°C
"SQ" Grade	−55		+125				°C

NOTES
[1]Gain Drift is the average drift from T_{min} to T_{max}, and is measured at +25°C, T_{min} and T_{max}.
[2]Offset is guaranteed adjustable to zero using a 20K potentiometer on pins 2 and 3 with the wiper connected to $+V_S$ through a 250k resistor.
Specifications in **boldface** are 100% tested at final test and are used to measure outgoing quality levels.
Specifications subject to change without notice.

3

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage (Figure 6) 36V
Maximum Output Current (Open Collector Output) . . 50mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Storage Temperature Range: Cerdip . . . . −65°C to +150°C

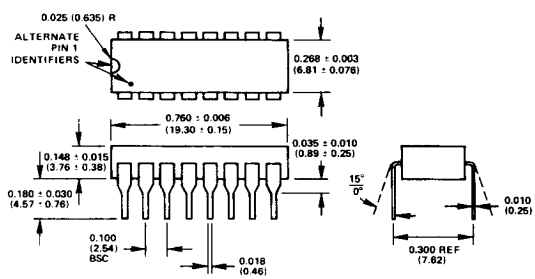
ORDERING GUIDE

Part Number	Gain Drift ppm/°C 100kHz	1MHz Linearity %	Specified Temperature Range °C	Package
AD651AQ	50 max	0.02 max	−25 to +85	Cerdip
AD651BQ	25 max	0.005 max	−25 to +85	Cerdip
AD651SQ	50 max	0.02 max	−55 to +125	Cerdip

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

"Q" PACKAGE
16-Pin CERDIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

DEFINITIONS OF SPECIFICATIONS

GAIN ERROR – The gain of a voltage-to-frequency converter is that scale factor setting that provides the nominal conversion relationship, e.g. 1MHz full scale. The "gain error" is the difference in slope between the actual and ideal transfer functions for the V-F converter.

LINEARITY ERROR – The "linearity error" of a V-F is the deviation of the actual transfer function from a straight line passing through the endpoints of the transfer function.

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THEORY OF OPERATION

A synchronous VFC is similar to other voltage-to-frequency converters in that an integrator is used to perform a charge-balance of the input signal with an internal reference current. However, rather than using a one-shot as the primary timing element which requires a high quality and low drift capacitor, a synchronous voltage-to-frequency converter (SVFC) uses an external clock; this allows the designer to determine the system stability and drift based upon the external clock selected. A crystal oscillator may also be used if desired.

The SVFC architecture provides other system advantages besides low drift. If the output frequency is measured by counting pulses gated to a signal which is derived from the clock, the clock stability is unimportant and the device simply performs as a voltage controlled frequency divider, producing a high resolution A/D. If a large number of inputs must be monitored simultaneously in a system, the controlled timing relationship between the frequency output pulses and the user supplied clock greatly simplifies this signal acquisition. Also, if the clock signal is provided by a VFC, then the output frequency of the SVFC will be proportional to the product of the two input voltages. Hence, multiplication and A-to-D conversion on two signals are performed simultaneously.

The pinout of the AD651 SVFC is shown in Figure 1. A block diagram of the device configured as a SVFC, along with various system waveforms, is shown in Figure 2.

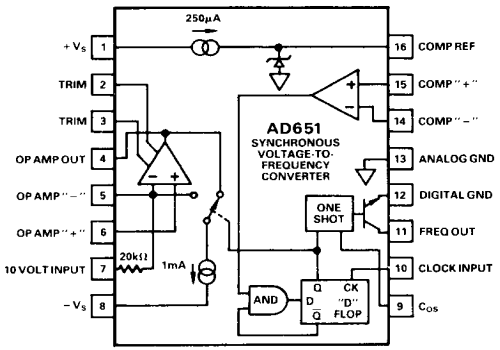

Figure 1. AD651 Pin Configuration

Figure 2 shows the typical up-and-down ramp integrator output of a charge-balance VFC. After the integrator output has crossed the comparator threshold and the output of the AND gate has gone high, nothing happens until a negative edge of the clock comes along to transfer the information to the output of the D-FLOP. At this point, the clock level is low, so the latch does not change state. When the clock returns high, the latch output goes high and drives the switch to reset the integrator. At the same time the latch drives the AND gate to a low output state. On the very next negative edge of the clock the low output state of the AND gate is transferred to the output of the D-FLOP and then when the clock returns high, the latch output goes low and drives the switch back into the Integrate Mode. At the same time the latch drives the AND gate to a mode where it will truthfully relay the information presented to it by the comparator.

Since the reset pulses applied to the integrator are exactly one clock period long, the only place where drift can occur is in a variation of the symmetry of the switching speed with temperature. Since each reset pulse is identical to every other, the AD651 SVFC produces a very linear voltage to frequency transfer relation. Also, since all of the reset pulses are gated by the clock, there are no problems with dielectric absorption causing the duration of a reset pulse to be influenced by the length of time since the last reset.

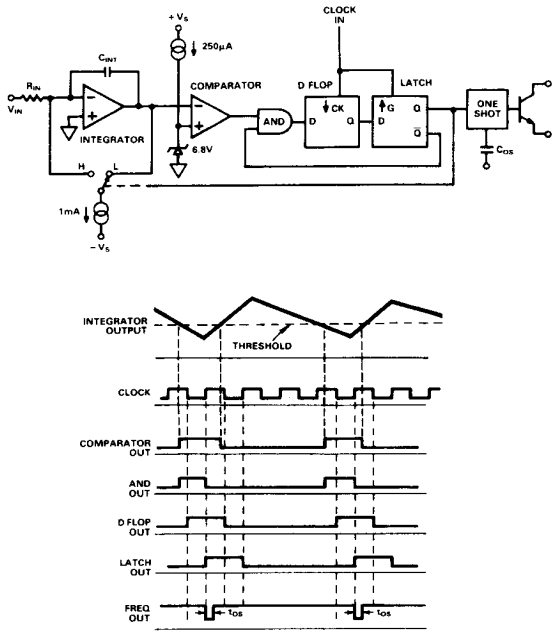

Figure 2. AD651 Block Diagram and System Waveforms

Referring to Figure 2, it can be seen that the period between output pulses is constrained to be an exact multiple of the clock period. Consider an input current of exactly one quarter of the value of the reference current. In order to achieve a charge balance, the output frequency will equal the clock frequency divided by four; one clock period for reset and three clock periods of integrate. This is shown in Figure 3. If the input current is increased by a very small amount, the output frequency should also increase by a very small amount. Initially, however, no output change is observed for a very small increase in the input current. The output frequency continues to run at one quarter of the clock, delivering an average of 250μA to the

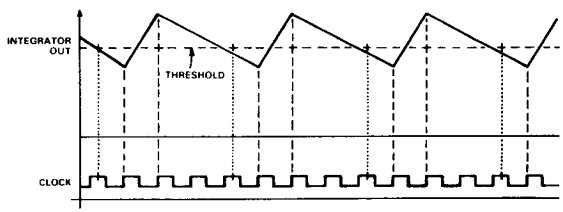

Figure 3. Integrator Output for I_{IN} = 250μA

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summing junction. Since the input current is slightly larger than this, charge accumulates in the integrator and the sawtooth signal starts to drift downward. As the integrator sawtooth drifts down, the comparator threshold is crossed earlier and earlier in each successive cycle, until finally, a whole cycle is lost. When the cycle is lost, the Integrate Phase lasts for two periods of the clock instead of the usual three periods. Thus, among a long string of divide-by-four's an occasional divide-by-three occurs; the average of the output frequency is very close to one quarter of the clock, but the instantaneous frequency can be very different. Because of this, it is very difficult to observe the waveform on an oscilloscope. During all of this time, the signal at the output of the integrator is a sawtooth wave with an envelope which is also a sawtooth. This is shown in Figure 4.

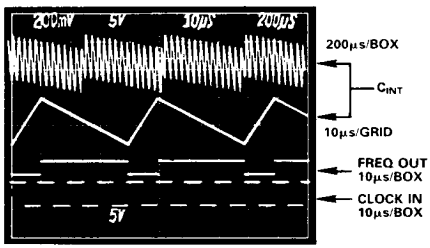

Figure 4. Integrator Output for I_{IN} Slightly Greater than 250μA

Another way to view this is that the output is a frequency of approximately one quarter of the clock that has been phase modulated. A constant frequency can be thought of as accumulating phase linearly with time at a rate equal to $2\pi f$ radians per second. Hence, the average output frequency which is slightly in excess of a quarter of the clock will require phase accumulation at a certain rate. However, since the SVFC is running at exactly one quarter of the clock, it will not accumulate enough phase (see Figure 5). When the difference between the required phase (average frequency) and the actual phase equals 2π, a step in phase is taken where the deficit is made up instantaneously. The output frequency is then a steady carrier which has been phase modulated by a sawtooth signal (see Figure 5). The period of the sawtooth phase modulation is the time required to accumulate a 2π difference in phase between the required average frequency and one quarter of the clock frequency. The amplitude of the sawtooth phase modulation is 2π.

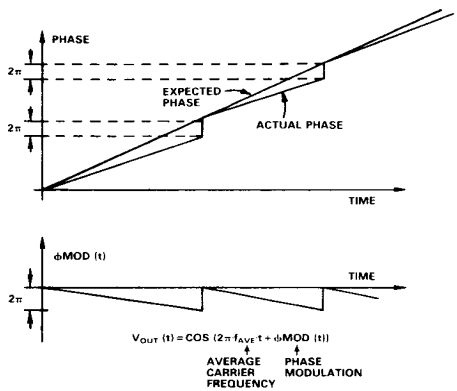

Figure 5. Phase Modulation

The result of this synchronism is that the rate at which data may be extracted from the series bit stream produced by the SVFC is limited. The output pulses are typically counted during a fixed gate interval and the result is interpreted as an average frequency. The resolution of such a measurement is determined by the clock frequency and the gate time. For example, if the clock frequency is 4MHz and the gate time is 4.096ms, then a maximum count of 8,192 is produced by a full-scale frequency of 2MHz. Thus, the resolution is 13 bits.

OVERRANGE

Since each reset pulse is only one clock period in length, the full-scale output frequency is equal to one-half the clock frequency. At full scale the current steering switch spends half of the time on the summing junction; thus, an input current of 0.5mA can be balanced. In the case of an overrange, the output of the integrator op amp will drift in the negative direction and the output of the comparator will remain high. The logic circuits will then simply settle into a "divide-by-two" of the clock state.

SVFC CONNECTION FOR DUAL SUPPLY, POSITIVE INPUT VOLTAGES

Figure 6 shows the AD651 connection scheme for the traditional dual supply, positive input mode of operation. The $\pm V_S$ range is from ±6 to ±18 volts. When $+V_S$ is lower than 9 volts, it is necessary to shunt pin 16 to pin 13 in order to maintain a minimum of 2 volts between pin 16 and $+V_S$. Pin 16 may be shorted directly to pin 13, or an external resistor may be shunted between the two pins. Shorting these pins will make analog ground the comparator reference; in this case pins 16 and 15 are tied directly to pin 13. If an external resistor is used then the comparator reference will be set by the 250μA current and this resistor.

The diode (IN4148 or similar) across pins 5 and 6 prevents any parasitic internal junctions from becoming forward biased under fault conditions. Opaque diodes should be used to prevent variances in the AD651 transfer function caused by photo injection.

The AD651 accepts either a 0 to 10V or 0 to 0.5mA full-scale input signal. The temperature drift of the AD651 is specified

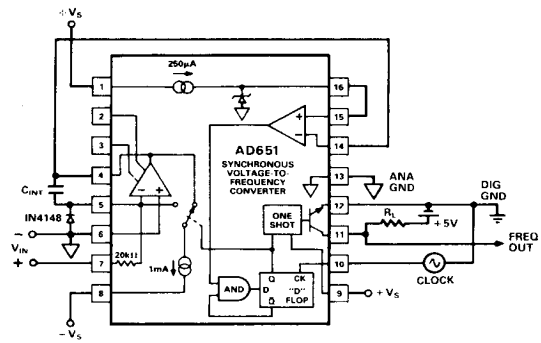

Figure 6. Standard V/F Connection for Positive Input Voltage with Dual Supply

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for a 0 to 10V input range using the internal 20kΩ resistor. If a current input is used, the gain drift will be degraded by approximately 50ppm/°C (the TC of the 20kΩ resistor). If an external resistor is connected to pin 5 to establish a different input voltage range, drift will be induced to the extent that the external resistor's TC differs from −50ppm/°C. The external resistor used to establish a different input voltage range should be selected as to provide a full-scale current of 0.5mA (i.e., 10kΩ for 0 to 5V).

SVFC CONNECTIONS FOR NEGATIVE INPUT VOLTAGES

Voltages which are negative with respect to ground may be used as the input to the AD651 SVFC. In this case, pin 7 is grounded and the input voltage is applied to pin 6 (see Figure 7). In this mode the input voltage can go as low as 4 volts above $-V_S$. In this configuration the input is a high impedance, and only the 40nA (typical) input bias current of the op amp need be supplied by the input signal. This is contrasted with the more usual positive input voltage configuration, which has a 20kΩ input impedance and requires 0.5mA from the signal source.

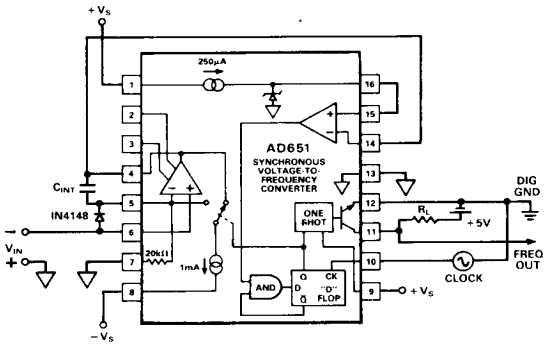

Figure 7. Negative Voltage Input

SVFC CONNECTION FOR BIPOLAR INPUT VOLTAGES

A bipolar input voltage of ±5V can be accommodated by injecting a 250μA current into pin 5. A −5V signal will then provide a zero sum current at the integrator summing junction which will result in a zero output frequency, while a +5V signal will provide a 0.5mA (full- scale) sum current which will result in the full-scale output frequency.

The 250μA bipolar offset current is best provided by an external reference voltage and resistor. However, if necessary, the comparator reference may be used. Since the current source feeding the zener diode is only 250μA, it is necessary to provide an additional 250μA from $+V_S$ for the bipolar offset current. This is shown in Figure 8.

GAIN AND OFFSET CALIBRATION

The gain error of the AD651 is laser trimmed to within ±0.5%. If higher accuracy is required, the internal 20kΩ resistor must be shunted with a 2MΩ resistor to produce a parallel equivalent which is 1% lower in value than the nominal 20kΩ. Full scale adjustment is then accomplished using a 500Ω series trimmer. See Figure 9. When negative input voltages are used, this 500Ω trimmer will be tied to ground and pin 6 will be the input pin.

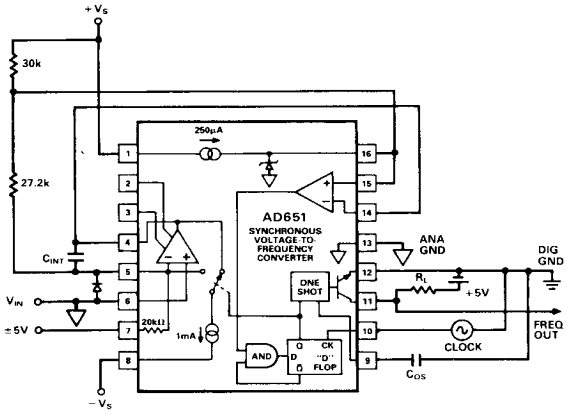

Figure 8. Bipolar Offset

This gain trim should be done with an input voltage of 9V, and the output frequency should be adjusted to exactly 45% of the clock frequency. Since the device settles into a divide-by-two mode for an input overrange condition, adjusting the gain with a 10V input is impractical; the output frequency would be exactly one-half the clock frequency if the gain were too high and would not change with adjustment until the exact proper scale factor was achieved. Hence, the gain adjustment should be done with a 9V input.

The offset voltage of the op amp may be trimmed to zero with a 20kΩ potentiometer across pins 2 and 3 and the wiper connected to $+V_S$ through a 250kΩ resistor. This is also shown in Figure 9. The offset is then trimmed by grounding pin 7 and observing the waveform at pin 4. If the offset voltage of the op amp is positive, then the integrator will have saturated and the voltage at pin 4 will be at the positive rail. If the offset voltage is negative, then there will be a small effective input current that will cause the AD651 to oscillate and a sawtooth waveform will be observed at pin 4. The trimpot should be adjusted until the downward slope of this sawtooth becomes very slow, down to a frequency of 1Hz or less.

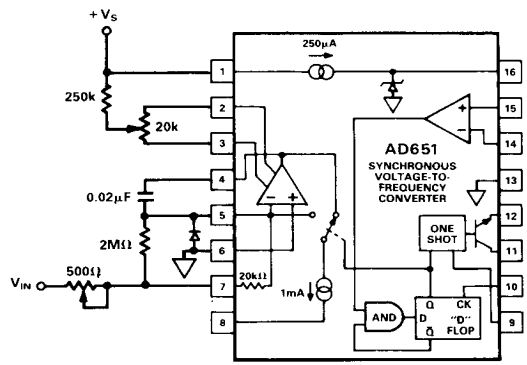

Figure 9. Gain and Offset Trim

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GAIN PERFORMANCE

The AD651 gain error is specified as the difference in slope between the actual and the ideal transfer function over the full-scale frequency range. Figure 10 shows a plot of the typical gain error changes vs. the clock input frequency, normalized to 100kHz. If after using the AD651 with a full-scale clock frequency of 100kHz it is decided to reduce the necessary gating time by increasing the clock frequency, this plot shows the typical gain changes normalized to the original 100kHz gain.

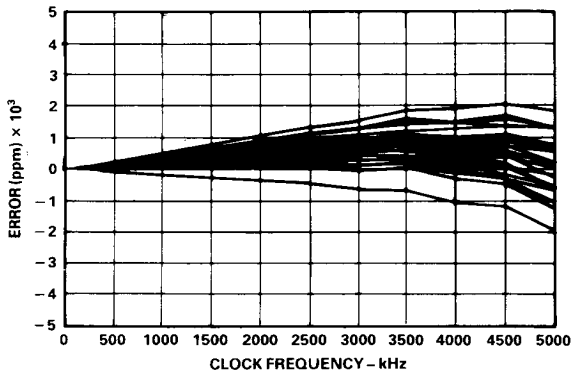

Figure 10. Gain vs. Clock Input

DIGITAL INTERFACING CONSIDERATIONS

The AD651 clock input is a high impedance input with a threshold voltage of two diode voltages with respect to Digital Ground at pin 12 (approximately 1.2 volts at room temp). When the clock input is low, 5-10μA flows out of this pin. When the clock input is high, no current flows.

The frequency output is an open collector pull-down and is capable of sinking 8mA with a maximum voltage of 0.4 volts. This will drive 5 standard TTL inputs. The open collector pull up voltage can be as high as 36 volts above digital ground.

COMPONENT SELECTION

The AD651 integrating capacitor should be 0.02μF. If a large amount of normal mode interference is expected (more than 0.1 volts) and the clock frequency is less than 500kHz, an integrating capacitor of 0.1μF should be used. Mylar, polypropylene, or polystyrene capacitors should be used.

The open collector pull-up resistor should be chosen to give adequately fast rise times. At low clock frequencies (100kHz) larger resistor values (several kΩ) and slower rise times may be tolerated. However, at higher clock frequencies (1MHz) a lower value resistor should be used. The loading of the logic input which is being driven must also be taken into consideration. For example, if 2 standard TTL loads are to be driven then a 3.2mA current must be sunk, leaving 4.8mA for the pull-up resistor if the maximum low level voltage is to be maintained at 0.4 volts. A 960Ω resistor would thus be selected ((5–0.4)V/4.8mA) = 960Ω.

The one-shot capacitor controls the pulse width of the frequency output. The pulse is initiated by the rising edge of the clock signal. The delay time between the rising edge of the clock and the falling edge of the frequency output is typically 150ns. The width of the pulse is 5ns/pF and the minimum width is about 100ns with pin 9 floating. If the one-shot period is accidentally chosen longer than the clock period, the width of the pulse will default to equal the clock period. The one-shot can be disabled by connecting pin 9 to $+V_S$ (Figure 11); the output pulse width will then be equal to the clock period. The one-shot is activated (Figure 12) by connecting a capacitor from pin 9 to $+V_S$, $-V_S$, or Digital Ground($+V_S$ is preferred).

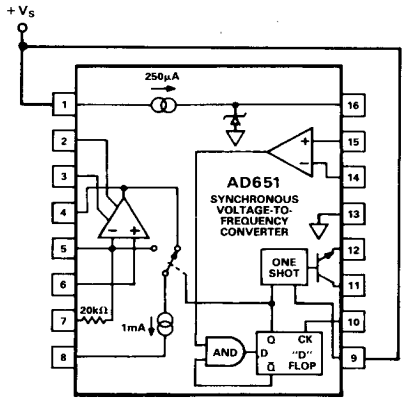

Figure 11. One Shot Disabled

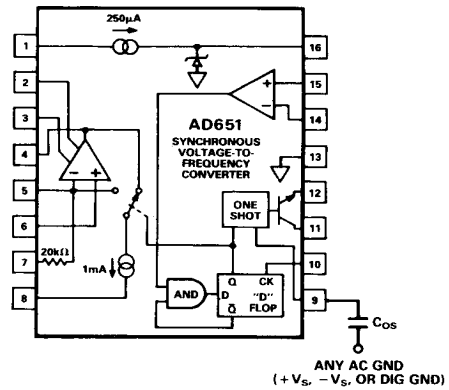

Figure 12. One Shot Enabled

DIGITAL GROUND

Digital Ground can be at any potential between $-V_S$ and ($+V_S$ -4 volts). This can be very useful a system with derived grounds rather than stiff supplies. For example, in a small isolated power circuit, often only a single supply is generated and the "ground" is set by a divider tap. Such a ground cannot handle the large currents associated with digital signals. With the AD651 SVFC, it is possible to connect the DIG GND to $-V_S$ for a solid logic reference, as shown in Figure 13.

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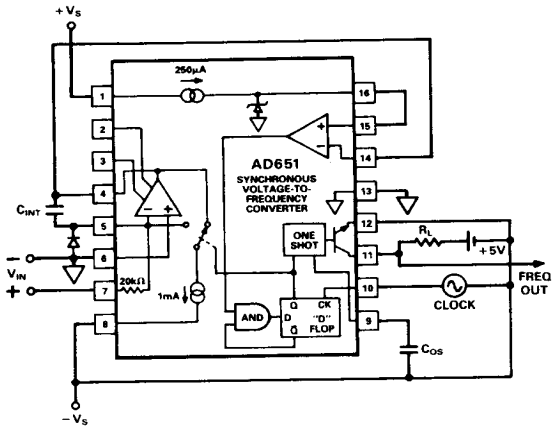

Figure 13. Digital GND at $-V_S$

SINGLE SUPPLY OPERATION

In addition to the Digital Ground being connected to $-V_S$, it is also possible to connect Analog Ground to $-V_S$ of the AD651. Hence, the device is truly operating from a single supply voltage that can range from $+12V$ to $+36V$. This is shown in Figure 14 for a positive voltage input and Figure 15 for a negative voltage input.

In Figure 14, the comparator reference is used as a derived ground, and the input voltage is referred to this point as well as the op amp common mode (pin 6 is tied to pin 16). It is necessary to place a pull up resistor between pin 16 and $+V_S$ to provide at least 0.5mA of current into pin 16. Since the input signal source must drive 0.5mA of full-scale signal current into pin 7, it must also draw the exact same current from the input reference potential. Since the internal current source driving the zener diode comparator reference is only 250μA, it cannot supply the current needed; hence the reason for the pull-up resistor between pin 16 and $+V_S$. The exact amount of extra current that must be supplied by the external resistor is not critical, so long as it is more than the 0.5mA full-scale signal current.

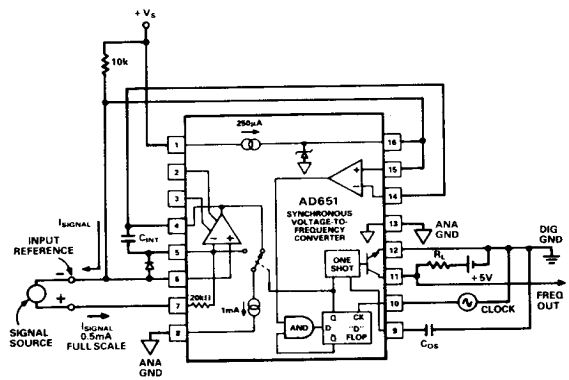

Figure 14. Single Supply Positive Voltage Input

Figure 15 shows the negative voltage input configuration for use of the AD651 in the single supply mode. Again, an external resistor is needed to supply the signal current being drawn out of the input reference. However, in this mode the signal source is driving the "+" input of the op amp which requires only 40nA (typical), rather than the 0.5mA required in the positive input voltage configuration. The voltage at pin 6 may go as low as 4 volts above ground ($-V_S$, pin 8). Since the input reference is about 6.5 volts above ground, this leaves a 2.5V window for the input signal. In order to drive the integrating capacitor with a 0.5mA full-scale current, it is necessary to shunt the internal 20kΩ resistor with an external 5kΩ resistor. This results in a 4kΩ equivalent resistor and a 2V input range. The external 5kΩ resistor should be a low-TC metal-film type for lowest drift degradation.

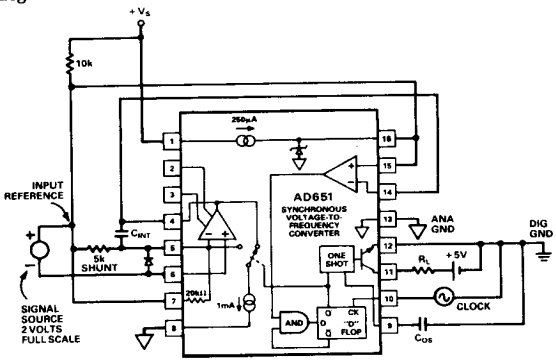

Figure 15. Single Supply Negative Voltage Input

FREQUENCY-TO-VOLTAGE CONVERTER

The AD651 SVFC also works as a frequency-to-voltage converter. Figure 16 shows the connection diagram for F/V conversion. In this case the "−" input of the comparator is fed the input pulses. Either comparator input may be used so that an input pulse of either polarity may be applied to the F/V. In Figure 16 the "+" input is tied to a 1.2V reference and low level TTL pulses are used as the frequency input. The pulse must be low on the falling edge of the clock. On the subsequent rising edge the 1mA current source is switched to the integrator summing junction and ramps up the voltage at pin 4. Due to the action of the AND gate, the 1mA current is switched off after only one clock period. The average current delivered to the summing junction varies from 0 to 0.5mA; using the internal 20kΩ resistor this results in a full-scale output voltage of 10V at pin 4.

The frequency response of the circuit is determined by the capacitor; the −3dB frequency is simply the RC time constant. A tradeoff exists between ripple and response. If low ripple is desired, a large value capacitor must be used (1μF), if fast response is needed, a small capacitor is used (1nF minimum).

The op amp can drive a 5kΩ resistor load to 10V, using a 15V positive power supply. If a large load capacitance (0.01μF) must be driven, then it is necessary to isolate the load with a 50Ω resistor as shown. Since the 50Ω resistor is 0.25% of the full scale, and the specified gain error with the 20kΩ resistor is ±0.5%, this extra resistor will only increase the total gain error to +0.75% max.

The circuit shown is unipolar and only a 0 to +10V output is allowed. The integrator op amp is not a general purpose op amp, rather it has been optimized for simplicity and high speed.

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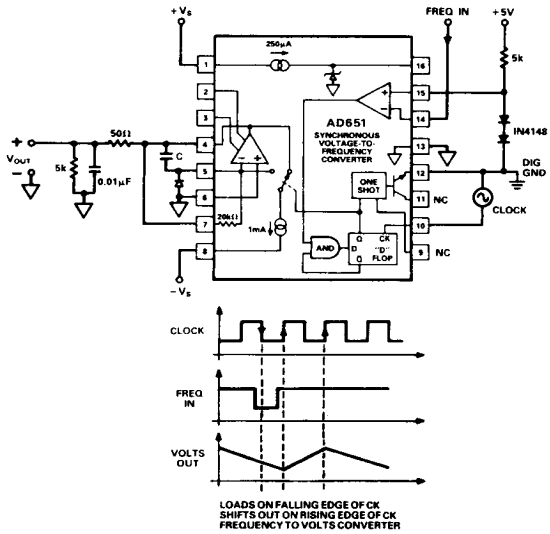

Figure 16. Frequency-to-Voltage Converter

The most significant difference between this amplifier and a general purpose op amp is the lack of an integrator (or level shift) stage. Consequently, the voltage on the output (pin 4) must always be more positive than 1 volt below the inputs (pins 6 and 7). For example, in the F-to-V conversion mode, the noninverting input of the op amp (pin 6) is grounded which means that the output (pin 4) cannot go below −1 volt. Normal operation of the circuit as shown will never call for a negative voltage at the output.

A second difference between this op amp and a general purpose amplifier is that the output will only sink 1.5mA to the negative supply. The only pulldown other than the 1mA current used for voltage-to-frequency conversion is a 0.5mA source. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 4 volts of the positive supply when not sourcing external current. When sourcing 10mA, the output voltage may be driven to within 6 volts of the positive supply.

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD651.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD651 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD651.

Separate digital and analog grounds are provided on the AD651. The emitter of the open collector frequency output transistor and the clock input threshold only are returned to the digital ground. Only the comparator reference zener diode is connected to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. Much noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At high full scale, it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA. This much current being switched will cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD651 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD651 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground, pin 12. The pull-up resistor should be connected directly to the frequency output, pin 11. The lead lengths on the bypass capacitor and the pull-up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull-up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 12) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current. There may be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause a problem. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 6) at the package. More information on proper grounding and reduction of interference can be found in reference 1.

[1]"Noise Reduction Techniques in Electronic Systems", by H.W. Ott, (John Wiley, 1976).

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Applications

FREQUENCY OUTPUT MULTIPLIER

The AD651 can serve as a frequency output multiplier when used in conjunction with a standard voltage-to-frequency converter. Figure 17 shows the low cost AD654 VFC being used as the clock input to the AD651. Also shown is a second AD651 in the F/V mode. The AD654 is set up to produce an output frequency of 0-500kHz for an input voltage (V_1) range of 0-10V. The use of R4, C1, and the XOR gate doubles this output frequency from 0-500kHz to 0-1MHz.

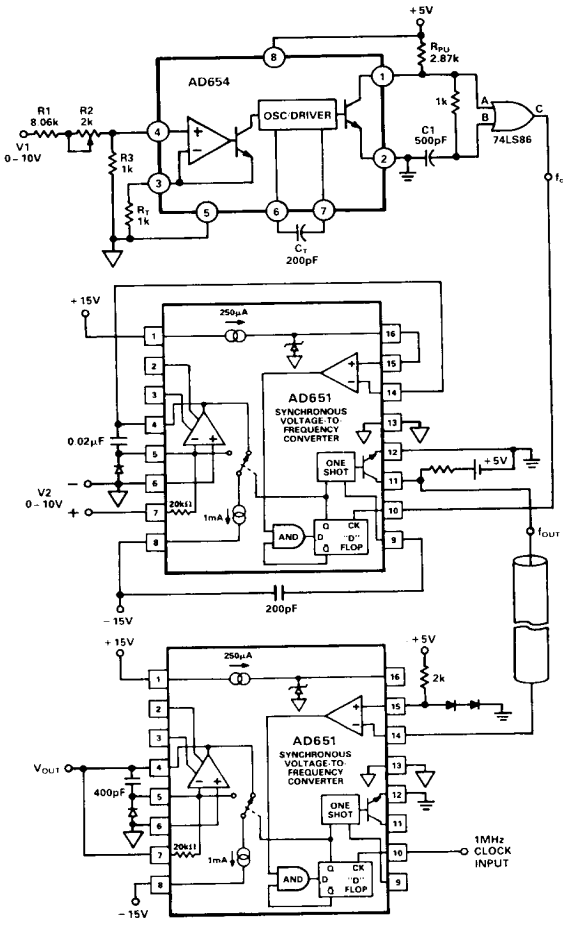

Figure 17. Frequency Output Multiplier

This 1MHz full-scale frequency is then used as the clock input to the AD651 SVFC. Since the AD651 full-scale output frequency is one-half the clock frequency, the 1MHz FS clock frequency establishes a 500kHz maximum output frequency for the AD651 when its input voltage (V_2) is +10V. The user thus has an output frequency range from 0-500kHz which is proportional to the product of V_1 and V_2.

This can be shown in equation form, where f_C is the AD654 output frequency and f_{OUT} is the AD651 output frequency:

$$f_C = V_1 \frac{1MHz}{10V}$$

$$f_{OUT} = V_2 \left(\frac{f_C/2}{10V}\right)$$

$$f_{OUT} = V_1 V_2 \left(\frac{1MHz}{2(10V)\,(10V)}\right)$$

$$f_{OUT} = V_1 \cdot V_2 \cdot 5kHz/V^2$$

The scope photo in Figure 18 shows V_1 and V_2 (top two traces) and the output of the F-V (bottom trace).

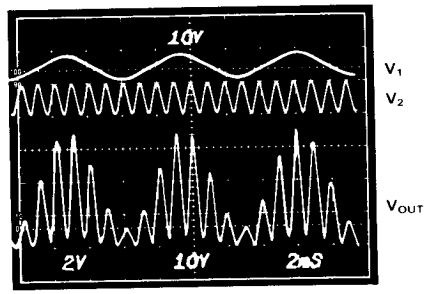

Figure 18. Multiplier Waveforms

SINGLE-LINE MULTIPLEXED DATA TRANSMISSION

It is often necessary to measure several different signals and relay the information to some remote location using a minimum amount of cable. Multiple AD651 SVFC devices may be used with a multiphase clock to combine these measurements for serial transmission and demultiplexing. Figure 19 shows a block diagram of a single-line multiplexed data transmission system with high noise immunity. Figures 20, 21 and 22 show the SVFC multiplexer, a representative means of data transmission, and an SVFC demultiplexer respectively.

Multiplexer

Figure 20 shows the SVFC multiplexer. The clock inputs for the several SVFC channels are generated by a TIM9904A four phase clock driver, and the frequency outputs are combined by strapping all the frequency output pins together (a "wire or" connection). The one-shot in the AD651 sets the pulse width of the frequency output pulses to be slightly shorter than one quarter of the clock period. Synchronization is achieved by applying one of the four available phases to a fixed TTL one-shot ('121) and combining the output with an external transistor. The width of this sync pulse is shorter than the width of the frequency output pulses to facilitate decoding the signal. The RC lag network on the input of the one-shot provides a slight delay between the rising edge of the clock and the sync pulse in order to match the 150ns delay of the AD651 between the rising edge of the clock and the output pulse.

Transmitter

The multiplexer signal can be transmitted in any manner suitable to the task at hand. A pulse transformer or an opto-isolator can

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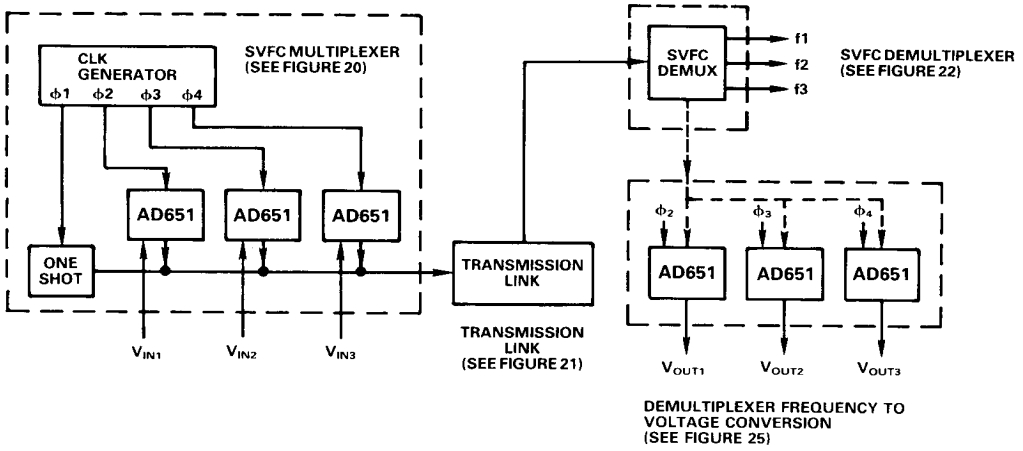

Figure 19. Single Line Multiplexed Data Transmission Block Diagram

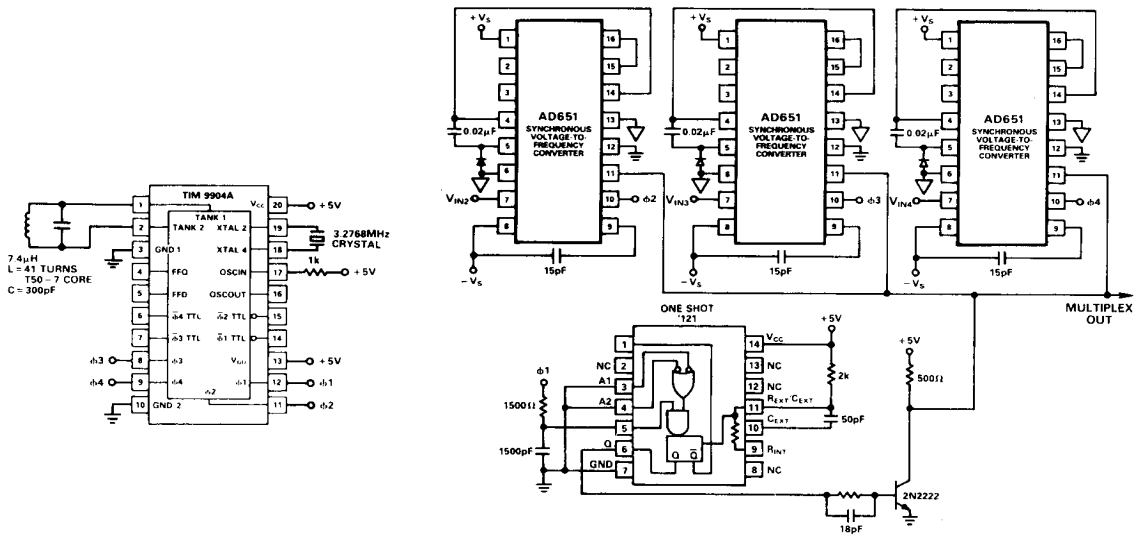

Figure 20. SVFC Multiplexer

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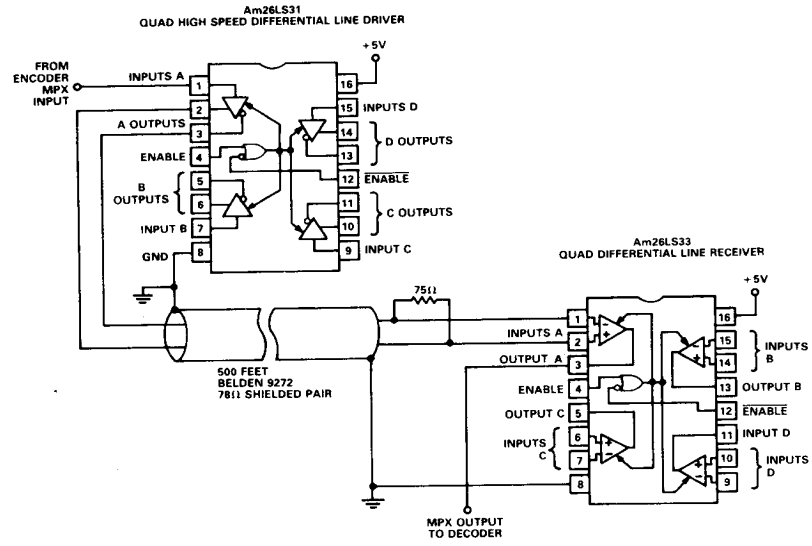

Figure 21. RS-422 Standard Data Transmission

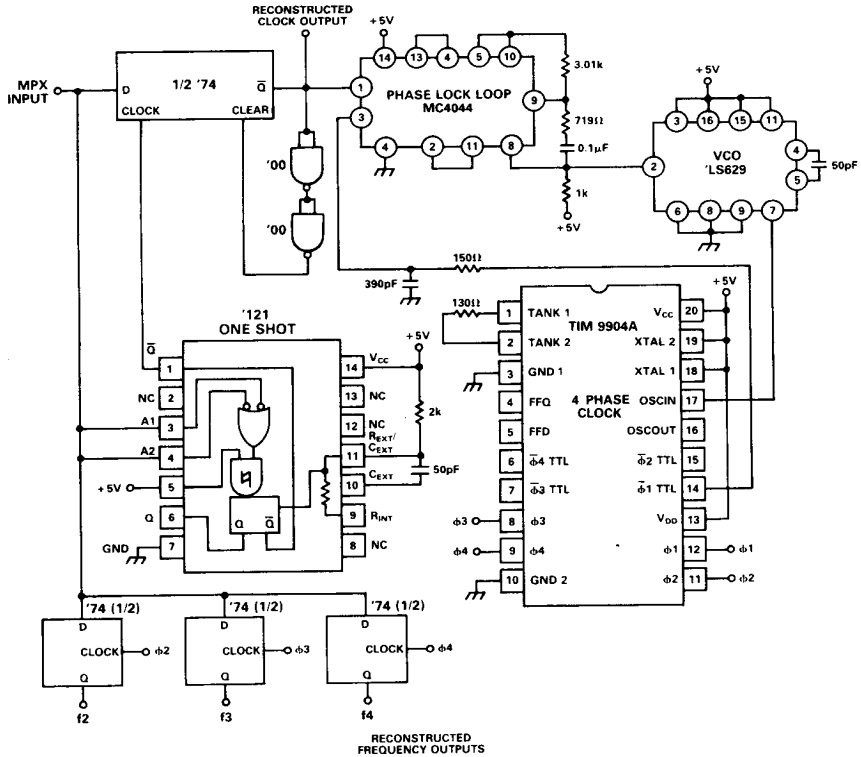

Figure 22. SVFC Demultiplexers

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provide galvanic isolation; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The circuit shown in Figure 21 uses an EIA RS-422 standard for digital data transmission over a balanced line. Figure 23 shows the waveforms of the four clock phases and the multiplex output signal. Note that the sync pulse is present every clock cycle, but the data pulses are no more frequent than every other clock cycle since the maximum output frequency from the SVFC is half the clock frequency. The clock frequency used in this circuit is 819.2 kHz and will provide more than 16 bits of resolution if 100 millisecond gate time is allowed for counting pulses of the decoded output frequencies.

SVFC Demultiplexer

The demultiplexer needed to separate the combined signals is shown in Figure 22. A phase locked loop drives another four phase clock chip to lock onto the reconstructed clock signal. The sync pulses are distinguished from the data pulses by their shorter duration. Each falling edge on the multiplex input signal triggers the one-shot, and at the end of this one-shot pulse the multiplex input signal is sampled by a D-type flip-flop. If the signal is high, then the pulse was short (a sync pulse) and the $\overline{Q}$ output of the D-flop goes low. The D-flop is cleared a short time (two gate delays) later, and the clock is reconstructed as a stream of short, low-going pulses. If the Multiplex input is a data pulse, then when the D-flop samples at the end of the one-shot period, the signal will still be low and no pulse will appear at the reconstructed clock output. These waveforms are shown in Figure 24.

If it is desired to recover the individual frequency signals, then the multiplex input is sampled with a D-flop at the appropriate time as determined by the rising edge of the various phases generated by the clock chip. These frequency signals can be counted as a ratio relative to the reconstructed clock, so it is not even necessary for the transmitter to be crystal controlled as shown here.

Analog Signal Reconstruction

If it is desired to reconstruct the analog voltages from the multiplex signal, then three more AD651 SVFC devices are used as frequency-to-voltage converters, as shown in Figure 25. The comparator inputs of all the devices are strapped together, and the "+" inputs are held at a 1.2 volt TTL threshold, while the "−" inputs are driven by the multiplex input. The three clock inputs are driven by the ϕ outputs of the clock chip. Remember that data at the comparator input of the SVFC is loaded on the falling edge of the clock signal and shifted out on the next rising edge. Note that the frequency signals for each data channel are available at the frequency output pin of each FVC.

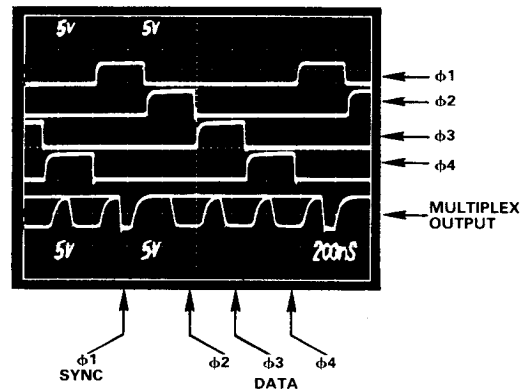

Figure 23. Multiplexer Waveforms

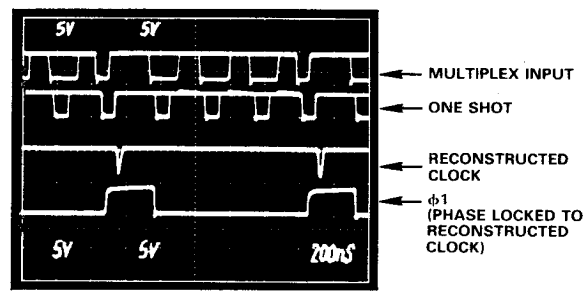

Figure 24. Demultiplexer Waveforms

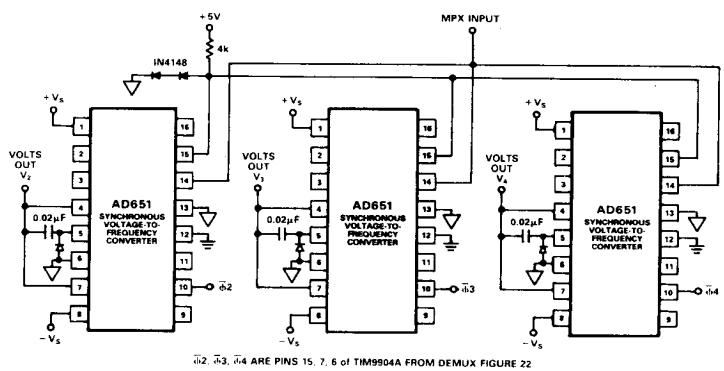

Figure 25. Demultiplexer Frequency-to-Voltage Conversion

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ISOLATED FRONT END

In some applications it may be necessary to have complete galvanic isolation between the analog signals being measured and the digital portions of the circuit. The circuit shown in Figure 26 runs off a single 5 volt power supply and provides a self-contained, completely isolated analog measurement system. The power for the AD651 SVFC is provided by a chopper and a transformer, and is regulated to ±15 volts.

Both the chopper frequency and the AD651 clock frequency are 125kHz, with the clock signal being relayed to the SVFC through the transformer. The frequency output signal is relayed through an opto-isolator and latched into a D-flop. The chopper frequency is generated from an AD654 VFC and is frequency divided by two to develop differential drive for the chopper transistors, and to ensure an accurate 50 percent duty cycle. The pull-up resistors on the D-flop outputs provide a well defined high level voltage to the choppers to equalize the drive in each direction. The 10μH inductor in the +5V lead of the transformer primary is necessary to equalize any residual imbalance in the drive on each half-cycle and thus prevent saturation of the core. The capacitor across the primary resonates the system so that under light loading conditions on the secondary the wave shape will be sinusoidal and the clock frequency will be relayed to the SVFC. To adjust the chopper frequency, disconnect any load on the secondary and tune the AD654 for a minimum in the supply current drawn from the 5 volt supply.

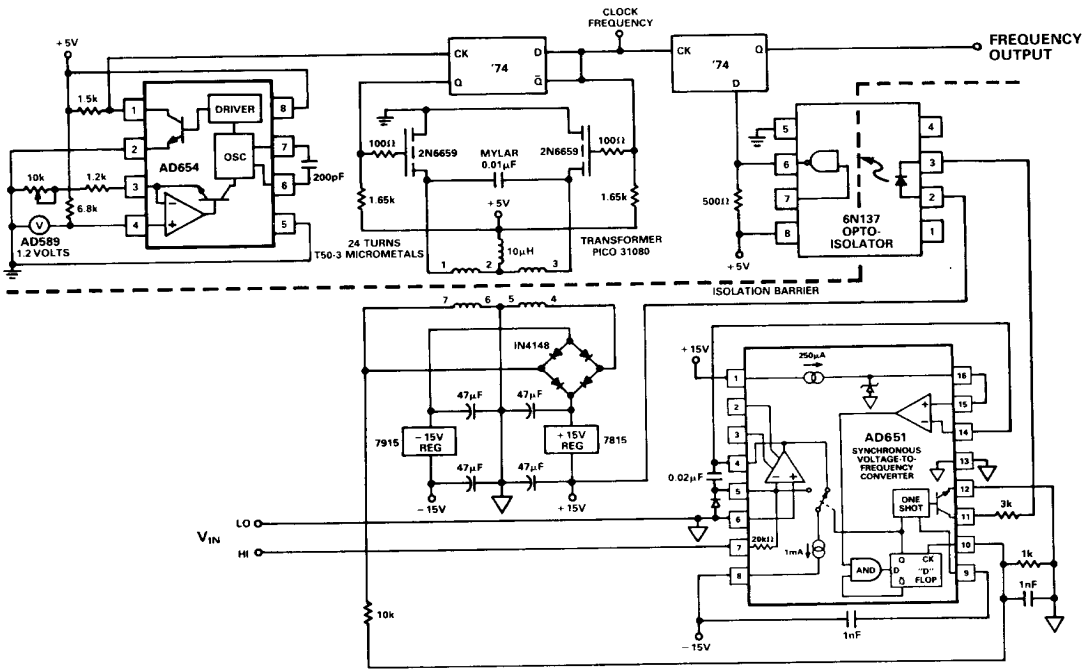

Figure 26. Isolated Synchronous VFC

A-TO-D CONVERSION

In performing an A-to-D conversion, the output pulses of a VFC are counted for a fixed gate interval. To achieve maximum performance with the AD651, the fixed gate interval should be generated using a multiple of the SVFC clock input. Counting in this manner will eliminate any errors due to the clock (whether it be jitter, drift with time or temperature, etc.) since it is the ratio of the clock and output frequencies that is being measured.

The resolution of the A-to-D conversion measurement is determined by the clock frequency and the gate time. If, for instance, a resolution of 12 bits is desired and the clock frequency is 1MHz (resulting in an AD651 FS frequency of 500kHz) the gate time will be:

$$\left(\frac{\text{FS Freq}}{N}\right)^{-1} = \left(\frac{1}{2}\frac{\text{Clock Freq}}{N}\right)^{-1} = \left(\frac{1\text{MHz}}{2(4096)}\right)^{-1}$$

$$= \frac{8192}{1\times 10^6}\ \text{sec} = 8.192\text{ms}$$

: Where N is the total number of codes for a given resolution.

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Figure 27 shows the AD651 SVFC as an A-to-D converter in block diagram form.

To provide the ÷ 2N block a single chip counter such as the 4020B can be used. The 4020B is a 14-stage binary ripple counter which has a clock and master reset for inputs, and buffered outputs from the first stage and the last eleven stages. The output of the first stage is $f_{CLOCK} \div 2^1 = f_{CLOCK}/2$, while the output of the last stage is $f_{CLOCK} \div 2^{14} = f_{CLOCK}/16384$. Hence using this single chip counter as the ÷ 2N block, 13-bit resolution can be achieved. Higher resolution can be achieved by cascading D-type flip-flops or another 4020B with the counter.

Table I shows the relationship between clock frequency and gate time for various degrees of resolution. Note that if the variables are chosen such that the gate times are multiples of 50, 60 or 400Hz, normal-mode rejection (NMR) of those line frequencies will occur.

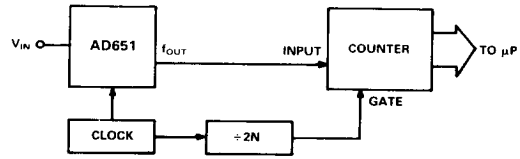

Figure 27. Block Diagram of SVFC A-to-D Converter

3

Resolution	N	Clock	Conversion or Gate Time	Typ Lin	Comments
12 Bits	4096	81.92kHz	100ms	0.002%	50, 60, 400Hz NMR
12 Bits	4096	2MHz	4.096ms	0.01%	
12 Bits	4096	4MHz	2.048ms	0.02%	
4 Digits	10000	200kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	327.68kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	1.966MHz	16.66ms	0.01%	60Hz NMR
14 Bits	16384	1.638MHz	20ms	0.01%	50Hz NMR
4 1/2 Digits	20000	400kHz	100ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	655.36kHz	200ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	4MHz	32.77ms	0.02%	

Table I.

DELTA MODULATOR

The circuit of Figure 28 shows the AD651 configured as a delta modulator. A reference voltage is applied to the input of the integrator (pin 7), which sets the steady state output frequency at one-half of the AD651 full-scale frequency (1/4 of the clock frequency). As a 0 to 10V input signal is applied to the comparator (pin 15), the output of the integrator attempts to track this signal. For an input in an idling condition (dc) the output frequency will be one-half full scale. For positive going signals the output frequency will be between one-half full scale and full scale, and for negative going signals the output frequency will be between zero and one-half full scale. The output frequency will correspond to the slope of the comparator input signal.

Since the output frequency corresponds to the slope of the input signal, the delta modulator acts as a differentiator. A delta modulator is thus a direct way of finding the derivative of a signal. This is useful in systems where, for example, a signal corresponding to velocity exists and it is desired to determine acceleration.

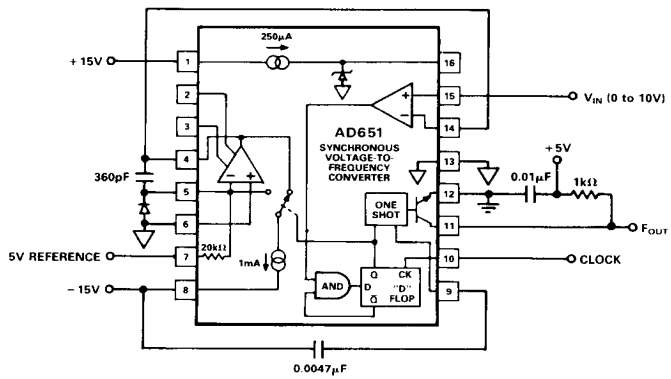

Figure 28. Delta Modulator

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Figure 29 is a scope photo showing a 20kHz, 0 to 10V sine wave used as the input to the comparator and its ramp-wise approximation at the integrator output. The clock frequency used as 2MHz and the integrating capacitor was 360pF. Figure 30 shows the same input signal and its ramp-wise approximation, along with the output frequency corresponding to the derivative of the input signal. In this case the clock frequency was 850kHz.

The choice of an integrating capacitor is primarily dictated by the input signal bandwidth. Figure 31 shows this relationship. It should be noted that as the value of C_{INT} is lowered, the ramp size of the integrator approximation becomes larger. This can be compensated for by increasing the clock frequency. The effect of the clock frequency on the ramp size is demonstrated in Figures 29 and 30.

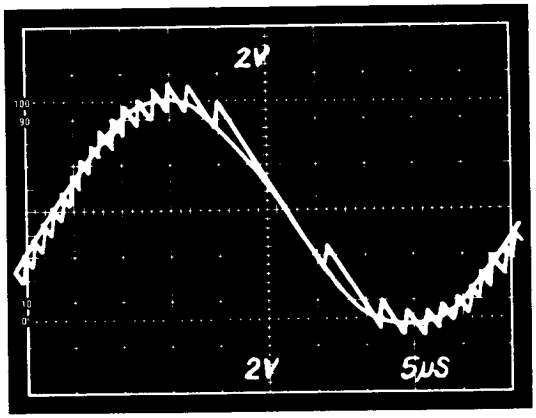

Figure 29. Delta Modulator Input Signal and Ramp-Wise Approximation

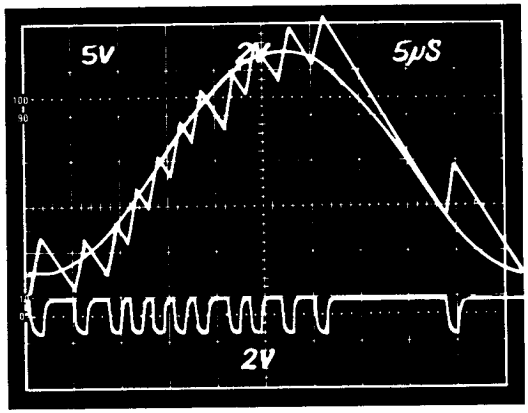

Figure 30. Delta Modulator Input Signal, Ramp-Wise Approximation and Output Frequency

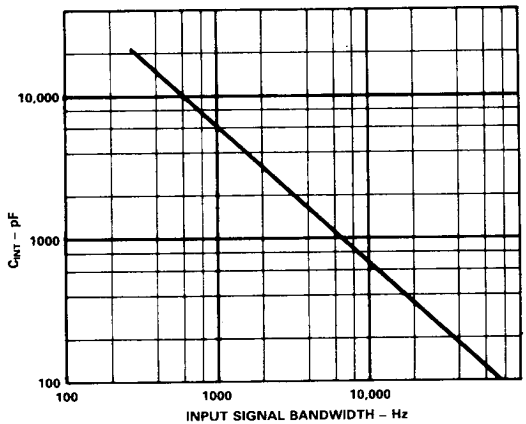

Figure 31. Maximum Integrating Cap Value vs. Input Signal Bandwidth

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