EL4501

Video Front End

FN7327
Rev 3.00
November 12, 2010

The EL4501 is a highly-integrated Video Front End (VFE) incorporating all of the key signal conditioning functions for analog video signals. It provides a flexible front-end interface for analog or analog/digital video sub-systems. The VFE contains a high bandwidth DC-restore, an advanced sync separator and a data slicer with an adjustable threshold, configurable output and power-down mode.

The VFE performs restoration of the DC level (blanking level) of a video signal and the recovery of all signal timing necessary for synchronization and control. Additionally, data embedded in the active video or VBI regions of the video signal may be extracted using the flexible data slicer incorporated into the VFE. The advanced sync separator exhibits excellent noise immunity by incorporating a digital brick wall filter and signal qualification algorithm. The DC-restored video amplifier is unity gain stable with an unloaded -3dB bandwidth of 100MHz. The input common mode voltage range extends from the negative rail to within 1.5V of the positive rail. When driving a 75Ω double terminated coaxial cable, the amplifier can drive to within 150mV of either rail. With 200V/µs slew rate, the amplifier is well suited for composite and component video applications.

The VFE operates from a single 5V supply from -40°C to +85°C and is available in a reduced footprint 24 Ld QSOP package.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL4501IU	EL4501IU	-	24 Ld QSOP	MDP0040
EL4501IU-T7	EL4501IU	7”	24 Ld QSOP	MDP0040
EL4501IU-T13	EL4501IU	13”	24 Ld QSOP	MDP0040
EL4501IUZ (See Note)	EL4501IUZ	-	24 Ld QSOP (Pb-free)	MDP0040
EL4501IUZ-T7 (See Note)	EL4501IUZ	7”	24 Ld QSOP (Pb-free)	MDP0040
EL4501IUZ-T13 (See Note)	EL4501IUZ	13”	24 Ld QSOP (Pb-free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- DC-restore and sync separator
- Wideband (100MHz) DC-restore
- Advanced sync separator
- Programmable data slicer
- Single 5V operation
- Diff gain/phase = 0.05%/0.03°, R_L = 10kΩ, A_V = 1
- Low power (<75mW)
- Pb-free plus anneal available (RoHS compliant)

Applications

- Video capture & editing
- Video projectors
- Set top boxes
- Security video
- Embedded data recovery

Pinout

EL4501
(24 LD QSOP)
TOP VIEW

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S to GND) . . . . . +6V
Pin Voltage. . . . . GND -0.3V, V_S +0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . 125°C
Power Dissipation . . . . . See Curves
Maximum Continuous Current (VIDEO OUT) 50mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_S = V_{SD}$ = 5V, GND = 0V, T_A = 25°C, Input Video = $1V_{P-P}$, R_{FREQ} = 130kΩ

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{SA}	Input Supply Current	No load	7.5	10.5	13.5	mA
I_{SD}	Digital Supply Current	No load, V_{IN} = 0V	1.9	2.3	4	mA
V_S	Input Supply Voltage Range		4.5		5.5	V
V_{SD}	Digital Input Supply Voltage Range		4.5		5.5	V
VIDEO AMPLIFIER SECTION						
V_{OP}	Positive Output Voltage Swing (VIDEO OUT) (Note 1)	R_L = 150Ω to V_S/2	4.65	4.70		V
		R_L = 150Ω to GND	4.20	4.60		V
		R_L = 1kΩ to V_S/2	4.85	4.90		V
V_{ON}	Negative Output Voltage Swing (VIDEO OUT) (Note 1)	R_L = 150Ω to V_S/2		0.15	0.30	V
		R_L = 150Ω to GND		0.06	0.25	V
		R_L = 1kΩ to V_S/2		0.05	0.20	V
$+I_{OUT}$	Positive Output Current (VIDEO OUT)	R_L = 10Ω to V_S/2	60	70		mA
$-I_{OUT}$	Negative Output Current (VIDEO OUT)	R_L = 10Ω to V_S/2	-50	-60		mA
dG	Differential Gain Error (VIDEO OUT) (Note 2)	A_V = 1, R_L = 10kΩ, R_F = 0Ω		0.05		%
dP	Differential Phase Error (VIDEO OUT) (Note 2)	A_V = 1, R_L = 10kΩ, R_F = 0Ω		0.03		°
BW	Bandwidth	-3dB, G = 1, R_L = 10kΩ to GND, R_F = 0		100		MHz
		-3dB, G = 1, R_L = 150Ω to GND, R_F = 0		60		MHz
BW1	Bandwidth	±0.1dB, G = 2, R_L = 150Ω to GND		8		MHz
SR	Slew Rate	25% to 75%, $3.5V_{P-P}$, R_L = 150Ω, R_F = 0	80	96		V/µs
V_{RL}	Ref Level Range			0/3.5		V
t_S	Settling Time	to 0.1%, V_{IN} = 0V to 3V		35		ns
R_{IN}	Input Resistance (VIDEO IN)			115		kΩ
C_{IN}	Input Capacitance (VIDEO IN)			1.5		pF
A_{VOL}	Open Loop Voltage Gain	R_L = no load, V_{OUT} = 0.5V to 3V		65		dB
		R_L = 150Ω to GND, V_{OUT} = 0.5V to 3V		50		dB
DC-RESTORE SECTION						
CMIR	Common Mode Input Range (REF IN)			0/3.5		V
V_{OS}	Input Offset Voltage	DC restored		±20		mV
TCV_{OS}	Input Offset Voltage Temperature Coefficient			10		µV/°C
I_B	Input Bias Current (REF IN)	V_{CM} = 0V to 3.5V	-10	0.001	10	µA

Electrical Specifications $V_S = V_{SD} = 5V$, GND = 0V, $T_A = 25°C$, Input Video = $1V_{P-P}$, $R_{FREQ} = 130k\Omega$ **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference Output Voltage (REF OUT)	I_{OUT} = +2mA to -0.5mA	1.15	1.3	1.4	V
I_{RMAX}	Available Restore Current (VFB)			18.5		µA
DATA SLICER SECTION						
I_{IH}	Input High Current (DS MODE & DS ENABLE)	V_{IH} = 5V		6	10	µA
I_{IL}	Input Low Current (DS MODE & DS ENABLE)	V_{IL} = 0V		200	350	nA
V_{IH}	Input High Voltage (DS MODE & DS ENABLE)		4.5			V
V_{IL}	Input Low Voltage (DS MODE & DS ENABLE)				0.5	V
V_{OH}	Output High Voltage (DS OUT)	I_{OUT} = -1mA	4.75	4.9		V
V_{OL}	Output Low Voltage (DS OUT)	I_{OUT} = +1mA		0.1	0.25	V
I_{OUT}	Short Circuit Current (DS OUT)	$R_L = 10\Omega$ to 2.5V	8	11		mA
I_B	Input Bias Current (DS REF)	DS REF = 0V to 5V	-10	0.001	10	µA
V_{OS}	Input Offset Voltage		-20		+20	mV
V_{HYS}	Hysteresis			±5		mV
t_{PD}	Propagation Delay	50% to 50%		18		ns
$t_{R/F}$	Rise/Fall Time	10% to 90%, $R_L = 150k\Omega$, C_L = 5pF		1.2		ns
SYNC SEPARATOR SECTION						
$Z_{SOURCE\ (MAX)}$	Maximimum source impedance driving SYNC IN			1000		Ω
I_{IH}	Input High Current (FSEL & SYNC MODE)	V_{IH} = 5V	-1		1	µA
I_{IL}	Input Low Current (FSEL & SYNC MODE)	V_{IL} = 0V	-1		1	µA
V_{IH}	Input High Voltage (FSEL & SYNC MODE)		4.5			V
V_{IL}	Input Low Voltage (FSEL & SYNC MODE)				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -1.6mA	4.6			V
V_{OL}	Output Low Voltage	I_{OL} = +1.6mA			0.4	V
V_{THRSHA}	Adaptive Slice Level	SYNC MODE = 0V	40	50	60	%
V_{THRSHF}	Fixed Slice Threshold	SLICE MODE = V_S	80	100	120	mV
V_{SI}	SYNC IN Reference Voltage			1.8		V
R_{INSI}	SYNC IN Input Impedance			115		kΩ
V_{RANGE}	Input Dynamic Range		0.5		2.0	V_{P-P}
t_{CD}	COMPOSITE Delay	FSEL = 0, from 50% of sync leading edge	25	35	45	ns
t_{CDF}	COMPOSITE Delay	FSEL = 1, from 50% of sync leading edge	150	225	280	ns
t_{BD}	BACK PORCH Delay	FSEL = 0, from 50% of trailing sync edge	125	170	225	ns
t_{BDF}	BACK PORCH Delay	FSEL = 1, from 50% of trailing sync edge	250	420	550	ns
t_{HD}	HORIZONTAL Delay	FSEL = 0/1, from 50% of sync leading edge	365	470	585	ns
t_{BW}	BACK PORCH Width	FSEL = 0/1	2.8	3.2	4.1	µs
t_{HW}	HORIZONTAL Width	FSEL = 0	1.1	1.3	1.5	µs
t_{HWF}	HORIZONTAL Width	FSEL = 1	1.2	1.5	1.8	µs
t_{VW}	VERTICAL Width	FSEL = 0/1, standard NTSC	196	198	200	µs
t_{VDD}	VERTICAL Default Delay	FSEL = 0	26.5	31.2	35.9	µs
t_{VDDF}	VERTICAL Default Delay	FSEL = 1		31.5		µs

Electrical Specifications $V_S = V_{SD} = 5V$, GND = 0V, $T_A = 25°C$, Input Video = $1V_{P-P}$, $R_{FREQ} = 130k\Omega$ **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
f_H	Horiz Scan Rate		15		130	kHz
V_{LOSE}	Analog LOS Enable Threshold	Minimum sync amplitude to enable outputs		120		mV
V_{LOSD}	Analog LOS Disable Threshold	Maximum sync amplitude to disable outputs		80		mV
t_{JIT}	Output Jitter	All sync separator outputs		5		ns
A_{SA}	SYNC AMP Gain		1.7	2.0	2.3	
R_{SA}	SYNC AMP Output Impedance			200		Ω
V_{RFREQ}	R_{FREQ} Reference Voltage	R_{FREQ} = 13kΩ to 130kΩ	1.15	1.28	1.4	V

NOTES:

1. R_L is Total Load Resistance due to Feedback Resistor and Load Resistor.
2. AC signal amplitude = $286mV_{PP}$, F = 3.58MHz, REF IN is swept from 0.8V to 3.4V, R_L is DC coupled.

Typical Performance Curves

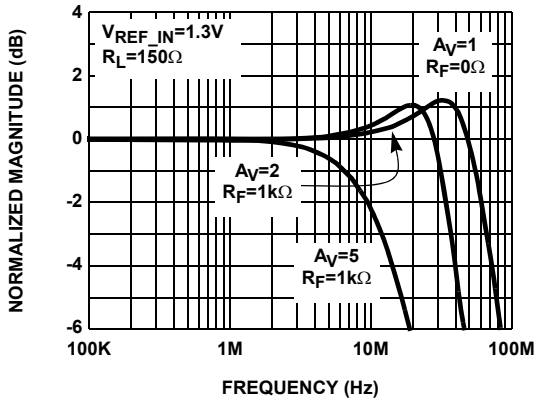


FIGURE 1. NON-INVERTING FREQUENCY RESPONSE (GAIN)

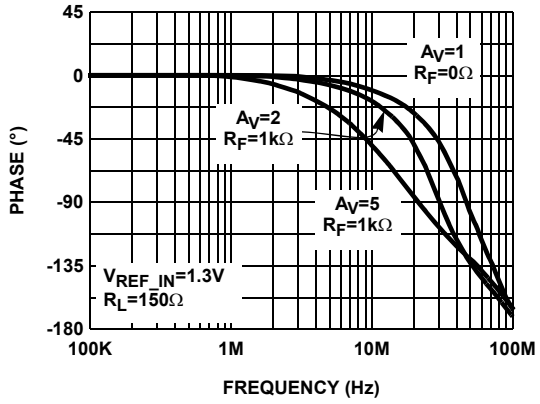


FIGURE 2. NON-INVERTING FREQUENCY RESPONSE (PHASE)

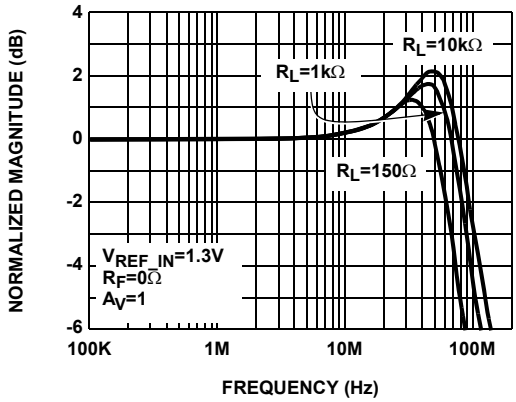


FIGURE 3. FREQUENCY RESPONSE FOR VARIOUS R_L

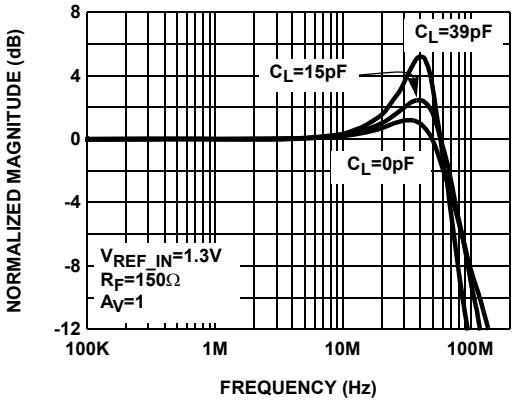


FIGURE 4. FREQUENCY RESPONSE FOR VARIOUS C_L

Typical Performance Curves (Continued)

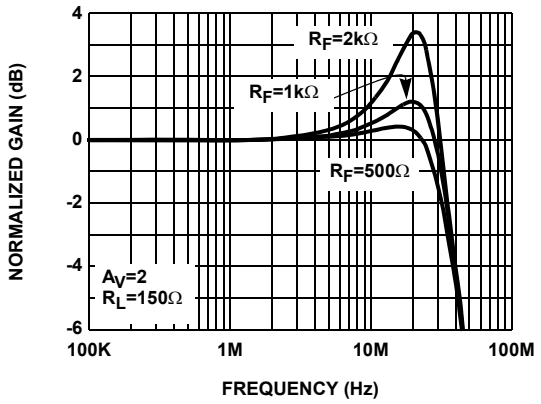


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS R_F

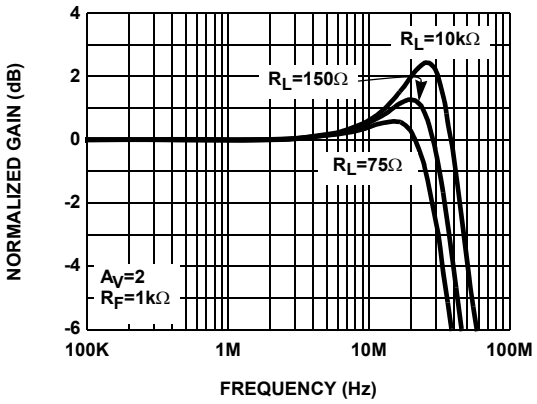


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS R_L

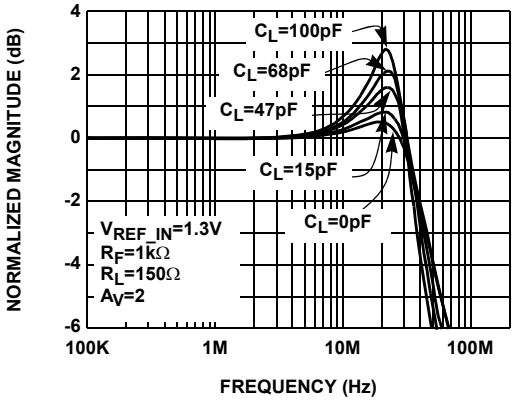


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS C_L

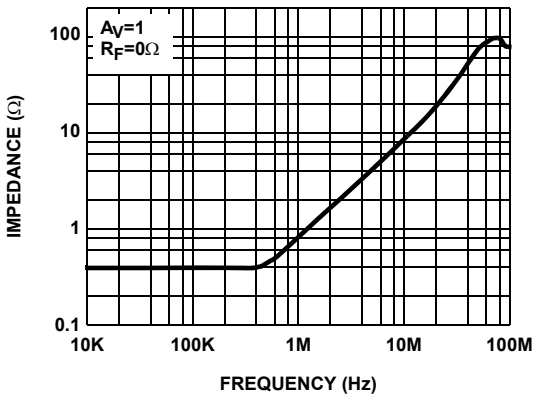


FIGURE 8. CLOSED LOOP OUTPUT IMPEDANCE

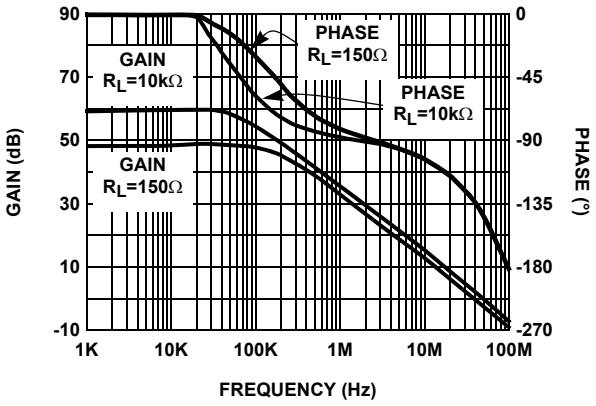


FIGURE 9. OPEN LOOP GAIN AND PHASE vs FREQUENCY

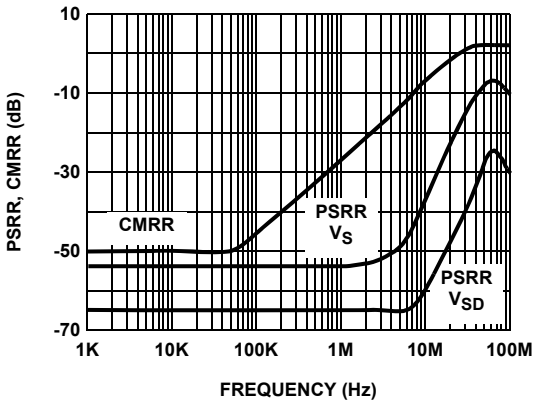


FIGURE 10. PSRR AND CMRR vs FREQUENCY - VIDEO AMP

Typical Performance Curves (Continued)

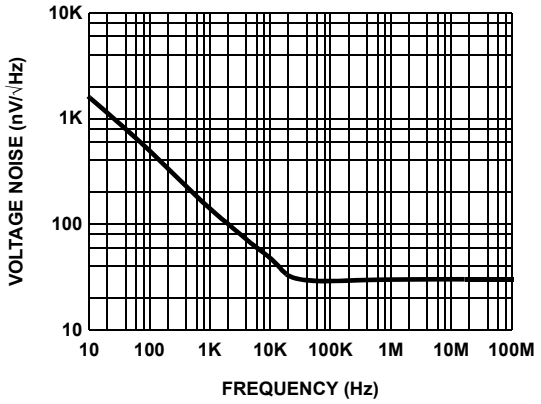


FIGURE 11. VOLTAGE NOISE vs FREQUENCY - VIDEO AMP

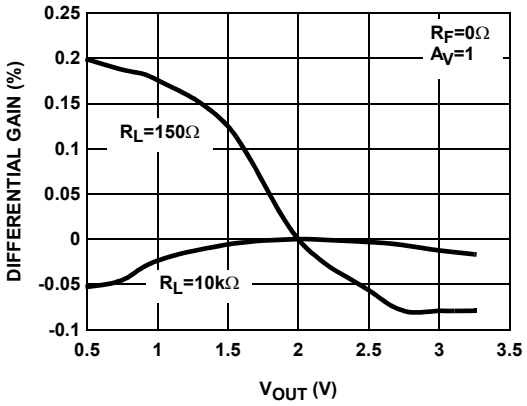


FIGURE 12. DIFFERENTIAL GAIN FOR R_L TIED TO 0V

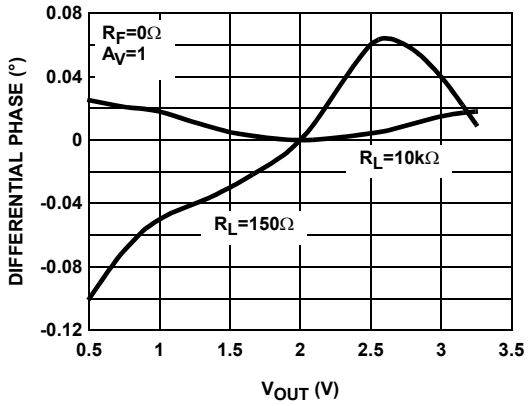


FIGURE 13. DIFFERENTIAL PHASE FOR R_L TIED TO 0V

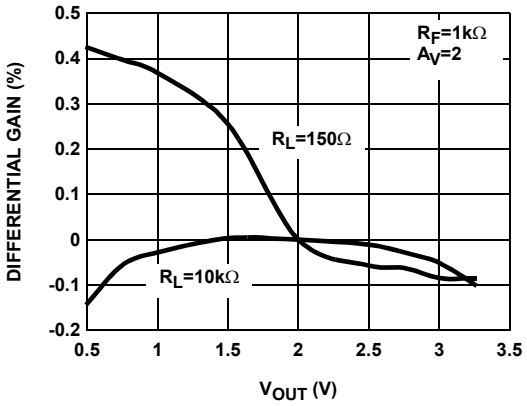


FIGURE 14. DIFFERENTIAL GAIN FOR R_L TIED TO 0V

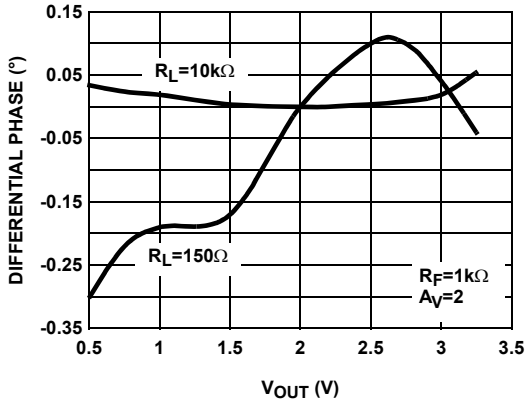


FIGURE 15. DIFFERENTIAL PHASE FOR R_L TIED TO 0V

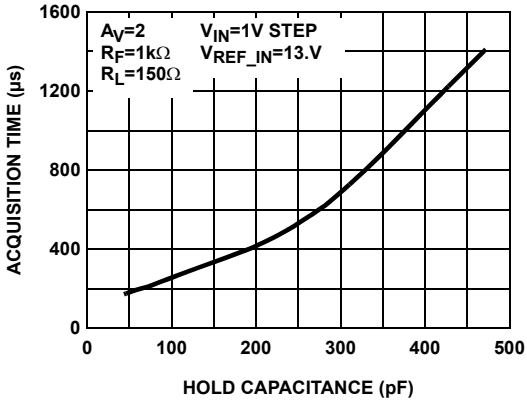


FIGURE 16. ACQUISITION TIME vs HOLD CAPACITANCE

Typical Performance Curves (Continued)

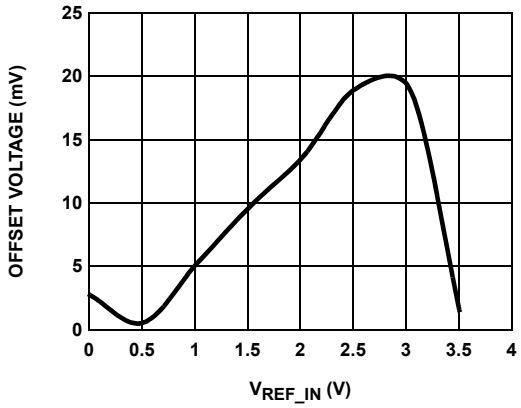


FIGURE 17. DC OFFSET VOLTAGE AT V_{OUT} vs V_{REF_IN}

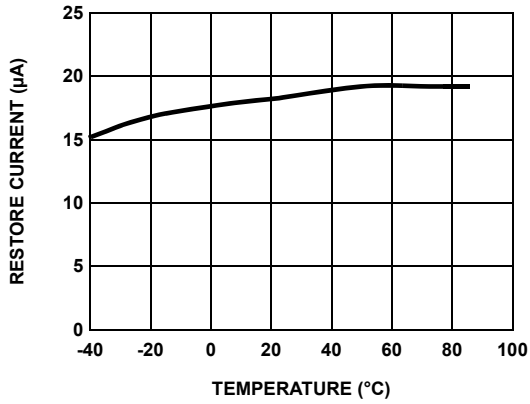


FIGURE 18. DC-RESTORE CURRENT vs TEMPERATURE

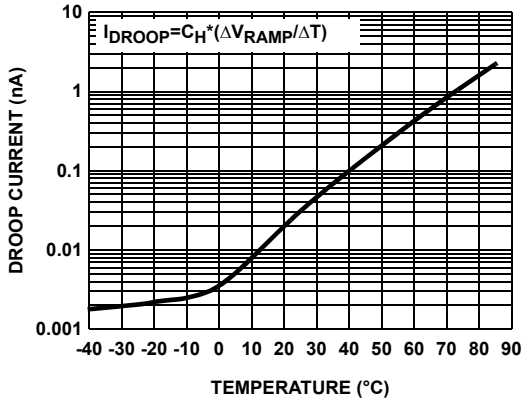


FIGURE 19. DROOP CURRENT vs TEMPERATURE

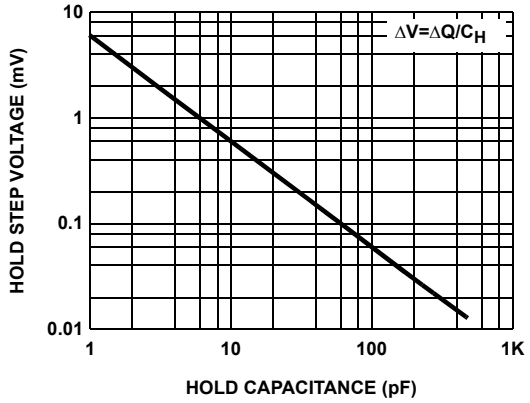


FIGURE 20. HOLD STEP VOLTAGE vs HOLD CAPACITANCE

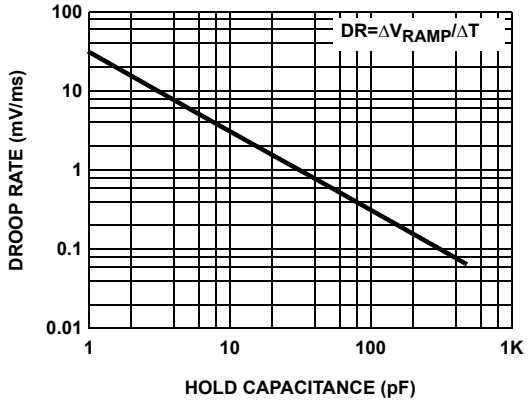


FIGURE 21. DROOP RATE vs HOLD CAPACITANCE

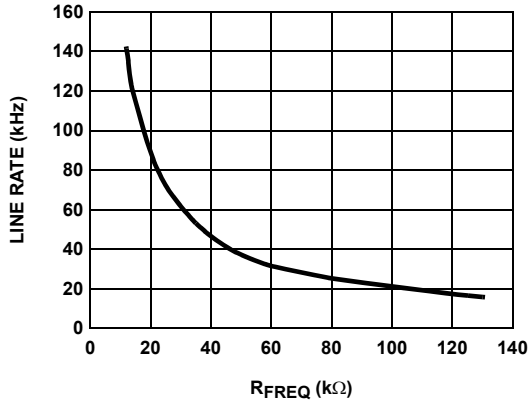


FIGURE 22. LINE RATE vs R_{FREQ}

Typical Performance Curves (Continued)

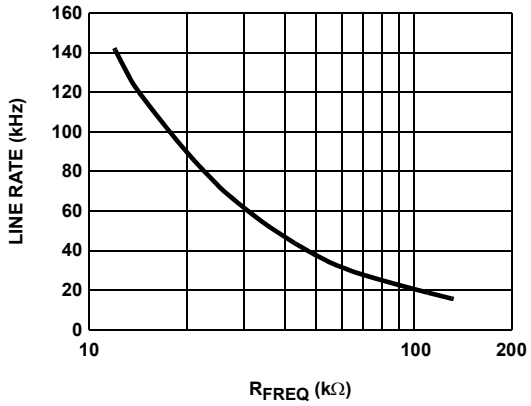


FIGURE 23. LINE RATE vs R_{FREQ}

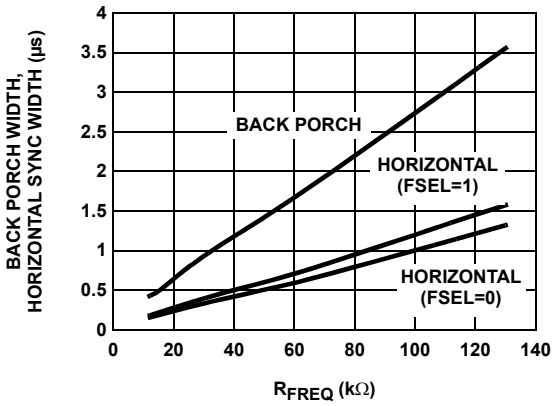


FIGURE 24. BACK PORCH AND HORIZONTAL SYNC WIDTH vs R_{FREQ}

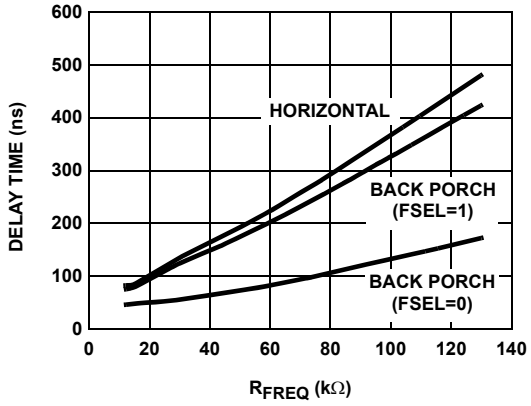


FIGURE 25. DELAY TIME vs R_{FREQ}

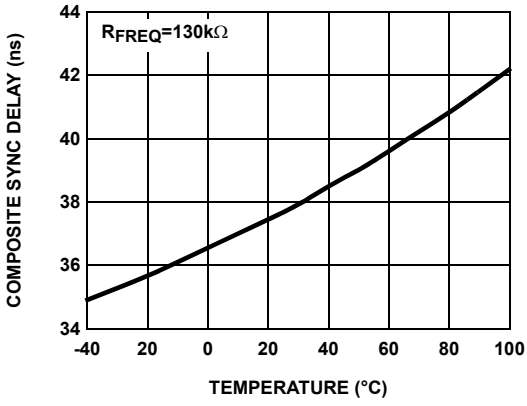


FIGURE 26. COMPOSITE DELAY vs TEMPERATURE - FSEL = 0

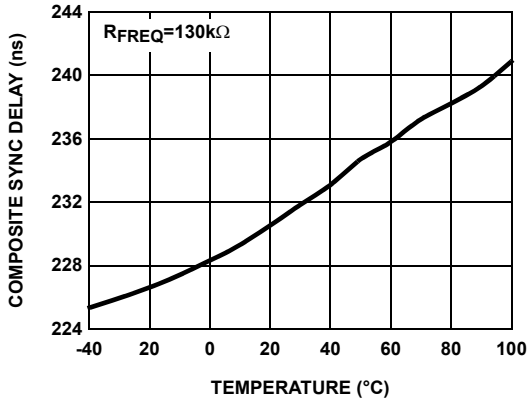


FIGURE 27. COMPOSITE DELAY vs TEMPERATURE - FSEL = 1

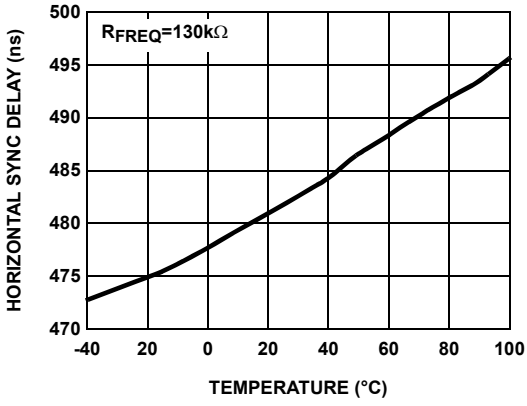


FIGURE 28. HORIZONTAL DELAY vs TEMPERATURE

Typical Performance Curves (Continued)

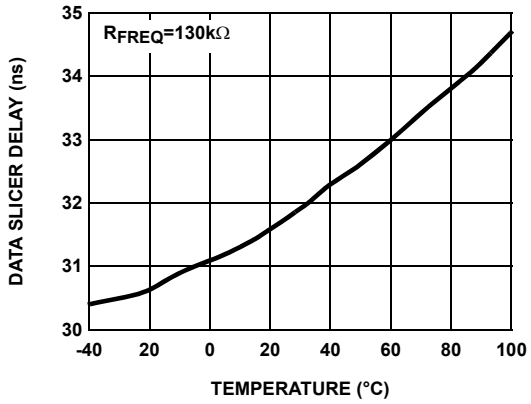


FIGURE 29. DATA SLICER DELAY vs TEMPERATURE - DS MODE = 1

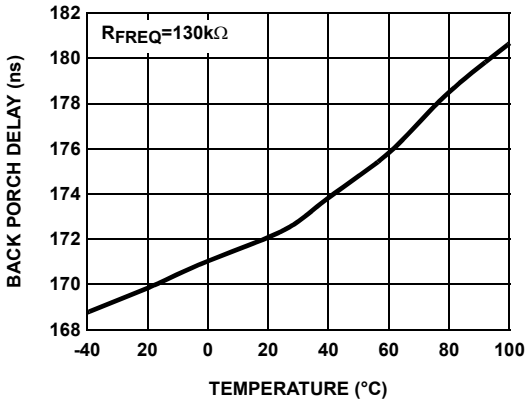


FIGURE 30. BACK PORCH DELAY vs TEMPERATURE - FSEL = 0

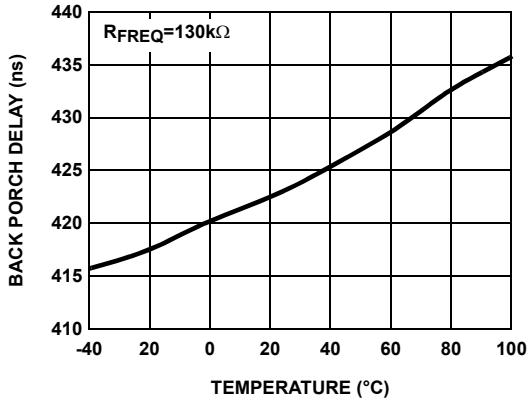


FIGURE 31. BACK PORCH DELAY vs TEMPERATURE - FSEL = 1

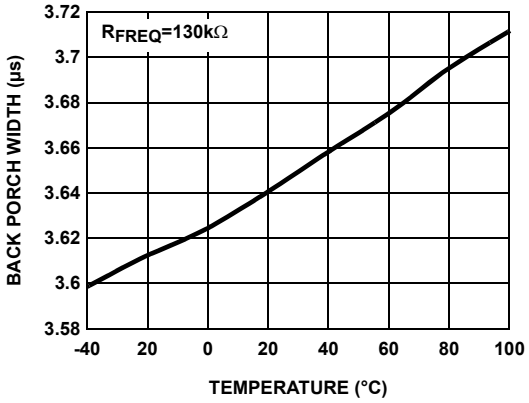


FIGURE 32. BACK PORCH WIDTH vs TEMPERATURE

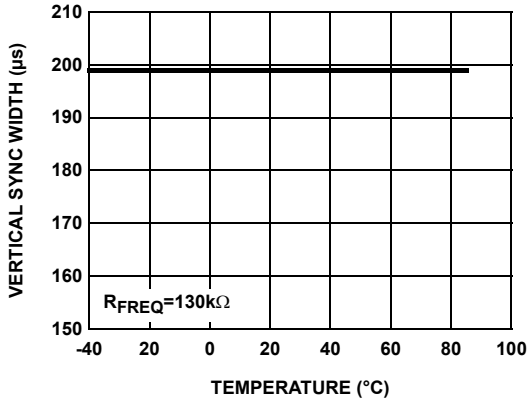


FIGURE 33. VERTICAL SYNC WIDTH vs TEMPERATURE

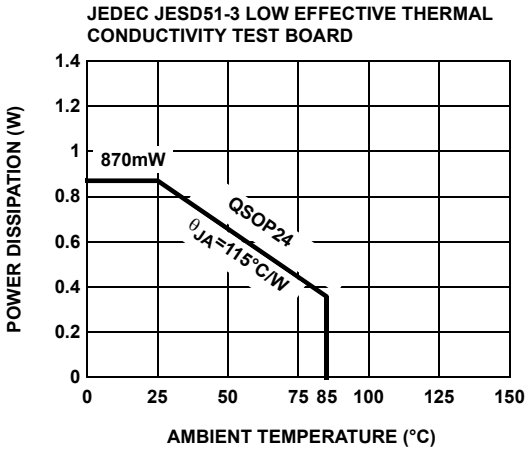


FIGURE 34. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

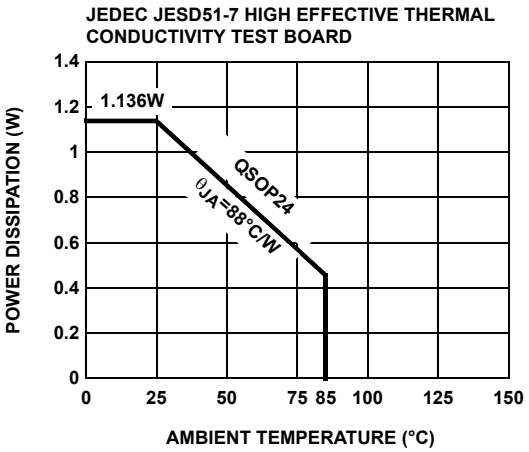
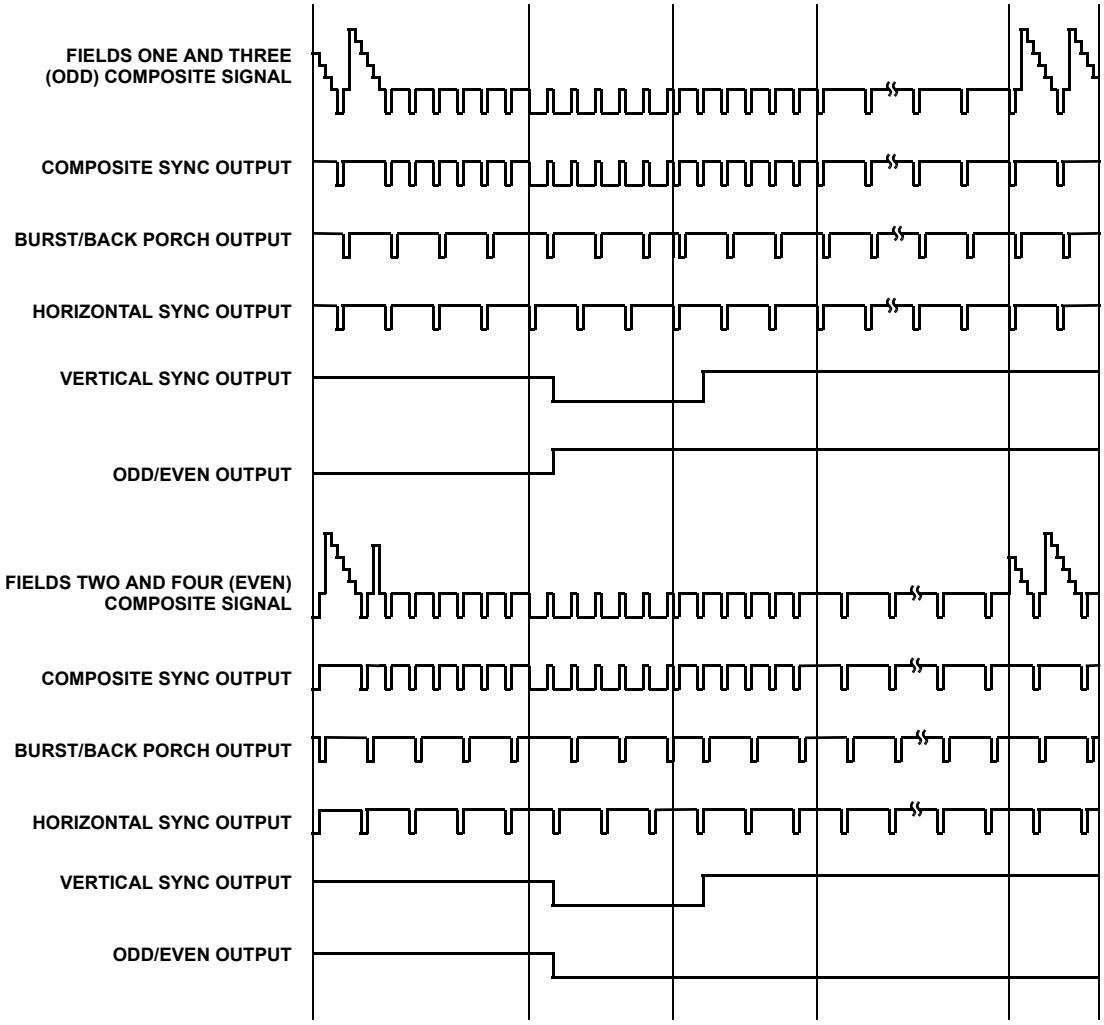
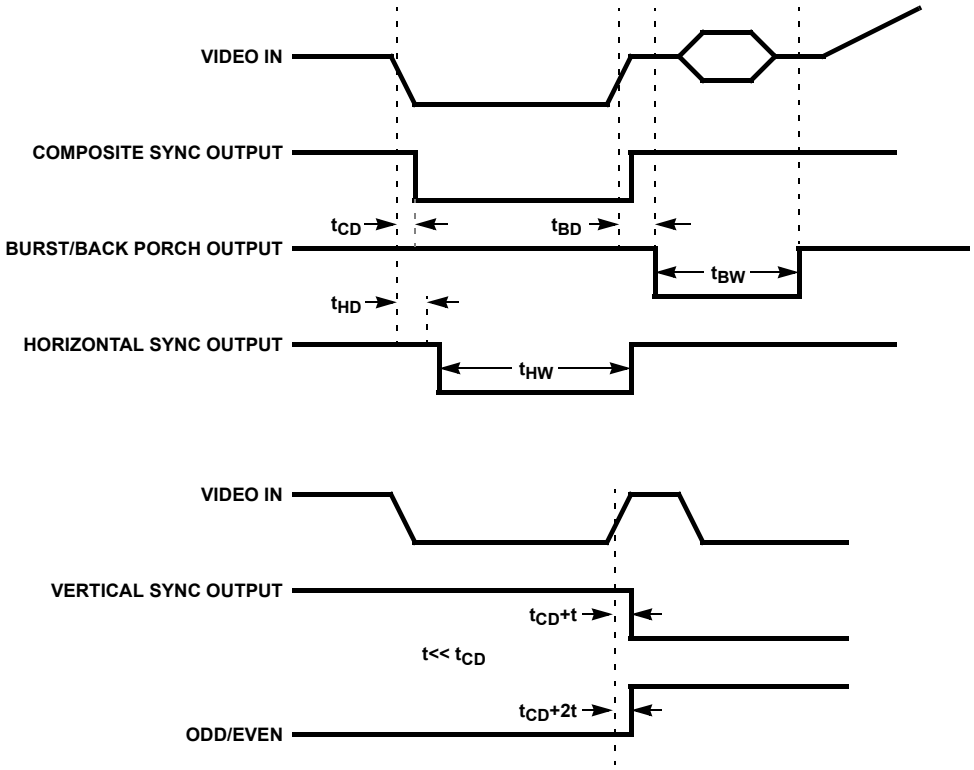


FIGURE 35. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

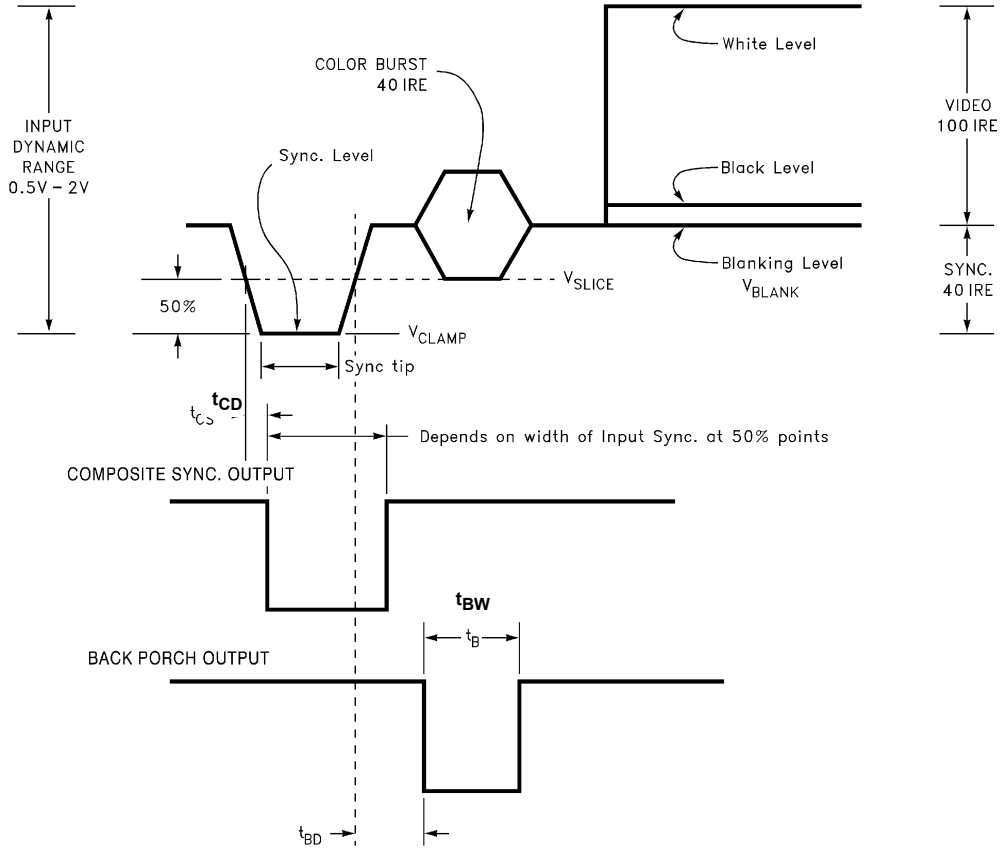
Timing Diagrams



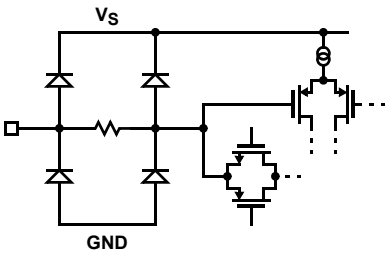
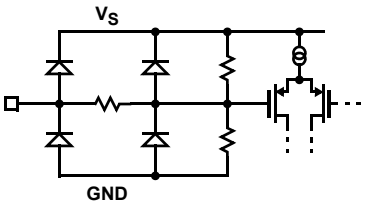
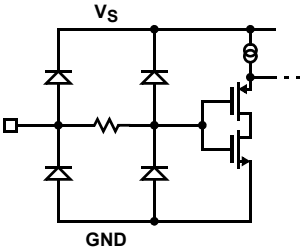
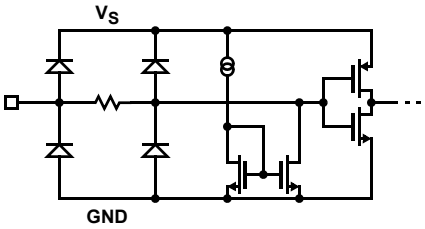
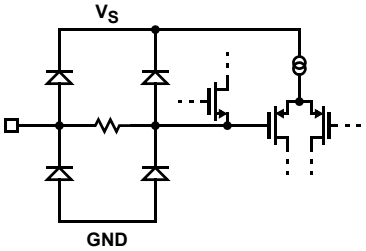
Timing Diagrams



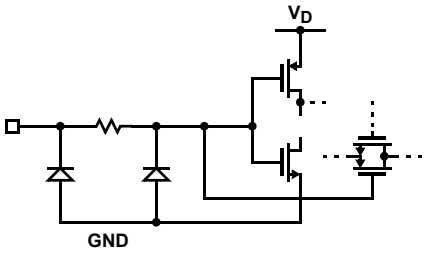
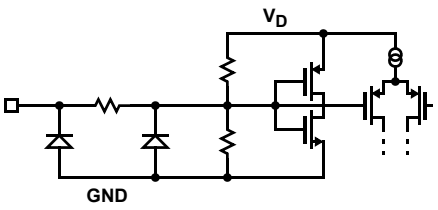
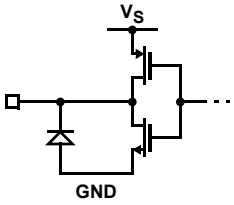
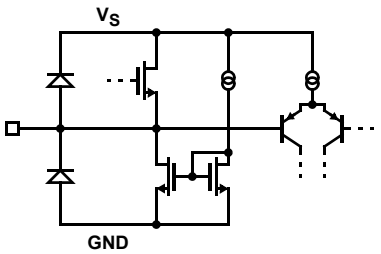
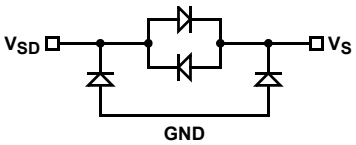
Standard (NTSC Input) H. Sync Detail



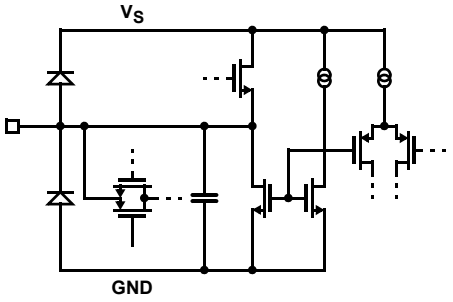
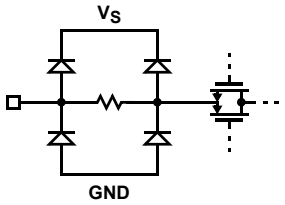
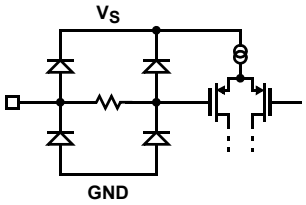
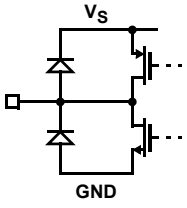
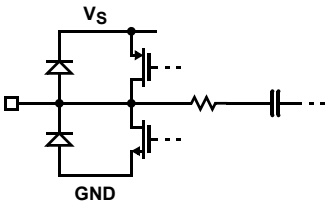
Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION	EQUIVALENT CIRCUIT
1	VFB	Input	Connection for gain and feedback resistors, R_F and R_G	 CIRCUIT 1
2	VIDEO IN	Input	Input to DC-restore amplifier; input coupling capacitor connects from here to video source	 CIRCUIT 2
3	DS MODE	Input	Sets the mode of the DS comparator; logic low selects a standard logic output; logic high selects an open drain/collector	 CIRCUIT 3
4	DS ENABLE	Input	Enables the output of the comparator; a logic high enables the comparator; a logic low three-states it	 CIRCUIT 4
5	GND	Input	Analog ground	
6	GNDD	Input	Digital ground	
7	RFREQ	Input	Connection for bias resistor that sets the overall timing	 CIRCUIT 5

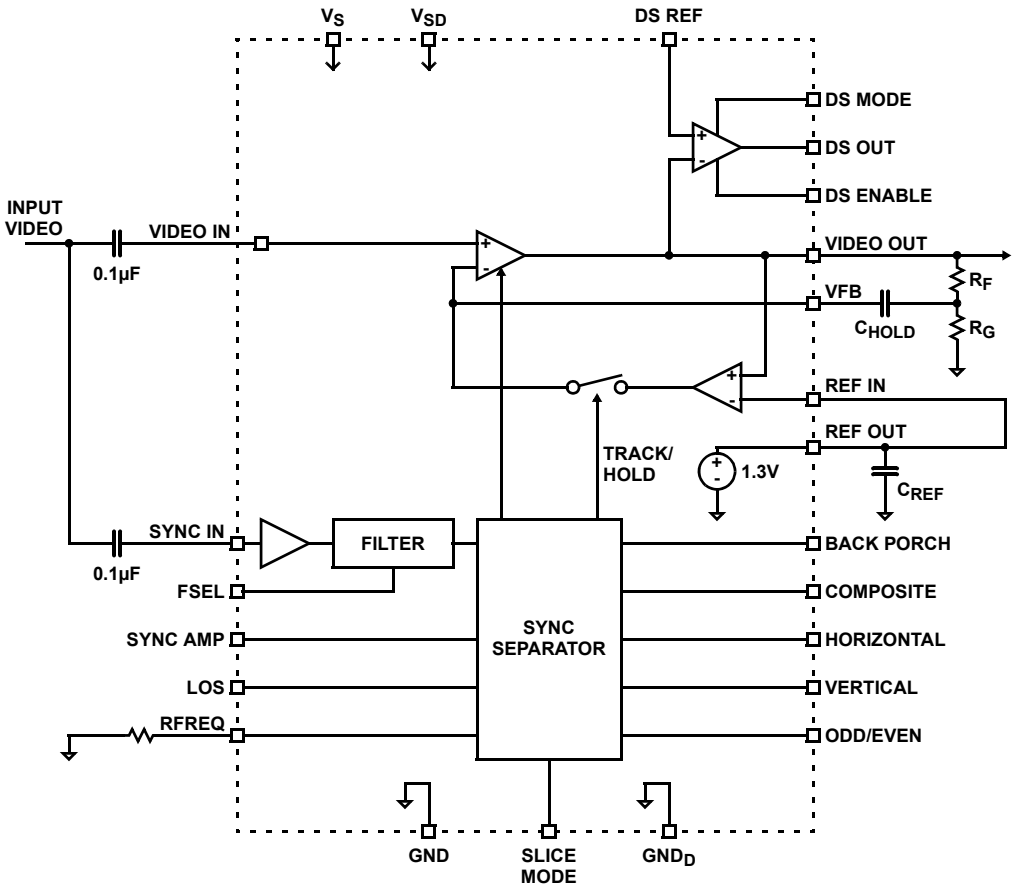
Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION	EQUIVALENT CIRCUIT
8	FSEL	Input	Enable/bypass internal brick wall filter; a logic high is used to enable the filter; a logic low to disable it	 CIRCUIT 6
9	SYNC IN	Input	Input to the sync separator; connects to the video source via a coupling capacitor or to a color burst input filter	 CIRCUIT 7
10	LOS	Output	Loss of signal output; goes high if no input video signal is detected	 CIRCUIT 8
11	COMPOSITE	Output	Composite sync output	Reference circuit 8
12	HORIZONTAL	Output	Horizontal sync output	Reference circuit 8
13	VERTICAL	Output	Vertical sync output	Reference circuit 8
14	ODD/EVEN	Output	Odd/even field indicator output	Reference circuit 8
15	BACK PORCH	Output	Back porch output	Reference circuit 8
16	SLICE MODE	Input	Low = 50% slicing level; high = 70mV fixed slicing level	Reference circuit 8
17	SYNC AMP	Output	Amplitude of sync tip; can be used to control AGC circuit	 CIRCUIT 9
18	VSD	Input	Digital power supply; nominally +5V	 CIRCUIT 10
19	VS	Input	Analog power supply; nominally +5V	Reference circuit 10

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION	EQUIVALENT CIRCUIT
20	REF OUT	Output	Voltage reference for use as blanking level in low cost system	 CIRCUIT 11
21	REF IN	Input	DC voltage on this pin sets the DC-restore voltage and output blanking level	 CIRCUIT 12
22	DS REF	Input	Sets the slicing level or reference level for the comparator	 CIRCUIT 13
23	DS OUT	Output	Output of the data slicing comparator; the output is either open drain or standard symmetrical logic depending on the DS MODE pin	 CIRCUIT 14
24	VIDEO OUT	Output	Output of DC-restore amplifier	 CIRCUIT 15

Block Diagram



Applications Information

Product Description

The EL4501 is a video front-end sub-system comprised of a video amplifier with DC-restore, an adjustable threshold data slicer, and an advanced sync separator. The prime function of the system is to DC-stabilize and buffer AC-coupled analog video signals and to extract timing reference signals embedded in the video signal. An adjustable threshold data slicer incorporated into the EL4501 may be used to extract data embedded within the active video or VBI regions of a video signal.

Theory of Operation

DC-RESTORE LOOP

When video signals are distributed, it is common to employ capacitive coupling to prevent DC current flow due to differences in local grounds or signal reference levels. However, the coupling capacitor causes the DC level of the signal post capacitor to be dependent on the video (luminance) content of the waveform. A DC-restore loop is used to correct this behavior by moving a portion of the video waveform to a DC reference level in response to a control signal. When the loop is operating, DC drift accumulates over a single line only, before it is corrected. The peak value of drift is limited by the rate of the control signal (typically video line rate) and the AC coupling time constant.

The restore loop is comprised of a 100MHz forward video amplifier, combined with a nulling amplifier and sample and hold circuit. For maximum flexibility the hold capacitor is placed off-chip, allowing the loop response rate to be tailored for specific applications and minimizing hold-step problems. The loop provides a restore current peak of ±20µA at room temperature. Figure 36 shows the amplifier and S/H connection. During normal operation the internally generated DC-restore control signal is timed to the back porch of the video waveform. Figure 37 shows an NTSC video signal, along with the EL4501 BACK PORCH output. In operation, BACK PORCH activates the S/H switch, completing the nulling feedback loop and driving the video amplifier output towards the reference voltage. At the end of BACK PORCH, the external capacitor holds the correction voltage for the remainder of the video line. In the absence of a valid input signal, the chip generates a repetitive, arbitrary restore control signal at the line rate set by the external resistor R_{FREQ}. Although uncorrelated to the input, the pulse prevents the amplifier output drifting significantly from the DC-restore

reference level. This improves start-up behavior and speeds recovery after a signal drop-out. For ease of use, the EL4501 provides a buffered 1.3V DC level normally connected directly to the restore loop reference input (REF IN). Alternatively, an external voltage between 0V and 3.5V, connected to REF IN, can be used to set the restored level.

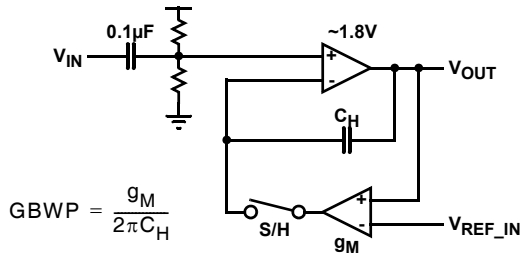


FIGURE 36. DC-RESTORE AMPLIFIER AND S/H CONFIGURATION

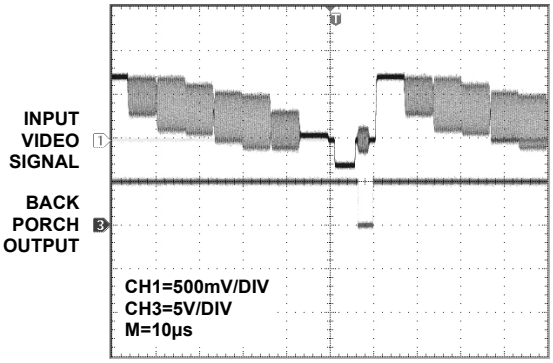


FIGURE 37. NTSC VIDEO SIGNAL WITH BACK PORCH OUTPUT

Auto-Zero Loop Bandwidth

The gain bandwidth product (GBWP) of the auto-zero loop is determined by the size of the hold capacitor and the transconductance (g_M1) of the sample and hold amplifier. GBWP = $g_M1/(2\pi * C_H)$, gM1 is about 1/(29kΩ), for C_H = 270pF, GBWP is 20kHz. For C_H = 100pF, GBWP is about 55kHz.

Charge Injection and Hold Step Error

Charge injection refers to the charge transferred to the hold capacitor when switching to the hold mode. The charge should ideally be 0, but due to stray capacitive coupling and other effects, it is typically 6fC. This charge changes the hold capacitor voltage by $\Delta V = \Delta Q/C_H$ and will shift the output voltage of the video amplifier by ΔV. However, this shift is small and can be negligible for the EL4501 (see the Hold Step Voltage Error vs Hold Capacitance curve). Assuming C_H = 100pF, ΔV is about 60µV. There will be 60µV change at the video amplifier output.

Droop Rate

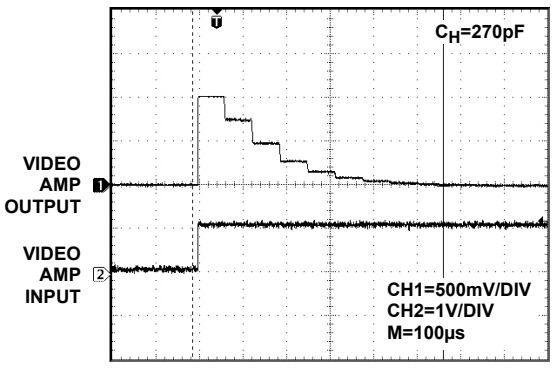
When the S/H amplifier is in the hold mode, there is a small current that leaks from the switch to the hold capacitor. This quantity is called the droop current. This droop current produces a ramp in the hold capacitor voltage, which in turn produces a similar voltage at the video amplifier output. The droop rate at the video amplifier output can be found using the following equation:

$$DroopRate = \frac{\Delta V_{RAMP}}{\Delta t}$$

Assuming C_H = 100pF, from the Droop Rate vs Hold Capacitance curve, the droop rate is about 0.31mV/ms at the video amplifier output at room temperature. In NTSC applications, there is about 60µs between auto-zero periods. Thus, there is (0.31mV/ms) * 60µs = 18.6µV. It is much less than 0.5IRE (3.5mV). This drift is negligible.

Choice of Hold Capacitor

The EL4501 allows the user to choose the hold capacitor as low as 1pF and it is still stable. A smaller hold capacitor has a faster acquisition time and faster auto-zero loop response, but would increase the droop and hold step error. Also, if the acquisition time is too fast, it would probably give an image with clamp streaking and low frequency noise with noisy signals. Increasing the hold capacitor would increase the acquisition time, lower the auto-zero loop response, lower the droop and hold step error. See the performance curves for the trade-off. Normally, in video (NTSC and PAL) applications, a smooth acquisition might takes about 10 to 20 scan lines. For a hold capacitor equal to 270pF, the acquisition time is about 10 lines. In the worse case, ambient temperature is 85°C, the droop current is 2.2nA which causes the output voltage ramp to about 0.49mV for 60µs. This drift is negligible in most applications. Figure 38 shows the input and output waveforms of the video amplifier while the S/H is in sample mode. Applying a 1V step to the video amplifier input, the output of the video amplifier jumps to 2.3V. Then, the auto-zero system tries to drive the video output to the reference voltage, which is 1.3V. The acquisition time takes about 10 NTSC scan lines.



Auto-zero mechanism restores amplifier output to 1.3V after +1V step at input

FIGURE 38. INPUT AND OUTPUT WAVEFORMS WITH S/H IN SAMPLE MODE

DATA SLICER

The data slicer is a fast comparator with the output of the video amplifier connected to its inverting input and the DS REF connected to its non-inverting input. The DS OUT is logical inverse of the video output sliced at the DS REF voltage. The propagation delay from the video amplifier output to the DS OUT is about 18ns. There is about 10mV hysteresis added internally in the comparator to prevent the oscillation at the DS OUT when the voltages at the two inputs are very close or equal. An adjustable DS REF voltage may be used to extract data embedded within the active video or video blanking interval regions of a video signal. Logic low at the DS ENABLE pin enables the comparator and logic low lets the DS OUT be three-state. The DS MODE pin sets the mode of the DS comparator. Logic low at the DS MODE pin selects a standard logic output and a logic high selects an open drain/collector output.

VIDEO AMPLIFIER

The EL4501 DC-restore block incorporates a wide bandwidth, single supply, low power, rail-to-rail output, voltage feedback operational amplifier. The amplifier is internally compensated for closed loop feedback gains of +1 or greater. Larger gains are acceptable but bandwidth will be reduced according to the familiar Gain-Bandwidth product.

Connected in a voltage follower mode and driving a high impedance load, the amplifier has a -3dB bandwidth of 100MHz. Driving a 150Ω load, the -3dB bandwidth reduces to 60MHz while maintaining a 200V/µs slew rate.

CHOICE OF FEEDBACK RESISTOR, R_F

The video amplifier is optimized for applications that require a gain of +1. Hence, no feedback resistor is required. However, for gains greater than +1, the feedback resistor forms a pole with the hold capacitance. As this pole becomes larger, phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce ringing and peaking at the expense of reducing the bandwidth. As far as the output stage of the amplifier is concerned, $R_F + R_G$ appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently R_F also has a minimum value that should not be exceeded for optimum performance.

- For A_V = +1, R_F = 0Ω is optimum
- For A_V = +2, R_F between 300Ω and 1kΩ is optimum

VIDEO PERFORMANCE

For good video signal integrity, an amplifier is required to maintain the same output impedance and frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150Ω because of the change in output current with DC level. A look at the Differential Gain and Differential Phase curves will help to obtain optimal performance. Curves are provided for A_V = +1 and +2, and R_L = 150Ω and 10kΩ. As with all video amplifiers, there is a common mode sweet spot for optimum differential gain/differential phase. For example, with A_V = +1 and R_L = 150Ω and the video level kept between 1V and 3V, the amplifier will provide dG/dP performance of 0.17%/0.07°. This condition is representative of using the amplifier as a buffer driving a DC coupled, double terminated, 75Ω coaxial cable. Driving high impedance loads, such as signals on computer video cards gives much better dG/dP performance. For A_V = 1, R_L = 10kΩ, and the video level kept between 1V and 3V, the dG/dP are 0.03%/0.02°.

SHORT-CIRCUIT CURRENT LIMIT

The EL4501 video amplifier has no internal short circuit protection circuitry. Short circuit current of 90mA sourcing and 65mA sinking typically will flow if the output is shorted midway between the rails. If the output is shorted indefinitely, the power dissipated could easily increase the die temperature such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±50mA. This limit is set by internal metal interconnect limitations. Obviously, short circuit conditions must not be allowed to persist or internal metal connections will be damaged or destroyed.

DRIVING CABLES AND CAPACITIVE LOADS

The EL4501 video amplifier can drive 39pF loads in parallel with 150Ω with 5dB of peaking. For less peaking in theses applications a small series resistor of between 5Ω and 50Ω can be placed in series with the output. However, this will obviously reduce the gain slightly. If your gain is greater than 1, the gain resistor R_G can be adjusted to make up for any lost gain caused by the additional output resistor. Peaking may also be reducing by adding a “snubber” circuit at the output. A snubber is a resistor in series with a capacitor, 150Ω and 100pF being typical values. The advantage of a snubber is that it does not draw DC load current.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor decouples the video amplifier from the cable and enables extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can reduce peaking.

VIDEO SYNC SEPARATOR

The EL4501 includes an advanced sync separator, which is used to generate the DC-restore control signal and seven major sync outputs. The advanced sync separator operates at

a 5V DC (pin VSD) single-supply voltage. The input signal source is composite video with levels of $0.5V_{P-P}$ to $2.0V_{P-P}$. Low jitter, temperature-stable timing signals are generated using a master time-base, embedded within the system. Line rate is adjustable from 10kHz to 135kHz using a single external resistor (R_{FREQ}). An integrated, pin-selectable digital filter tracks line rate and rejects high frequency noise and video artifacts, such as color burst. In addition to the digital filter, a window-based, time qualification scheme is employed to improve recovered signal quality. During loss of signal, all outputs are blanked to prevent output chatter caused by input noise.

The maximum total source impedance driving the SYNC IN pin should be 1kΩ or lower. Source impedances greater than 1kΩ may reduce the ability of the EL4501 to reliably recover the sync signal.

Composite Sync Output

The composite sync output is a reproduction of the signal waveform below the composite video black level, with the video completely removed. The composite video signal is AC-coupled to SYNC IN (pin 9). The video signal passes through a comparator whose threshold is controlled by the SLICE MODE pin. The output of the comparator is buffered to the COMPOSITE output (pin 11) as a CMOS logic signal.

Horizontal Sync Output

The horizontal circuit triggers on the falling edge of the sync tip of the input composite video signal and produces a horizontal output with pulse widths about 12 times the internal oscillator clock. For NTSC video input, the pulse width of the horizontal sync is 1.5µs, with the digital filter selected. The half line pulses present in the input signal during vertical blanking are removed with an internal 2H-eliminator circuit.

Vertical Sync Output

A low-going vertical sync pulse is generated during the start of the vertical cycle of the incoming composite video signal. The vertical output pulse is started on the first serration pulse in the vertical interval and is ended on the second rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 31µs after the last falling edge of the vertical pre-equalizing pulse for R_{FREQ} = 130kΩ.

Back Porch Output

In a composite video signal, the chroma burst is located on the back porch of the horizontal blanking period and is also the black level reference for the subsequent video scan line. The back porch is triggered from the rising edge of the sync tip. The pulse width of the back porch is about 29 times the internal oscillator clock cycle. For the NTSC video input, the pulse width of the back porch is about 3.5µs. In EL4501, the back porch pulse controls the sample and hold switch of the DC-restored loop.

Odd and Even Output

For a composite video signal that is interlaced, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. The odd and even circuit tracks the relationship of the horizontal pulses to the leading edge of the vertical output and will switch on every field at the start of vertical sync pulse interval. ODD/EVEN, pin 14 is high during the odd field and low during the even field.

Sync Amplitude Output

The output voltage at the SYNC AMP output (pin 17) is about 2 times the sync tip voltage. This signal can be used for AGC applications. When there is no sync signal at the input, the SYNC AMP output is 0V.

Loss of Sync Output

Loss of video signal can be detected by monitoring the LOS output at pin 10. LOS goes low indicating the EL4501 has locked to the right line rate. LOS goes high indicating the EL4501 is out of lock. When there is loss of sync, all the sync outputs go high, except ODD/EVEN.

Digital Filter Operation

The EL4501 contains a user-selectable digital filter which tracks the line rate and rejects high frequency noise and video artifacts, such as color burst. Basically, the digital filter delays all signals and filters out the pulses which are shorter than the filters delay time. The digital filter greatly reduces the jitters in the outputs. With the digital filter on, the jitter at the composite sync output is only 2ns. Figure 39 shows the jitter at the output when the digital filter is selected. However, the output waveforms will be delayed from 150ns to 300ns due to this filter. Refer to the performance curves for details. Applying logic high to the FSEL pin, the digital filter is enabled. Applying a logic low to the FSEL pin, the digital filter is disabled.

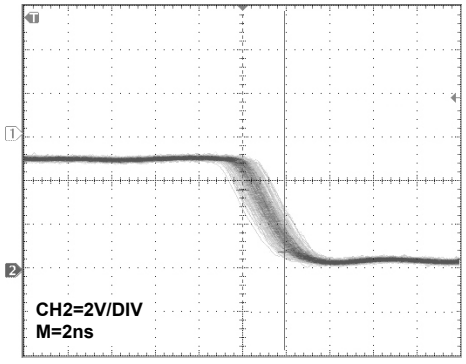


FIGURE 39. JITTER AT THE OUTPUTS WITH FSEL=1

R_{FREQ}

An external R_{FREQ} resistor, connected from pin 7 to ground, produces a reference current that is used internally as the timing reference for all the sync output delay time and output pulse widths. Decreasing the value of R_{FREQ} increases the reference current and frequency of the internal oscillator, which in turn decreases the reference time and pulse width. A higher frequency video input requires a lower R_{FREQ} value. The Line Rates vs R_{FREQ} performance curve shows the variation of line rate with R_{FREQ}.

Slice Mode and Operation with VCRs

Normally the signal source for the EL4501 is assumed to be clean and relatively noise free. If that is the case, the SLICE MODE pin (pin 16) should be connected to ground, which sets the slice level to 50% of the sync tip. Some signal sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference, such as VCR signals which generate lots of head switching noise. In this case, the SLICE MODE pin should be connected to logic high which sets the slice level to a fixed 100mV above the sync tip. Also, a single pole chroma filter is required at the composite video input to increase the S/N ratio of the incoming noisy video signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and 470pF capacitor to ground will form a low pass filter with a roll-off frequency of about 550kHz. This bandwidth sufficiently attenuates the 3.58MHz (NTSC) or 4.43MHz (PAL) color burst signal and high frequency spikes, yet passes the sync pulse portion without appreciable attenuation. The chroma filter will increase the propagation delay from the composite sync input to the outputs. Applying a chroma filter, setting the SLICE MODE pin and FSEL pin to high greatly improve the noise immunity performance in VCR applications.

Output Drive Capability

The outputs of the sync separator are not designed to drive heavy loads. For a 5V VDS, if the output is driving 5kΩ load to ground, the output high voltage is about 4.9V. If the output is driving 500Ω load, the output high voltage is down to 4.2V.

General

Power Dissipation

With the high output drive capability of the EL4501 video amplifier, it is possible to exceed the 125°C Absolute Maximum junction temperature under certain load current conditions. It is important to calculate the maximum junction temperature for a given application to determine if load conditions or package type need to be modified for the amplifier to remain in its safe operating region.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature (125°C)
- T_{AMAX} = Maximum ambient temperature (85°C)
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the product of total quiescent supply current and power supply voltage, plus the power in the IC due to the load. Assume no load at the sync separator outputs:

$$P_{DMAX} = V_S \times I_{SMAX} + V_{SD} \times I_{SDMAX} + \left[(V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \right]$$

where:

- V_S = Supply voltage
- V_{SD} = Digital supply
- I_{SMAX} = Maximum supply current
- I_{SDMAX} = Maximum digital supply current
- V_{OUT} = Maximum output voltage
- R_L = Load resistance tied to ground

Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. In normal operation, where the GND pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S to GND will suffice. To reduce cross talk between the analog signal path and the embedded sync separator, a separate digital supply pin, V_{SD} is included on the EL4501. This pin should be bypassed in a similar manner to V_S. For additional isolation a ferrite bead may be added in line with the supply connections to both pins. For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire wound resistors should be avoided because of their additional series inductance.