STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	Regulator IC for Memory termination
PRODUCT SERIES	**BD3532EFV**
FEATURES	・Incorporates a push-pull power supply for termination (VTT)
	・Incorporates a reference voltage circuit(VREF)

○ ABSOLUTE MAXIMUM RATINGS(Ta=100°C)

Parameter	Symbol	Limit	Unit
Input Voltage	VCC	7 *1	V
Enable Input Voltage	VEN	7 *1	V
Termination Input Voltage	VTT_IN1,VTT_IN2	7 *1	V
VDDQ Reference Voltage	VDDQ	7 *1	V
Output Current	ITT	3	A
Power Dissipation	Pd	1000*2	mW
Operating Temperature Range	Topr	-40～+100	°C
Storage Temperature Range	Tstg	-55～+150	°C
Maximum Junction Temperature	Tjmax	+150	°C

*1 Should not exceed Pd.
*2 Reduced by 8.0mW for each increase in Ta of 1°C over 25°C(When mounted on a board 70mm × 70mm × 1.6mm Glass-epoxyPCB).

○ RECOMMENDED OPERATING CONDITIONS(Ta=25°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Voltage	VCC	4.3	5.5	V
Termination Input Voltage	VTT_IN1,VTT_IN2	1.0	5.5	V
EN Input Voltage	VEN	-0.3	5.5	V

★ No radiation-resistant design is adopted for the present product.

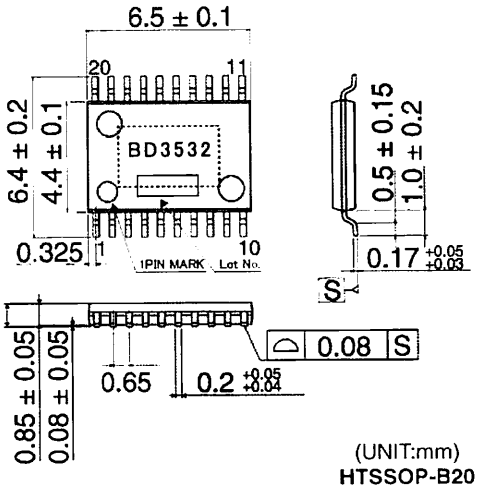
Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ ELECTRICAL CHARACTERISTICS (Unless otherwise specified,
Ta=25°C VCC=5V VEN=3V VDDQ=2.5V VTT_IN1=VTT_IN2=2.5V)

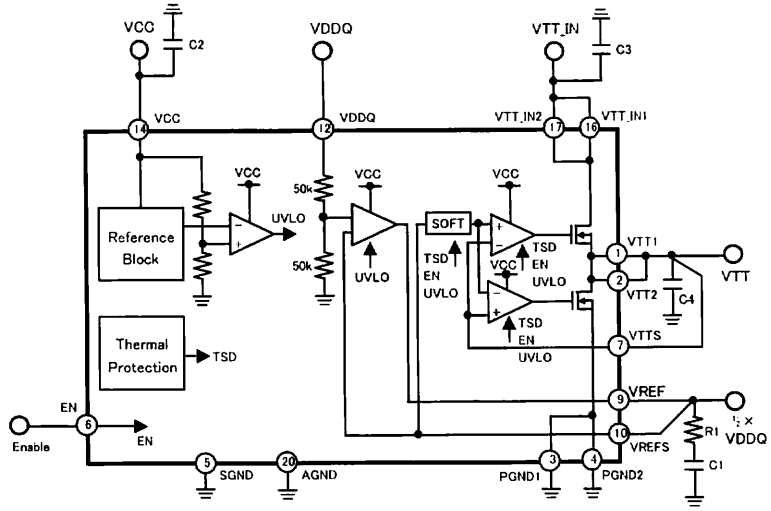
PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Standby Current	IST	-	0.8	1.6	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	
[Enable]						
High Level Enable Input Voltage	VENHI	2.3	-	5.5	V	VCC=4.3V to 5.5V Ta=0°C to 100°C *3
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	VCC=4.3V to 5.5V Ta=0°C to 100°C *3
Enable Pin Input Current	IEN	-	7	10	uA	VEN=3V
[Termination]						
Termination Output Voltage 1	VTT1	VREF-30 mV	VREF	VREF+30 mV	V	Io=-3A to 3A Ta=0°C to 100°C *3
Termination Output Voltage 2	VTT2	VREF-30 mV	VREF	VREF+30 mV	V	VDDQ=VTT_IN1=VTT_IN2=1.8V Io=-2A to 2A Ta=0°C to 100°C *3
Source Current 1	ITT1+	3	-	-	A	
Sink Current 1	ITT1-	-	-	-3	A	
Source Current 2	ITT2+	2	-	-	A	VDDQ=VTT_IN1=VTT_IN2=1.8V
Sink Current 2	ITT2-	-	-	-2	A	VDDQ=VTT_IN1=VTT_IN2=1.8V
Load Regulation 1	⊿VTT1	-	-	40	mV	Io=-3A to 3A
Load Regulation 2	⊿VTT2	-	-	35	mV	VDDQ=VTT_IN1=VTT_IN2=1.8V Io=-2A to 2A
Line Regulation 1	Reg.I	-	20	40	mV	VCC=4.3V to 5.5V
Line Regulation 2	Reg.2	-	20	40	mV	VCC=4.3V to 5.5V VDDQ=VTT_IN1=VTT_IN2=1.8V
Upper Side ON Resistance 1	HRON1	-	0.2	0.4	Ω	
Lower Side ON Resistance 1	LRON1	-	0.2	0.4	Ω	
Upper Side ON Resistance 2	HRON2	-	0.2	0.4	Ω	VDDQ=VTT_IN1=VTT_IN2=1.8V
Lower Side ON Resistance 2	LRON2	-	0.2	0.4	Ω	VDDQ=VTT_IN1=VTT_IN2=1.8V
[Input of Reference Voltage]						
Input Impedance	ZVDDQ	70	100	130	kΩ	
[Reference voltage]						
Output Voltage 1	VREF1	1/2 × VDDQ -30mV	1/2 × VDDQ	1/2 × VDDQ +30mV	V	IREF=0mA
Output Voltage 2	VREF2	1/2 × VDDQ -40mV	1/2 × VDDQ	1/2 × VDDQ +40mV	V	IREF=-10mA to 10mA Ta=0°C to 100°C *3
Output Voltage 1'	VREF1'	1/2 × VDDQ -30mV	1/2 × VDDQ	1/2 × VDDQ +30mV	V	VDDQ=VTT_IN1=VTT_IN2=1.8V IREF=0mA
Output Voltage 2'	VREF2'	1/2 × VDDQ -40mV	1/2 × VDDQ	1/2 × VDDQ +40mV	V	VDDQ=VTT_IN1=VTT_IN2=1.8V IREF=-10mA to 10mA Ta=0°C to 100°C *3
Source Current 1	IREF1+	20	-	-	mA	
Sink Current 1	IREF1-	-	-	-20	mA	
Source Current 2	IREF2+	20	-	-	mA	VDDQ=VTT_IN1=VTT_IN2=1.8V
Sink Current 2	IREF2-	-	-	-20	mA	VDDQ=VTT_IN1=VTT_IN2=1.8V
[UVLO]						
UVLO OFF Voltage	VUVLO	4.0	4.15	4.3	V	VCC : sweep up
Hysteresis Voltage	⊿VUVLO	100	160	220	mV	VCC : sweep down

*3 Design Guarantee

○PHYSICAL DIMENSIONS



○ BLOCK DIAGRAM



○ Pin number Pin name

PIN No.	Pin name
1	VTT1
2	VTT2
3	PGND1
4	PGND2
5	SGND
6	EN
7	VTTS
8	N.C
9	VREF
10	VREFS
11	N.C
12	VDDQ
13	N.C
14	VCC
15	N.C
16	VTT_IN1
17	VTT_IN2
18	N.C
19	N.C
20	AGND
-	FIN

ONOTES FOR USE

(1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.

(5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	15

(7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Output Capacitor (C2, R1)
Mount an output capacitor and resistor between VREF and GND for stability purposes. The VREF output capacitor and resistor are for the open loop gain phase compensation. If the capacitor and resistor value are not large enough, the output voltage may oscillate. A ceramic 1.0 - 2.2uF capacitor with minimal susceptibility to temperature and 0.5 – 2.2 ohm resistor in series with this capacitor, or a 10uF ceramic capacitor, or a tantalum 10uF capacitor (TCFGPOJ106M8R: ROHM) are recommended. However, this stability depends on the characteristics of temperature and load. Please confirm operation across a variety of temperature and load conditions.

(9) Output Capacitor (C1)
Mount an output capacitor between VTT and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A 220uF polymer capacitor is recommended. However, the stability depends on the characteristics of temperature and load conditions. And if a small ESR capacitor such as a ceramic capacitor is utilized, the output voltage may oscillate due to lack of phase margin. In this case, measures can be taken by adding a resistor in series with this capacitor. Please confirm operation across a variety of temperature and load conditions.

(10) Input Capacitor (C3, C4)
The input capacitor reduces the output impedence of the voltage supply source connected in the VCC and VTT_IN. If the output impedence of this power supply increases, the input voltage (VCC,VTT_IN) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 1uF capacitor in VCC and 10uF capacitor in VTT_IN with minimal susceptibility to temperature are preferable, but stability depends on power supply characteristics and the substrate wiring pattern (a parasitic capacitance and impedance). Please confirm operation across a variety of temperature and load conditions.

(11) Input (VCC, VDDQ, VTT_IN, EN)
The VCC, VDDQ, VTT_IN, and EN are isolated. The UVLO function is integrated to protect faulty operation due to low voltage levels of VCC. VTT output voltage starts up when VCC reaches the UVLO threshold level and EN reaches the threshold level respectively regardless of the start up order in those inputs. And also VREF output voltage starts up when VCC reaches the UVLO threshold level. Please short VTT_IN1 and VTT_IN2.

(12) VTTS and VREFS
VTTS and VREFS are to improve load regulation of VTT and VREF output. For precise load regulation, VTTS and VREFS are connected close by VTT and VREF respectively to avoid common impedance. Please short VTT1 and VTT2.

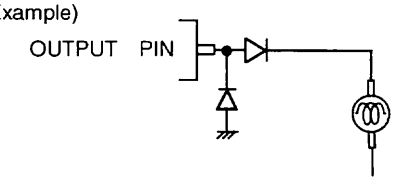
(13) GND Terminal
Basically, AGND, SGND, PGND1, and PGND2 are shorted as common GND pin. To minimize the packag power, measures can be taken by adding low resistance between SGND and PGND1 or PGND2.

(14) Heat Sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND.

(15) This product is not designed for protection against radioactive rays.

(16) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Example)



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U.S.A / San Diego	TEL : +1(858)625-3630	FAX : +1(858)625-3670
Atlanta	TEL : +1(770)754-5972	FAX : +1(770)754-0691
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Germany / Dusseldorf	TEL : +49(2154)9210	FAX : +49(2154)921400
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China / Hong Kong	TEL : +852(2)740-6262	FAX : +852(2)375-8971
Shanghai	TEL : +86(21)6279-2727	FAX : +86(21)6247-2066
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Beijing	TEL : +86(10)8525-2483	FAX : +86(10)8525-2489
Taiwan / Taipei	TEL : +866(2)2500-6956	FAX : +866(2)2503-2869
Korea / Seoul	TEL : +82(2)8182-700	FAX : +82(2)8182-715
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Japan /
(Internal Sales)

Tokyo 2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082
TEL : +81(3)5203-0321 FAX : +81(3)5203-0300

Yokohama 2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575
TEL : +81(45)476-2131 FAX : +81(45)476-2128

Nagoya Dainagayo Building 9F 3-28-12, Meieki, Nakamura-ku, Nagoya,Aichi 450-0002
TEL : +81(52)581-8521 FAX : +81(52)561-2173

Kyoto 579-32 Higashi Shiokouji-cho, Karasuma Nishi-iru, Shiokoujidori, Shimogyo-ku, Kyoto 600-8216
TEL : +81(75)311-2121 FAX : +81(75)314-6559

(Contact address for overseas customers in Japan)

Yokohama TEL : +81(45)476-9270 FAX : +81(045)476-9271

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