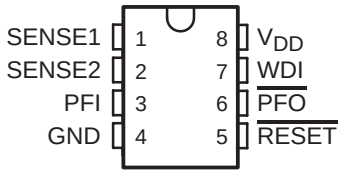
- **Qualified for Automotive Applications**
- **Dual Supervisory Circuits With Power Fail for DSP and Processor-Based Systems**
- **Voltage Monitor for Power Fail or Low-Battery Warning**
- **Watchdog Timer With 0.8-s Time-Out**
- **Power-On Reset Generator With Integrated 100-ms Delay Time**
- **Open-Drain Reset and Power-Fail Output**
- **Supply Current of 15 μA (Typ)**
- **Supply Voltage Range . . . 2.7 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output From $V_{DD} \geq 1.1$ V**
- **SO-8 Package**
- **Temperature Range . . . −40°C to 125°C**
- **Applications Include:**
  Multivoltage DSPs and Processors
  Portable Battery-Powered Equipment
  Embedded Control Systems
  Intelligent Instruments
  Automotive Systems

D PACKAGE
(TOP VIEW)

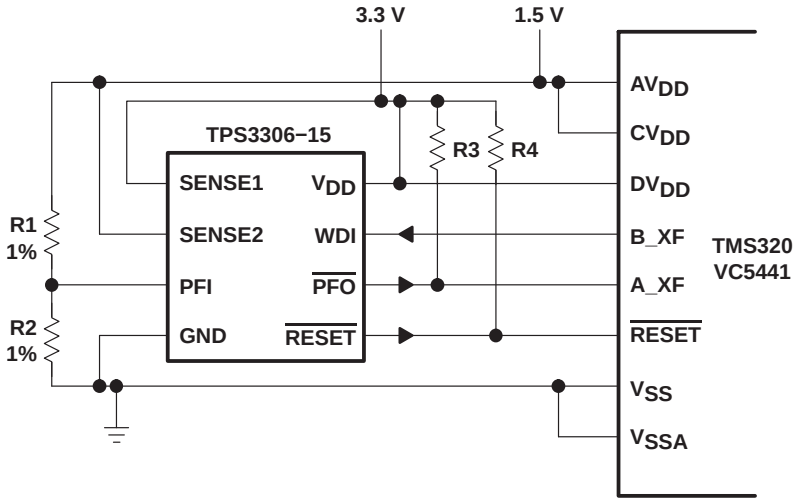


description

The TPS3306 family is a series of supervisory circuits designed for circuit initialization, which require two supply voltages, primarily in DSP and processor-based systems.

The product spectrum of the TPS3306-xx is designed for monitoring two independent supply voltages of 3.3 V/1.5 V, 3.3 V/1.8 V, 3.3 V/2 V, 3.3 V/2.5 V, or 3.3 V/5 V.

TYPICAL OPERATING CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

The various supervisory circuits are designed to monitor the nominal supply voltage, as shown in the following supply-voltage monitoring table.

SUPPLY-VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3306-15	3.3 V	1.5 V	2.93 V	1.4 V
TPS3306-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3306-20	3.3 V	2 V	2.93 V	1.85 V
TPS3306-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3306-33	5 V	3.3 V	4.55 V	2.93 V

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage, V_{DD}, becomes higher than 1.1 V. Thereafter, the supervisory circuits monitor the SENSEn inputs and keep $\overline{\text{RESET}}$ active as long as SENSEn remains below the threshold voltage, V_{IT}.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(typ)}$ = 100 ms, starts after SENSE1 and SENSE2 inputs have risen above V_{IT}. When the voltage at SENSE1 or SENSE2 input drops below the V_{IT}, the output becomes active (low) again.

The integrated power-fail (PFI) comparator with separate open-drain ($\overline{\text{PFO}}$) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3306-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of the watch-dog timer (WDI). When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$ = 0.50 s, $\overline{\text{RESET}}$ becomes active for the time period t_d . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3306-xx devices are available in standard 8-pin SO packages.

The TPS3306-xxQ family is characterized for operation over a temperature range of −40°C to 125°C.

AVAILABLE OPTIONS†

T_A	PACKAGED DEVICES‡		TOP-SIDE MARKING
	SMALL OUTLINE (D)		
−40°C to 125°C	Tape and reel	TPS3306-15QDRQ1	615Q1
	Tape and reel	TPS3306-18QDRQ1	618Q1
	Tape and reel	TPS3306-20QDRQ1	620Q1
	Tape and reel	TPS3306-25QDRQ1	625Q1
	Tape and reel	TPS3306-33QDRQ1	633Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

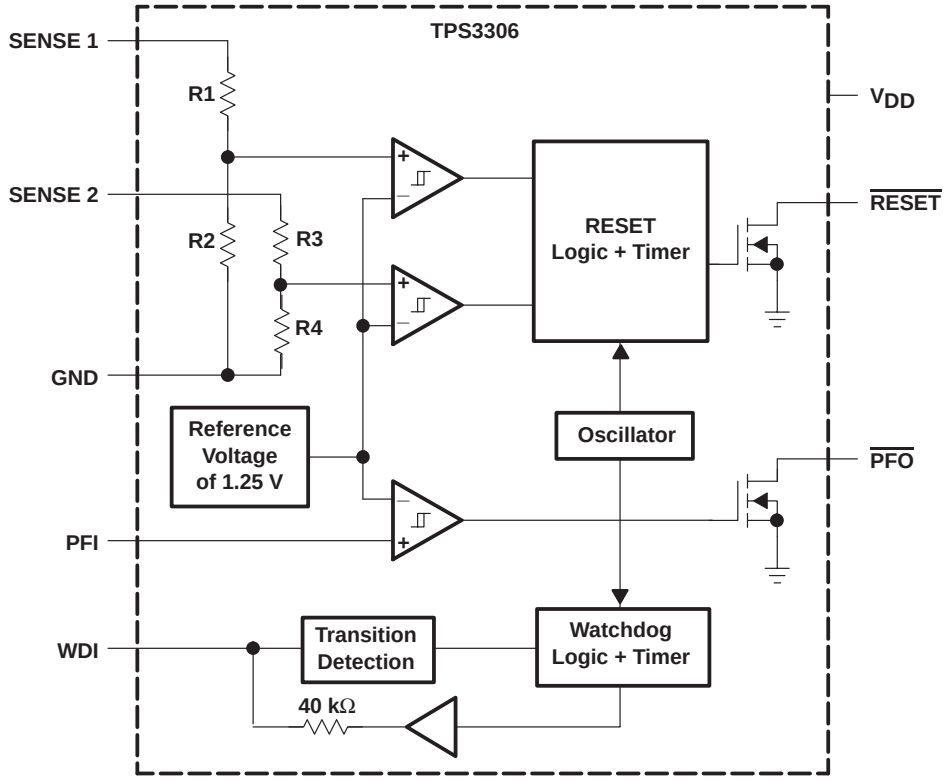
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

FUNCTION/TRUTH TABLES

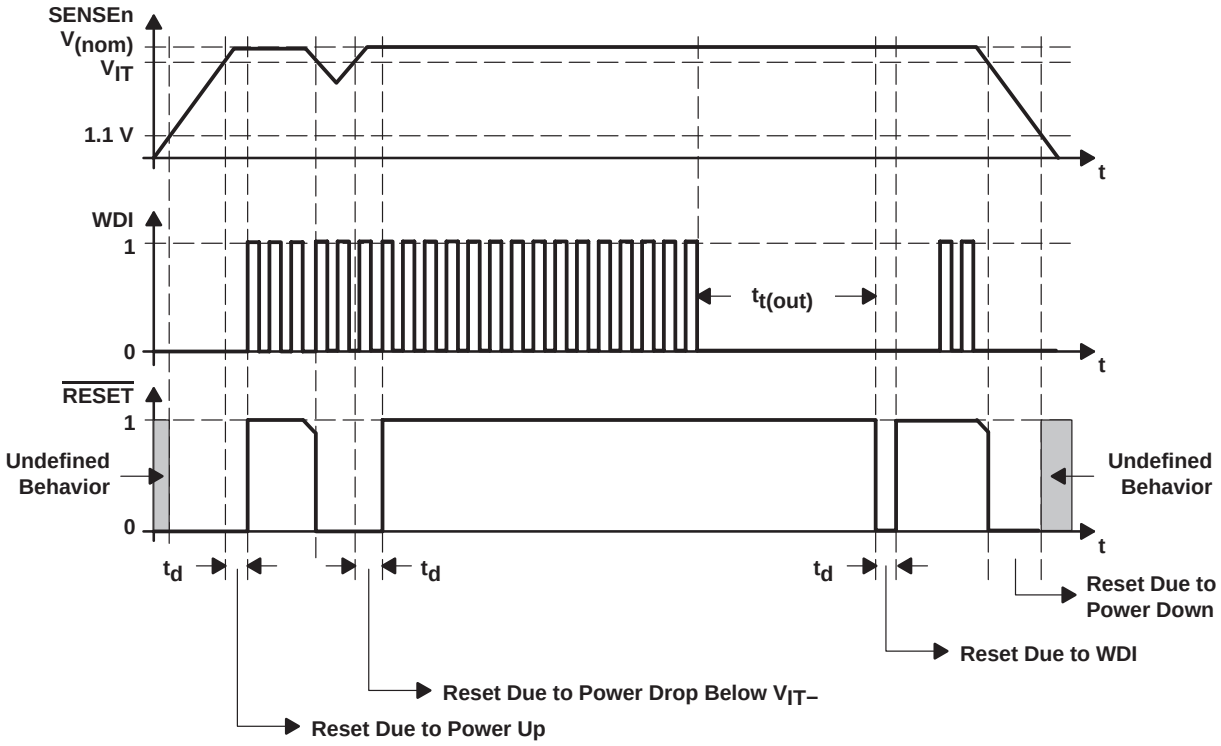
SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	$\overline{\text{RESET}}$
0	0	L
0	1	L
1	0	L
1	1	H

PFI > V_{IT}	$\overline{\text{PFO}}$	TYPICAL DELAY
0→1	L→H	0.5 µs
1→0	H→L	0.5 µs

functional block diagram



timing diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4	I	Ground
PFI	3	I	Power-fail comparator input
$\overline{\text{PFO}}$	6	O	Power-fail comparator output, open drain
$\overline{\text{RESET}}$	5	O	Active-low reset output, open drain
SENSE1	1	I	Sense voltage 1
SENSE2	2	I	Sense voltage 2
WDI	7	I	Watchdog timer input
V_{DD}	8	I	Supply voltage

detailed description

watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to typically toggle the watchdog input (WDI) within 0.8 s to avoid a time-out occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected or tied with a high-impedance driver, the watchdog is disabled and is retriggered internally.

saving current while using the watchdog

WDI is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If, instead, WDI is externally driven high for the majority of the time-out period, a current of 5 V/40 kΩ ≈ 125 μA can flow into WDI.

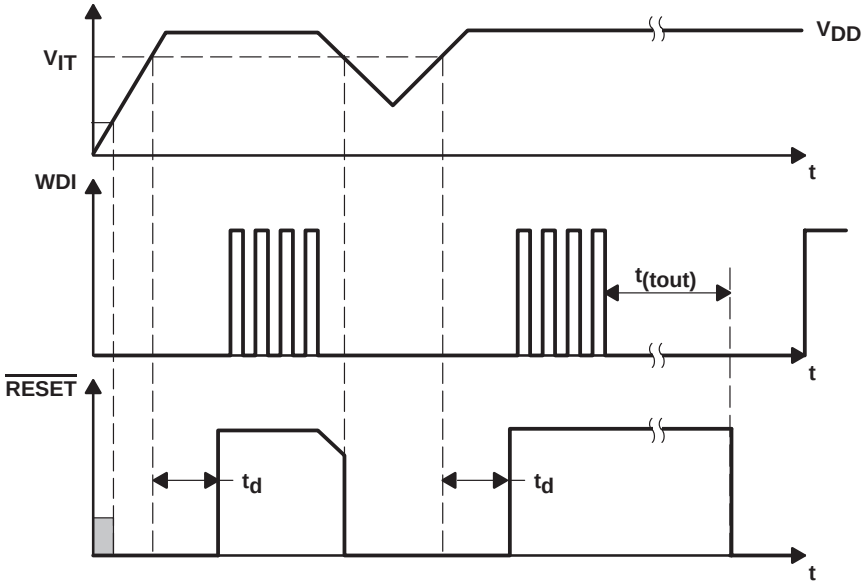
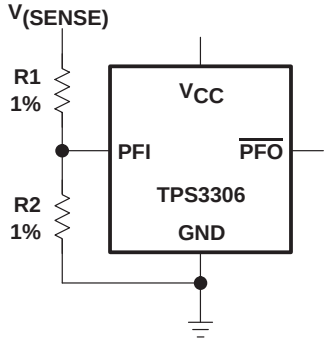


Figure 1. Watchdog Timing

power-fail comparator (PFI and $\overline{\text{PFO}}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) is compared with an internal voltage reference of 1.25 V. If the input voltage falls below the power-fail threshold (V_{PFI}) of 1.25 V (typ), the power-fail output ($\overline{\text{PFO}}$) goes low. If $\overline{\text{PFO}}$ goes above 1.25 V plus about 10−mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above 1.25 V. The sum of both resistors should be approximately 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave $\overline{\text{PFO}}$ unconnected.

$$V_{PFI,trip} = 1.25\ V \times \frac{R_1 + R_2}{R_2}$$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note1): V_{DD} . . . . . 7 V
All other pins . . . . . −0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 5 mA
Maximum high output current, I_{OH} . . . . . −5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than t = 1000 h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	6	V
Input voltage at WDI and PFI, V_I	0	V_{DD} + 0.3	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD} + 0.3)V_{IT}/1.25$ V	V
High-level input voltage at WDI, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage at WDI, V_{IL}		$0.3 \times V_{DD}$	V
Operating free-air temperature range, T_A	−40	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$, $\overline{\text{PFO}}$	V_{DD} = 2.7 V to 6 V, I_{OL} = 20 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage (see Note 2)		$V_{DD} \geq$ 1.1 V, I_{OL} = 20 µA			0.4	V
V_{IT}	Negative-going input threshold voltage (see Note 3)	VSENSE1, VSENSE2	V_{DD} = 2.7 V to 6 V, T_A = −40°C to 125°C	1.35	1.4	1.44	V
				1.62	1.68	1.74	
				1.79	1.85	1.91	
				2.18	2.25	2.34	
				2.84	2.93	3.04	
				4.44	4.55	4.68	
		PFI		1.2	1.25	1.3	
V_{hys}	Hysteresis	PFI	V_{IT} = 1.25 V		10		mV
		VSENSEn	V_{IT} = 1.4 V		15		
			V_{IT} = 1.68 V		15		
			V_{IT} = 1.86 V		20		
			V_{IT} = 2.25 V		20		
			V_{IT} = 2.93 V		30		
			V_{IT} = 4.55 V		40		
$I_{H(AV)}$	Average high-level input current	WDI	WDI = V_{DD} = 6 V, Time average (dc = 88%)		100	150	µA
$I_{L(AV)}$	Average low-level input current	WDI	WDI = 0 V, V_{DD} = 6 V, Time average (dc = 12%)		−15	−20	µA
I_H	High-level input current	WDI	WDI = V_{DD} = 6 V		120	170	µA
		SENSE1	V_{SENSE1} = V_{DD} = 6 V		5	10	
		SENSE2	V_{SENSE2} = V_{DD} = 6 V		6	10	
I_L	Low-level input current	WDI	WDI = 0 V, V_{DD} = 6 V		−120	−170	µA
I_I	Input current	PFI	V_{DD} = 6 V, 0 V ≤ V_I ≤ V_{DD}	−30		30	nA
I_{DD}	Supply current				15	40	µA
C_i	Input capacitance		V_I = 0 V to V_{DD}		10		pF

NOTES: 2. The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. t_r, $V_{DD} \geq$ 15 µs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 µF) should be placed close to the supply terminals.

timing requirements at V_{DD} = 2.7 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL}$ = V_{IT} − 0.2 V, $V_{SENSEnH}$ = V_{IT} + 0.2 V	6		µs
		WDI	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.3 × V_{DD}	100		ns

switching characteristics at V_{DD} = 2.7 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time-out			$V_{I(SENSEn)} \geq V_{IT}$ + 0.2 V, See timing diagram	0.5	0.8	1.2	s
t_d	Delay time			$V_{I(SENSEn)} \geq V_{IT}$ + 0.2 V, See timing diagram	70	100	140	ms
t_{PHL}	Propagation (delay) time, high- to low-level output	SENSEn	$\overline{\text{RESET}}$	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ − 0.2 V		1	5	µs
t_{PHL}	Propagation (delay) time, high- to low-level output	PFI	$\overline{\text{PFO}}$			0.5	1	µs
t_{PLH}	Propagation (delay) time, low- to high-level output							

TYPICAL CHARACTERISTICS

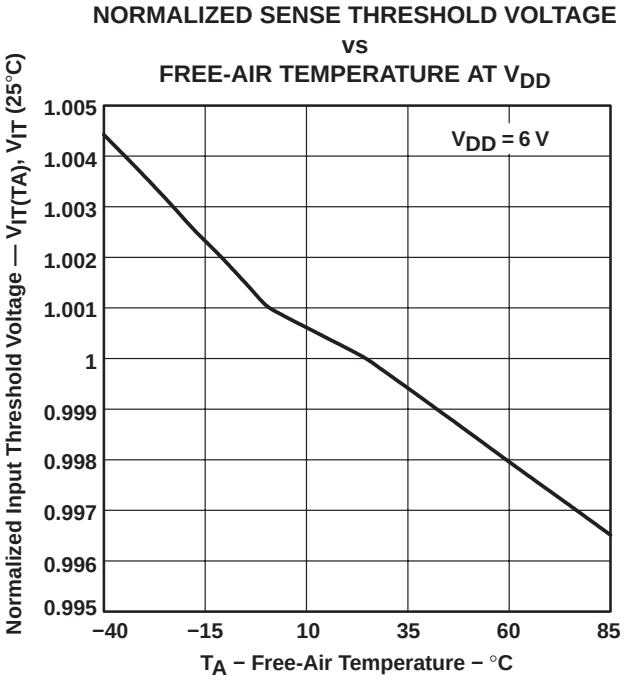


Figure 2

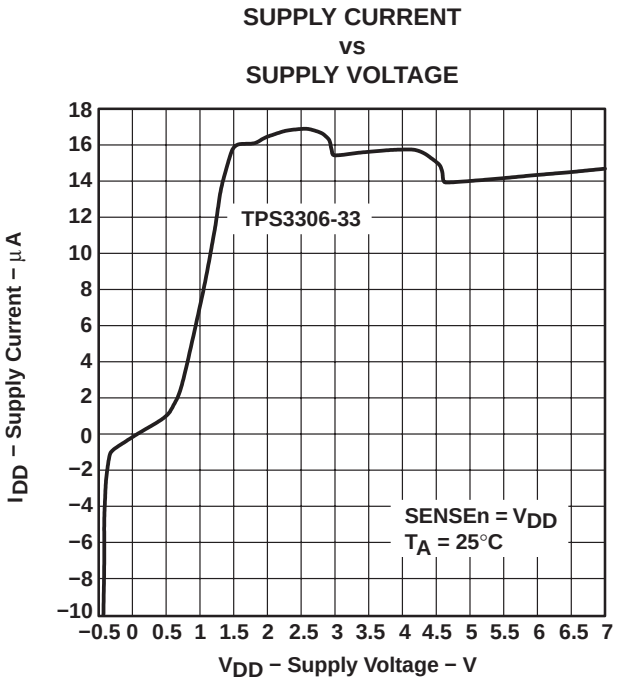


Figure 3

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

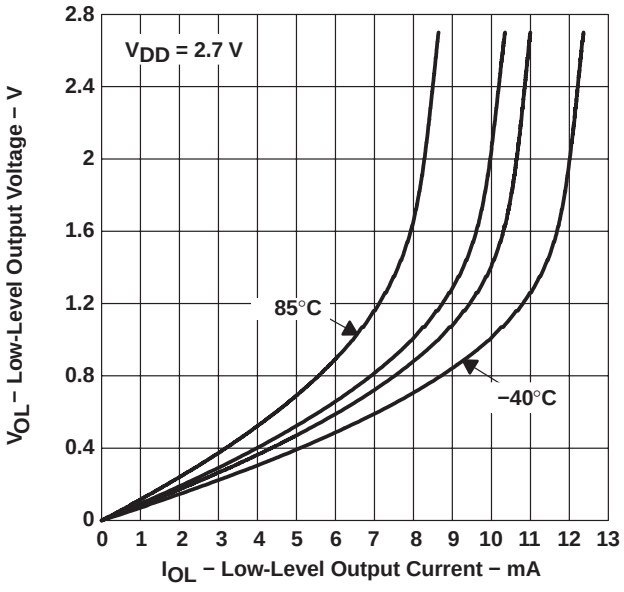


Figure 4

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

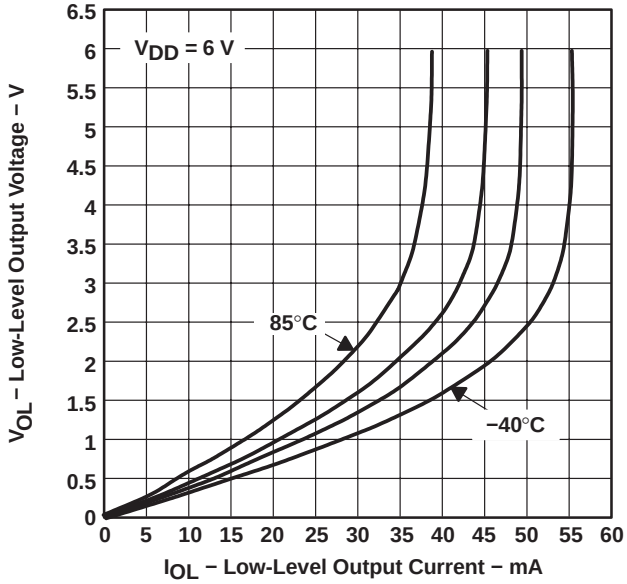


Figure 5

MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE

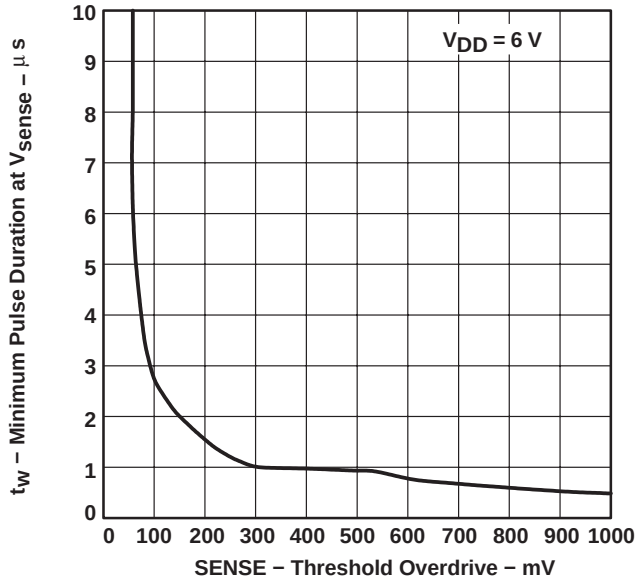


Figure 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3306-15QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	615Q1	Samples
TPS3306-15QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	615Q1	Samples
TPS3306-18QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	618Q1	Samples
TPS3306-18QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	618Q1	Samples
TPS3306-20QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	620Q1	Samples
TPS3306-25QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	625Q1	Samples
TPS3306-33QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	633Q1	Samples
TPS3306-33QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	633Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3306-Q1 :

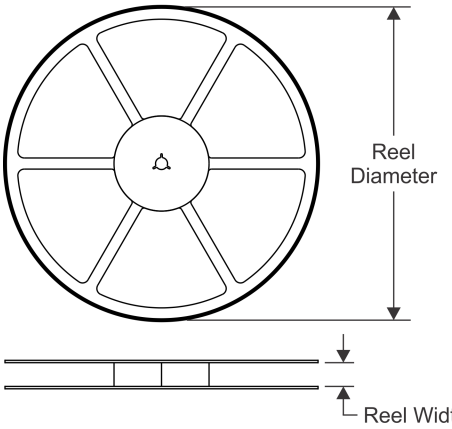
- Catalog: TPS3306

NOTE: Qualified Version Definitions:

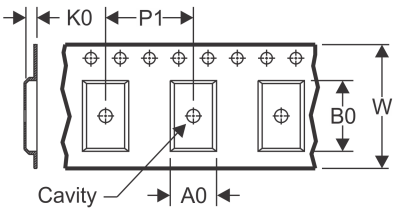
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

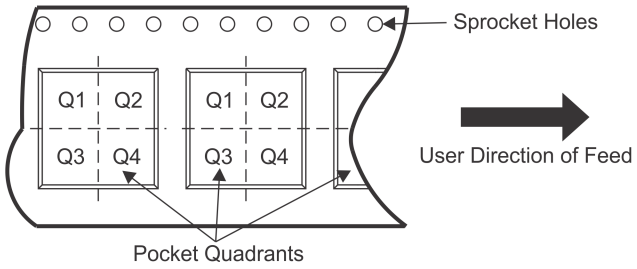


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

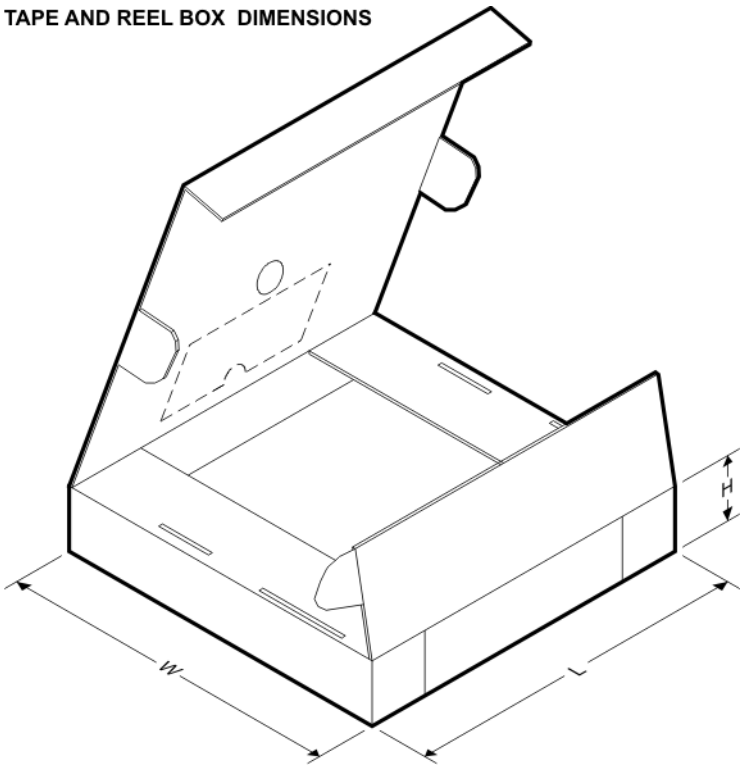
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3306-15QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3306-33QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

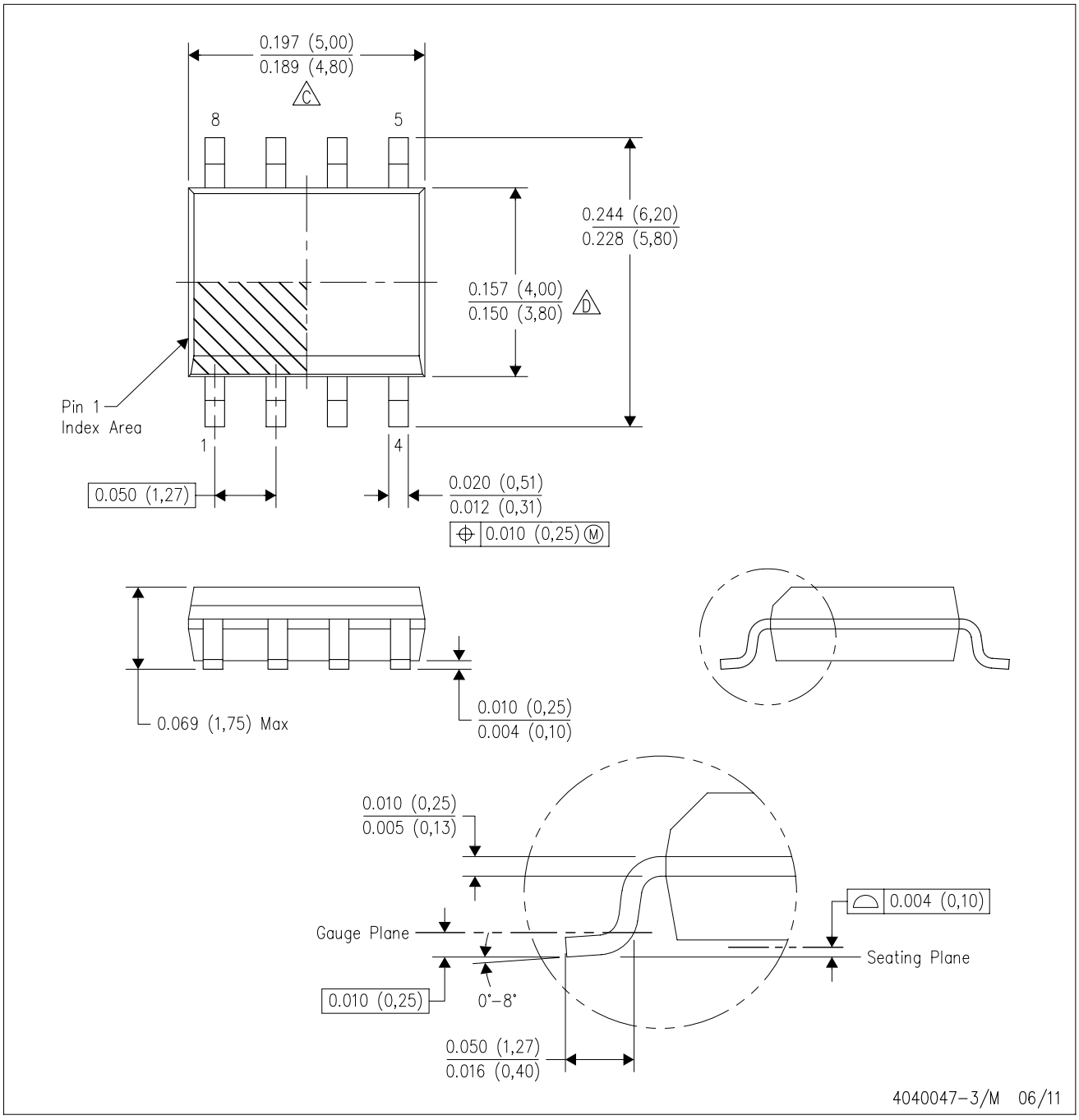
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

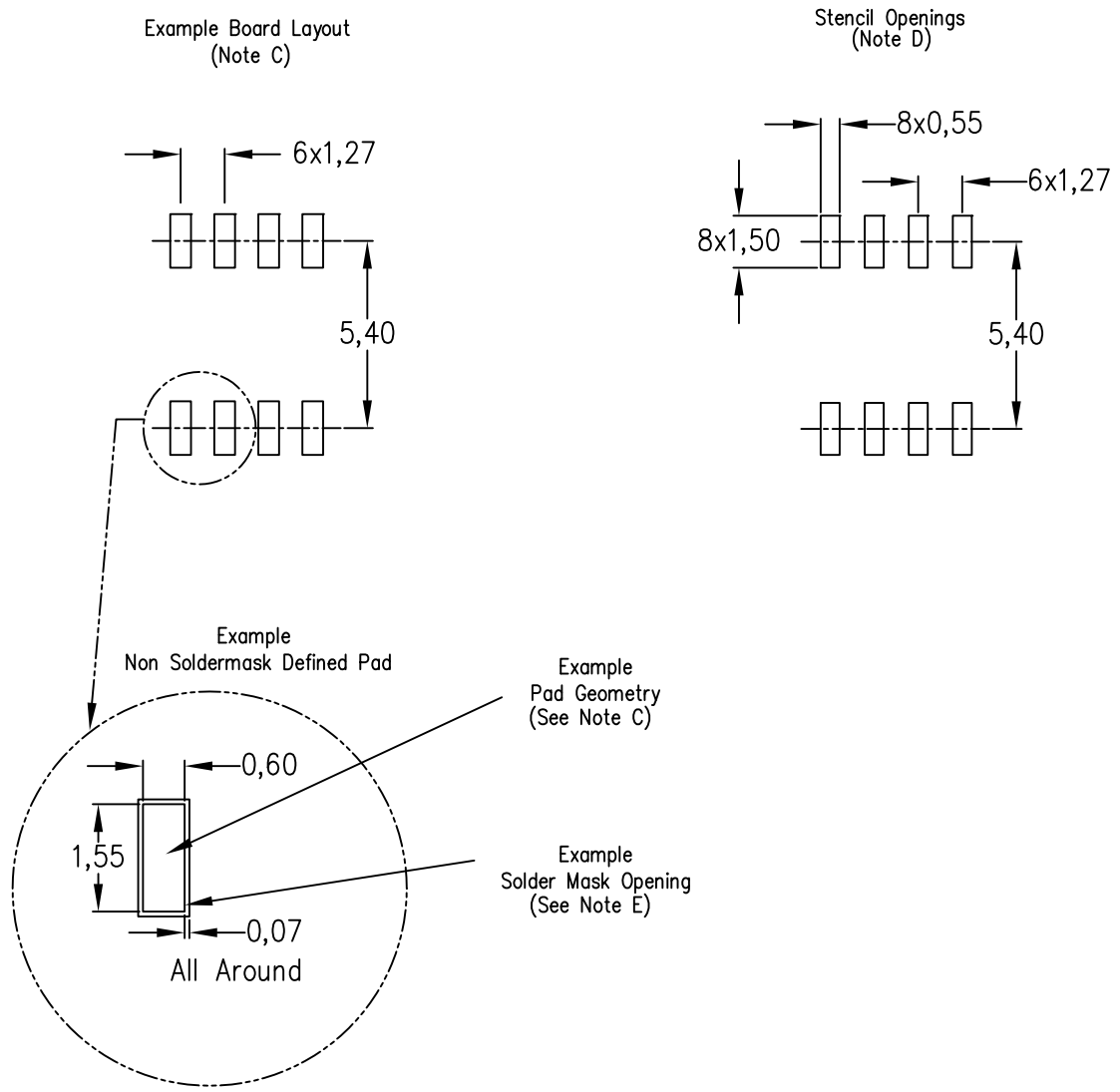
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3306-15QDRQ1	SOIC	D	8	2500	367.0	367.0	38.0
TPS3306-33QDRQ1	SOIC	D	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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