



POCSAG DECODER FOR PAGERS

GENERAL DESCRIPTION

The W93902 is a very-low-power decoder for pagers that is fully compatible with CCIR Radio Paging Code Number 1 (POCSAG code) operating at 512, 1200, or 2400 bps using a single 76.8 KHz crystal.

To enhance the sensitivity of the pager system, a digital filter and digital PLL have been incorporated to remove the noise factor generated by the RF part and lock the signal phase.

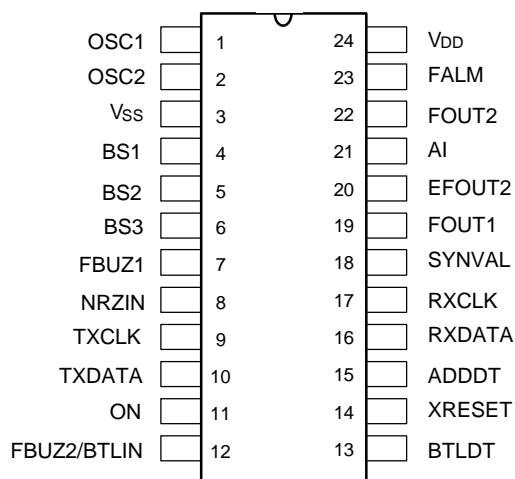
To reduce the RF turn-on time and minimize power consumption, an advanced synchronization algorithm (1/18 turn on-time, as opposed to 1/17 or 1/16) is used to provide synchronization. Synchronization skip mode is also available for power reduction.

For convenient pager programming, the decoder provides fully software-programmable options and a simple CPU control format (data output packaged as 4/7/8 bits or not packaged). Also included are independent buzzer and LED frequency control outputs and a reference clock (32768 Hz, 64 Hz, 16 Hz, 1/60 Hz) that can be output or disabled. The decoder supports four independent user addresses, which can be assigned to different frames.

FEATURES

- Data rate of 512, 1200, or 2400 bps
- 32768 Hz or 76800 Hz crystal
- Embedded digital filter and digital PLL
- Real two-random-bit error correction or one-bit error correction ability, plus four-bit burst error correction can be selected
- 1/18 RF enable time (more efficient than 1/17 or 1/16)
- Four real independent user address in different frames
- 25% to 75% duty cycle data capability in receive mode
- 2.7/3.2/2/4 KHz frequency output controlled by two pins, FBUZ1 and FBUZ2
- 6-bit/8-bit preamble acknowledge selection
- Four preamble search delay time settings
- Selection of from 1 to 15 sync search retry attempts
- Multi-frequency output for LED or other usage
- Inversion or non-inversion NRZIN signal and BS1/BS2/BS3 selection
- 4/7/8 bits package per byte output selection for receiving messages
- Independent power-saving control pin allows device to enter or exit reception mode at any time
- 16 selections for RF and PLL stable time
- Five selections for out-of-range indication
- Two selections for end-of-message condition
- Embedded power-on reset circuit
- Four Rxclk rate selection
- 2.5 to 5V operating voltage range
- Packaged in small size 24-pin SSOP

PIN CONFIGURATION



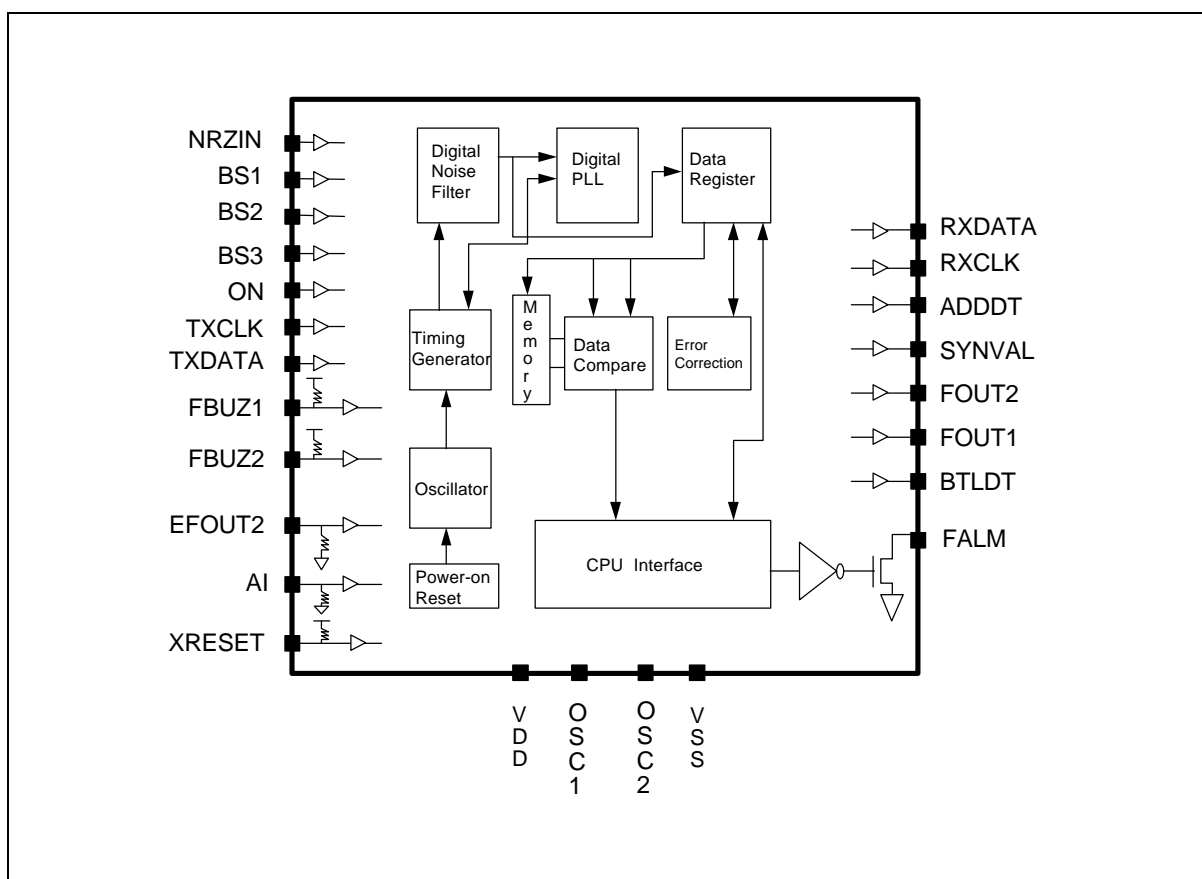
PIN DESCRIPTION

PIN	SYMBOL	I/O	DESCRIPTION
1	OSC1	Input	Crystal oscillator input (32768 Hz or 76.8 KHz)
2	OSC2	Output	Crystal oscillator output
3	V _{SS}	Power	Ground
4	BS1	Output	RF control pin
5	BS2	Output	RF quick charge pin
6	BS3	Output	PLL control pin
7	FBUZ1	Input	Buzzer frequency select pin 1 (with internal pull-up)
8	NRZIN	Input	NRZ signal input (inversion or non-inversion)
9	TXCLK	Input	Address data and option data strobe clock
10	TXDATA	Input	Address data and option data input
11	ON	Input	Receive mode enable pin
12	FBUZ2/BTLIN	Input	Buzzer frequency select pin 2 (with internal pull-up resistor)
13	BTLDT	Output	Battery low detect indicator output
14	XRESET	Input	Chip reset pin (internal pull-up resistor, low reset)
15	ADDDT	Output	Address received detector output (normal high)

Pin Description, continued

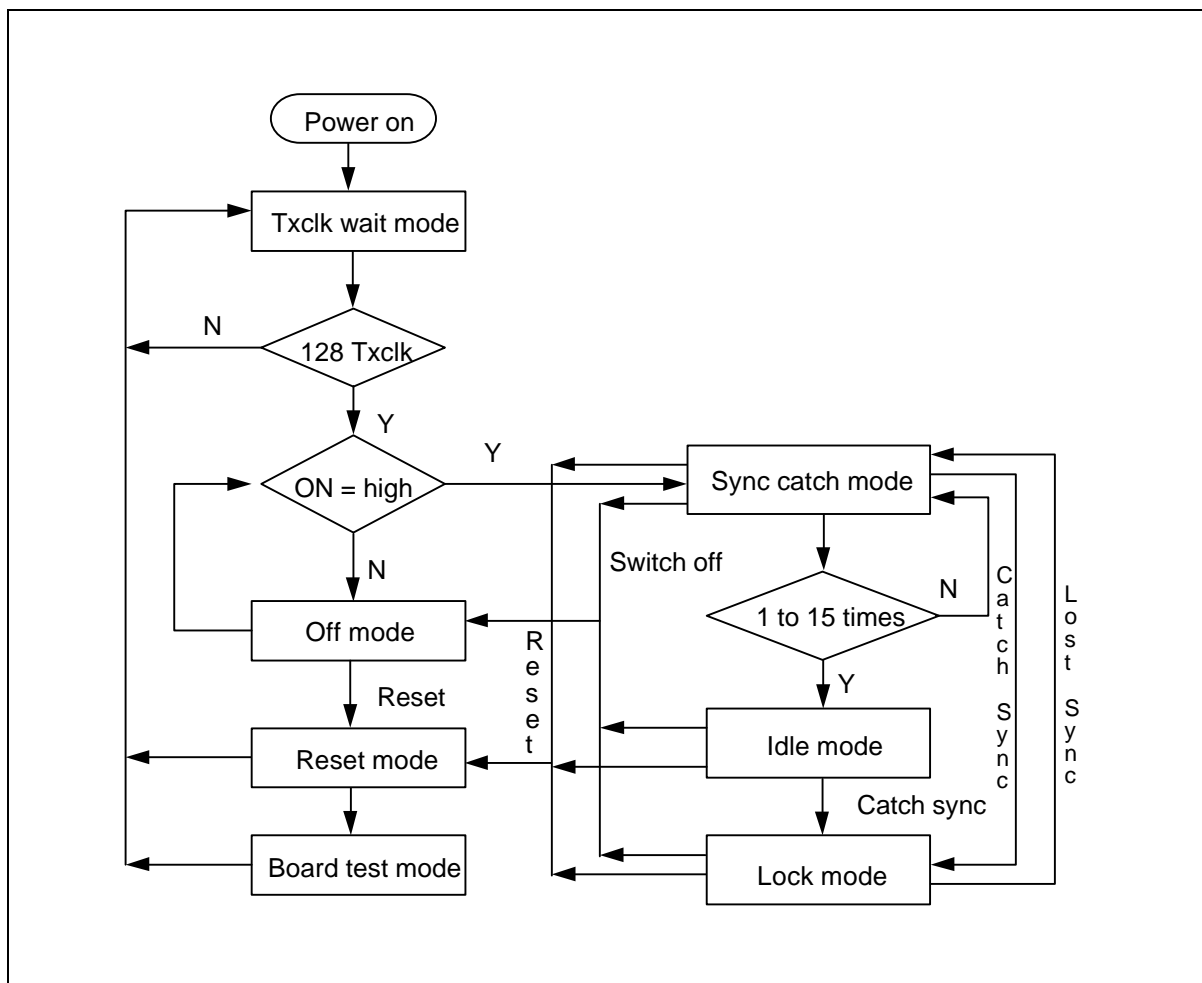
PIN	SYMBOL	I/O	DESCRIPTION
16	RXDATA	Output	Received data output pin
17	RXCLK	Output	Received data output strobe clock
18	SYNVAL	Output	Sync word detector output (out-of-range indicator output)
19	FOUT1	Output	Clock output (32768 Hz, 64 Hz, 16 Hz, 1/60 Hz or disable)
20	EFOUT2	Input	Multi-frequency output enable pin (internal pull-down resistor)
21	AI	Input	FALM buzzer output enable pin (internal pull-down resistor)
22	FOUT2	Output	Multi-frequency output
23	FALM	Output	2.7 KHz, 3.2 KHz, 2 KHz, 4 KHz, buzzer output (normal high)
24	VDD	Power	Power supply input (2.5 to 5V)

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation Flow Chart



Txclk Wait Mode

After the power-on stage or the XRESET pin goes from low to high, the W93902 enters Txclk wait mode. In this mode, the CPU should send 128 clock inputs to the TXCLK pin and address and options data to the TXDATA pin. After 128 clocks are sent, the chip is programmed and enters the mode determined by the ON pin. If more than 128 strobe clocks are sent to TXCLK, the chip ignores the extra clocks.

The programming timing is shown in Figure 1, and programming data are shown in Table 1 to Table 30. Data are latched at the rising edge of the strobe clock.

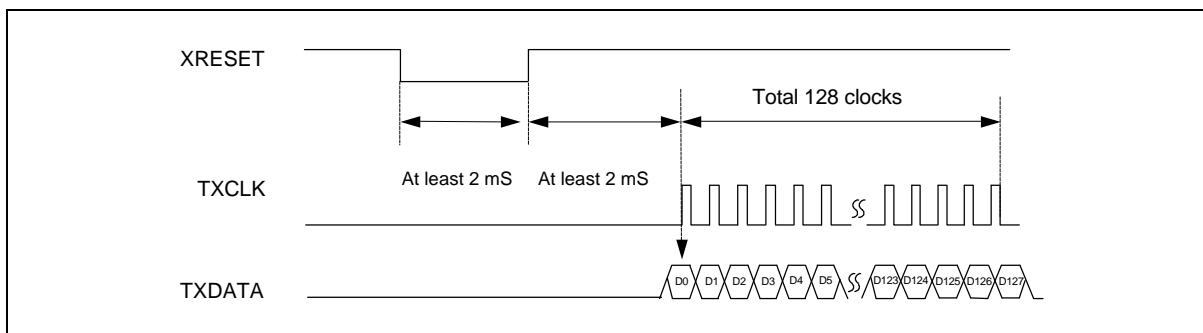


Figure 1. Programming Timing

Off Mode

After the W93902 has received 128 TXCLKs it will enter sync catch mode, if the ON pin is high, or off mode, if the ON pin is low. When the chip is in off mode, all output pins are inactive except for the Fout pin. Thus in off mode the chip provides only a timer reference clock function.

The chip can be switched on or off at any time by setting the ON pin to high or low, respectively.

Sync Catch Mode

In sync catch mode, the W93902 uses special timing to detect the synchronization codeword. First, when the ON pin goes from low to high, BS1 and BS3 remain high for up to four batches (4.5 sec for 512 bps and 1.92 sec for 1200 bps) to search for the preamble codeword or synchronization codeword. The detailed timing is shown below.

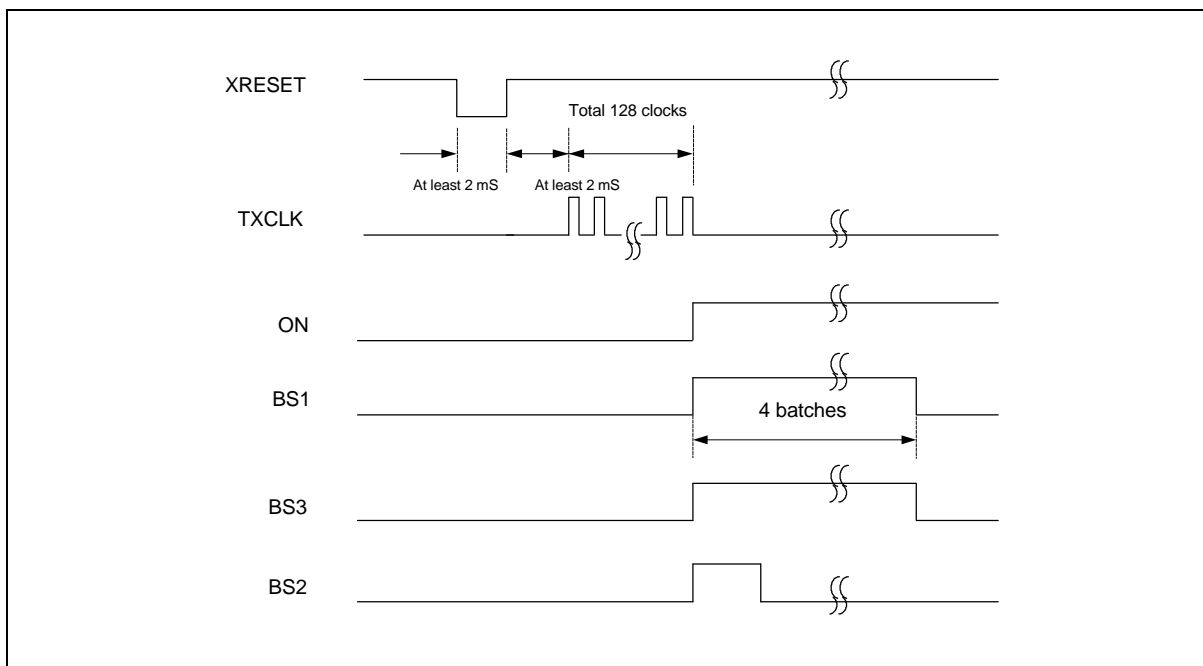


Figure 2

Note: The BS1 is to control the RF power, the BS2 is to discharge, and the BS3 is used to control the PLL power.

If no preamble or synchronization codeword is detected during the first four batches, the chip enters the second stage, in which 1/3 turn-on time is used every 576 bits (one batch) to detect synchronization or preamble for 1 to 15 batches, depending on the setting of TD1 to TD3. If a synchronization codeword is matched during these two stages, the chip enters lock mode. If no codeword is matched, the chip enters idle mode.

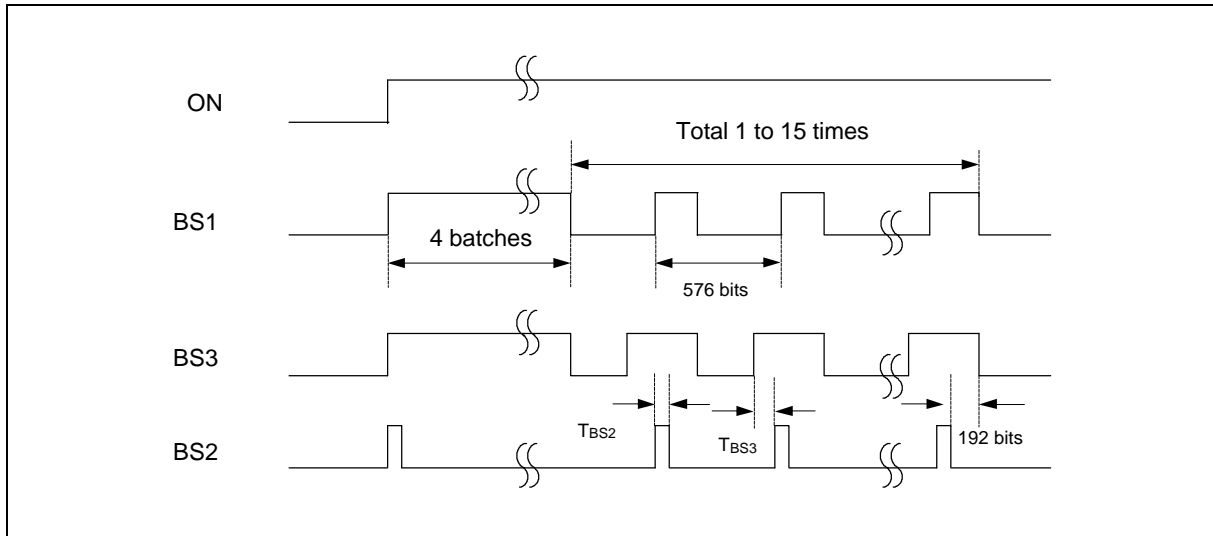


Figure 3

Idle Mode

In sync catch mode the chip attempts to achieve synchronization in a short period of time, but the RF power consumption in this mode is quite high. Consequently if there is no meaningful signal input, the chip enters idle mode to reduce the power consumption. If a preamble or synchronization codeword is present, however, it can still be detected by using 1/18 RF turn-on time ($T_{ON} = 32$ bits duration time).

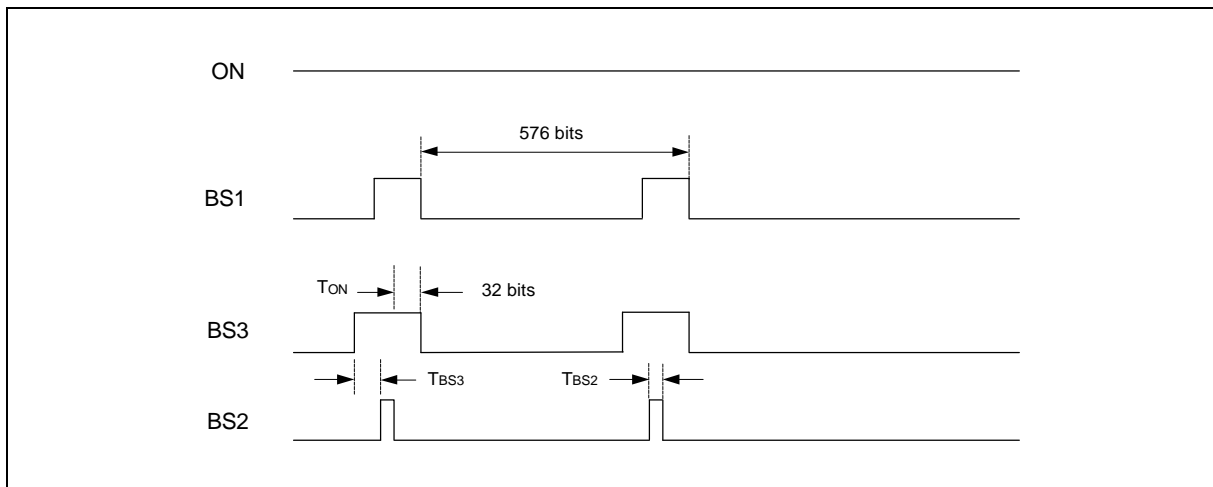


Figure 4



Lock Mode

If a synchronization codeword is detected in sync catch mode or in idle mode, then the chip enters lock mode. While in the lock mode the chip will check the addresses assigned in Txclk wait mode. If a matching address codeword appears, an ADDDT low signal will be generated and the message will be received. The message will then be sent from the RXDATA pin and the data strobe clock will be generated from RXCLK pin. The format used to send data from the RXDATA pin depends on the options Convl and Conv2.

The data consist of an output address word followed by the message words and then terminated by a termination word. The format is depicted below.

While in the lock mode, if the synchronization word is lost for a period of time, predefined by the option Outr1, Outr2, and Eoutr, the chip will return to sync catch mode.

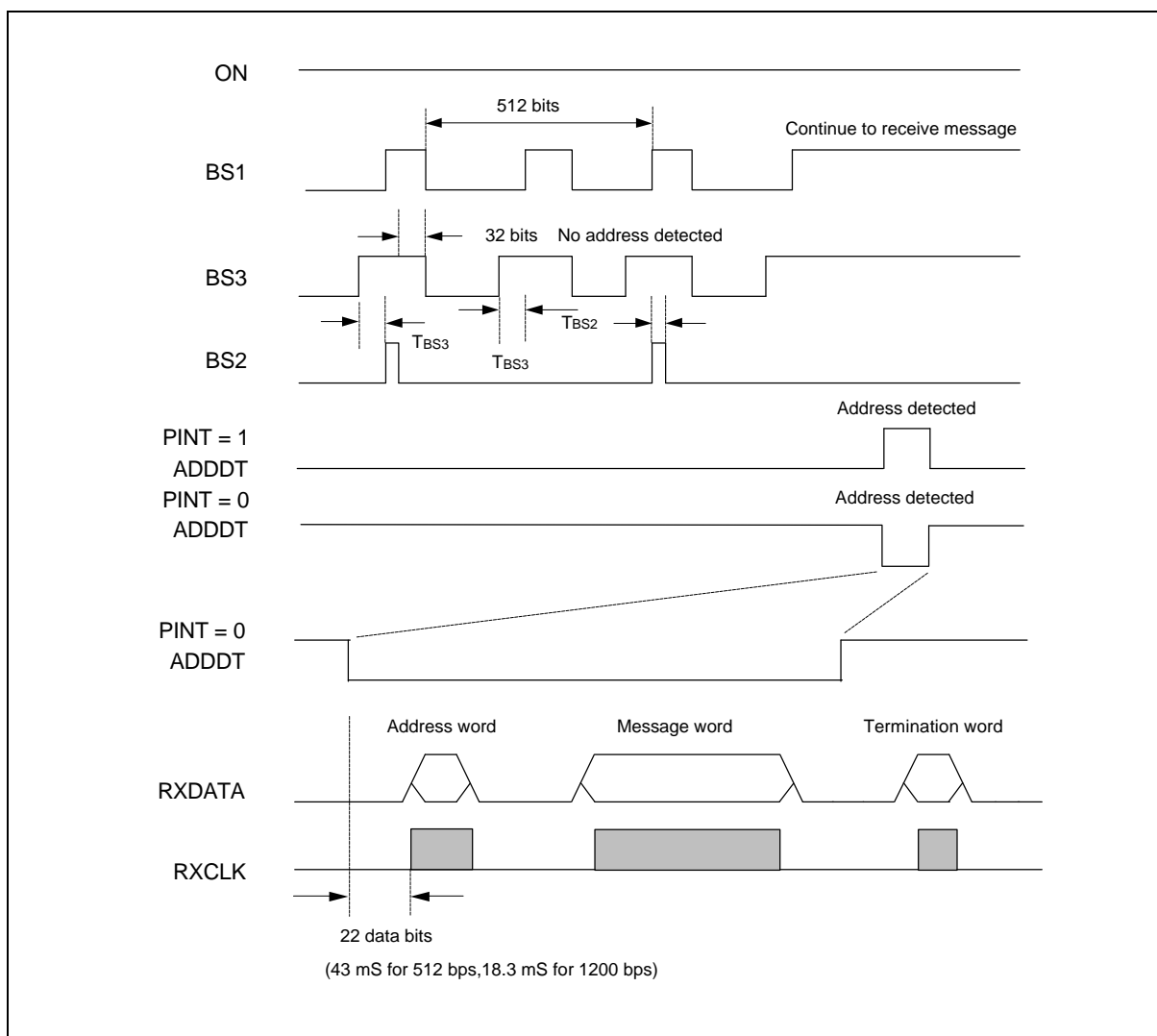


Figure 5



Reset Mode

Pulling the XRESET pin low for more than 2 mS places the W93902 in reset mode, which causes all configurations to be cleared. To release the configuration mode, let the XRESET pin return to high for 2 mS. The W93902 will then automatically enter Txclk wait mode, and so another 128 Txclk are needed. If the XRESET pin is low for more than 2 mS and the ON pin is high, the chip enters board test mode.

Board Test Mode

To place the W93902 in board test mode, set the ON pin high in reset mode. In board test mode BS1 and BS3 remain high until the ON pin returns to low. When the XRESET pin returns to high, the W93902 exits both board test mode and reset mode. Board test mode is usually used for the RF adjust function. When in board test mode, the NRZIN signal will output to FALM pin, so that we can trim the RF trimmer by buzzer frequency.

Address & Option List

CLOCK	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK	DATA
D0	NBS1	D32	NBS2	D64	NBS3	D96	EOUTR
D1	PRECTL	D33	EFOUT1	D65	TD3	D97	ERT0
D2	Rate0	D34	Rate1	D66	ERTR	D98	ERT1
D3	ADA17	D35	ADB17	D67	ADC17	D99	ADD17
D4	ADA16	D36	ADB16	D68	ADC16	D100	ADD16
D5	ADA15	D37	ADB15	D69	ADC15	D101	ADD15
D6	ADA14	D38	ADB14	D70	ADC14	D102	ADD14
D7	ADA13	D39	ADB13	D71	ADC13	D103	ADD13
D8	ADA12	D40	ADB12	D72	ADC12	D104	ADD12
D9	ADA11	D41	ADB11	D73	ADC11	D105	ADD11
D10	ADA10	D42	ADB10	D74	ADC10	D106	ADD10
D11	ADA9	D43	ADB9	D75	ADC9	D107	ADD9
D12	ADA8	D44	ADB8	D76	ADC8	D108	ADD8
D13	ADA7	D45	ADB7	D77	ADC7	D109	ADD7
D14	ADA6	D46	ADB6	D78	ADC6	D110	ADD6
D15	ADA5	D47	ADB5	D79	ADC5	D111	ADD5
D16	ADA4	D48	ADB4	D80	ADC4	D112	ADD4
D17	ADA3	D49	ADB3	D81	ADC3	D113	ADD3
D18	ADA2	D50	ADB2	D82	ADC2	D114	ADD2
D19	ADA1	D51	ADB1	D83	ADC1	D115	ADD1
D20	ADA0	D52	ADB0	D84	ADC0	D116	ADD0
D21	FA3	D53	FB3	D85	FC3	D117	FD3
D22	FA2	D54	FB2	D86	FC2	D118	FD2



Address & Option List, continuud

CLOCK	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK	DATA
D23	FA1	D55	FB1	D87	FC1	D119	FD1
D24	Freq0	D56	EnA	D88	PL1	D120	Conv1
D25	Baud0	D57	EnB	D89	PL2	D121	Conv2
D26	Inv	D58	EnC	D90	PL3	D122	Outr1
D27	EBTL	D59	EnD	D91	PL4	D123	Outr2
D28	Over	D60	Shmt	D92	MSGONE	D124	SF10
D29	Epre0	D61	Pkgsel	D93	TD1	D125	SF11
D30	Epre1	D62	Baud1	D94	TD2	D126	SF20
D31	NOPKG	D63	Extadd	D95	Pint	D127	SF21

Table 1

Option List

FUNCTION		OPTION		
Crystal	Baud rate	Freq0	Baud0	Baud1
76.8K	512 bps	1	0	0
76.8K	1200 bps	1	1	0
76.8K	2400 bps	1	X	1
32K	512 bps	0	X	X

Table 2

FUNCTION	OPTION
Address A, B, C, D	EnA, EnB, EnC, EnD
Disable	0
Enable	1

Table 3

FUNCTION	OPTION
NRZ signal	Inv
Non-inversion	0
Inversion	1

Table 4

FUNCTION	OPTION	
NRZ signal/RF cycle	Shmt	ERTR
With Schmitt trigger, RF 1/18 turn-on	1	0
Without Schmitt trigger, RF 1/18 turn-on cycle	0	X
Without Schmitt trigger, RF 1/9 turn-on	1	1

Table 5

FUNCTION	OPTION
Message reception termination condition	Over
Reception termination on first uncorrectable codeword	0
Reception termination on two uncorrectable codeword	1

Table 6

FUNCTION		OPTION	
TBS2		PL2	PL1
512 bps	1200/2400 bps		
3.90 mS	1.67 mS	0	0
11.71 mS	5.00 mS	0	1
19.53 mS	8.33 mS	1	0
27.34 mS	11.67 mS	1	1

Table 7

Note: PLL pre-on time = TBS2 + TBS3, RF pre-on time = TBS2

FUNCTION		OPTION	
TBS3		PL4	PL3
512 bps	1200/2400 bps		
0.00 mS	0.00 mS	0	0
31.25 mS	13.33 mS	0	1
62.50 mS	26.67 mS	1	0
93.75 mS	40.00 mS	1	1

Table 8



Option List NBS1/NBS2/NBS3 Setting

When NBS1 = 0, NBS2 = 0, and NBS3 = 0, the timing is as follows:

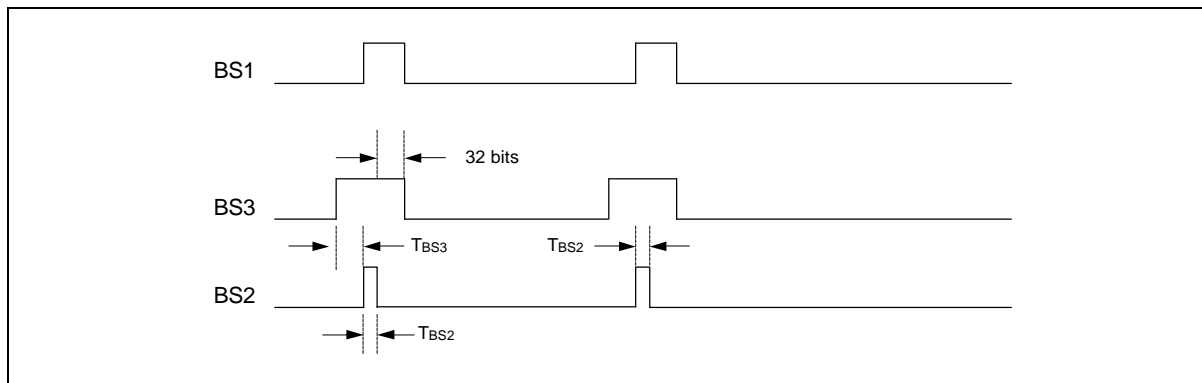


Figure 6

When NBS1 = 1, NBS2 = 1, and NBS3 = 1, the timing is as follows:

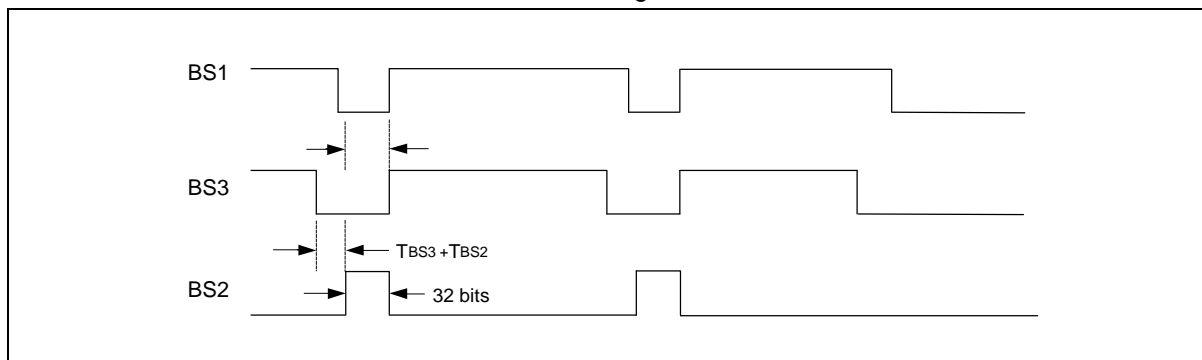


Figure 7

If the BS1 pin is used to turn RF on, then the pre-on time for RF is equal to T_{BS2} (max.11.67 mS). If the BS3 pin is used to turn RF on, then the pre-on time will be equal to $T_{BS2} + T_{BS3}$ (max.51.67 mS). The BS3 pin can also be used to turn on the PLL circuit.

FUNCTION	OPTION		
Sync retry times	TD1	TD2	TD3
1	0	0	1
3	1	0	1
5	0	1	1
7	1	1	1
9	0	0	0
11	1	0	0
13	0	1	0
15	1	1	0

Table 9

FUNCTION		OPTION		
Out-of-range hold time when synchronization is lost		OUTR1	OUTR2	EOUTR
512 bps	1200/2400 bps			
36 sec	31 sec	0	0	0
72 sec	61 sec	0	1	0
144 sec	123 sec	1	0	0
288 sec	246 sec	1	1	0
0 sec	0 sec	X	X	1

Table 10

FUNCTION	OPTION
Preamble recognition	PRECTL
8 bit	0
6 bit	1

Table 11

FUNCTION	OPTION	
Preamble search delay	Epre1	Epre0
512 bit	0	0
896 bit	0	1
1024 bit	1	0
1792 bit	1	1

Table 12

Error correction method option list:

FUNCTION	OPTION	
Correction Method	ERT1	ERT0
Two-bit random	0	0
Four-bit burst + Two-bit random	0	1
Four-bit burst	1	0
One bit	1	1

Table 13

Note: When option MSGONE = 0, the error correction methods of address and message all follow the above setting, If MSGONE = 1, the error correction method follows the setting when receiving the address word. The message receiving method is always one-bit error correction, however.



Error Message, for one-bit random, two-bit random, or four-bit burst error correction method:

ONE-BIT/TWO-BIT RANDOM/4-BIT BURST ERROR CORRECTION METHOD							
Before Correction	After Correction	Parity Error	4-bit Package and ERTR = 1				7/8-bit Package
			ER0	ER1	ER2	ER3	Error flag
No error	-	No error	0	0	1	0	0
No error	-	Error	1	0	1	0	0
Error	No error	No error	0	1	1	0	0
Error	No error	Error	1	1	1	0	1
Error	Error	No error	0	1	1	1	1
Error	Error	Error	1	1	1	1	1

Table 14

Notes:

1. When ERTR = 0, in the 4-bit package ER0 = 0, ER1 = 1, ER2 = 1, ER3 = Error flag.
2. If 3-bit random errors (or more than three) are detected or five (or more) burst errors are detected, no error correction method will be activated and ER0 to ER3 will be set or the error flag will be set directly.

Error message, for two-bit random plus four-bit burst error correction method

TWO-BIT RANDOM WITH 4-BIT BURST ERROR CORRECTION METHOD										
Detect Random		Detect Burst		Parity Error	Random/Burst	4-bit Package and ERTR = 1				7/8-bit Package
Before Correction	After Correction	Before Correction	After Correction			ER0	ER1	ER2	ER3	Error Flag
No error	-	No error	-	No error	Original	0	0	0	0	0
No error	-	No error	-	Error	Original	1	0	0	0	0
Error	No error	Error	No error	No error	Burst	0	1	0	0	0
Error	No error	Error	No error	Error	Burst	1	1	0	0	1
Error	Error	Error	Error	No error	Random	0	1	1	1	1
Error	Error	Error	Error	Error	Random	1	1	1	1	1
Error	Error	Error	No error	No error	Burst	0	1	0	1	1
Error	Error	Error	No error	Error	Burst	1	1	0	1	1
Error	No error	Error	Error	No error	Random	0	1	1	0	1
Error	No error	Error	Error	Error	Random	1	1	1	0	1

Table 15

Notes:

1. When ERTR = 0, in the 4-bit package ER0 = 0, ER1 = 1, ER2 = 1, ER3 = Error flag.
2. If 3-bit random errors (or more than three) are detected or five (or more) burst errors are detected, no error correction method will be activated and the display mode will be set as mode F.

Note: When ERTR = 0, in the 4-bit package ER0 = 0, ER1 = 1, ER2 = 1, ER3 = Error flag.

*Generally, ER0 represents the parity error and ER1 represents the error condition before correction. ER2 represents the burst error correction result and ER3 represents the random error correction result.

Data Transfer Timing

While the chip detects the proper address in the lock mode, the chip will send the message to the uC from RXDATA pin as shown in figure 5. The detailed timing is depicted below.

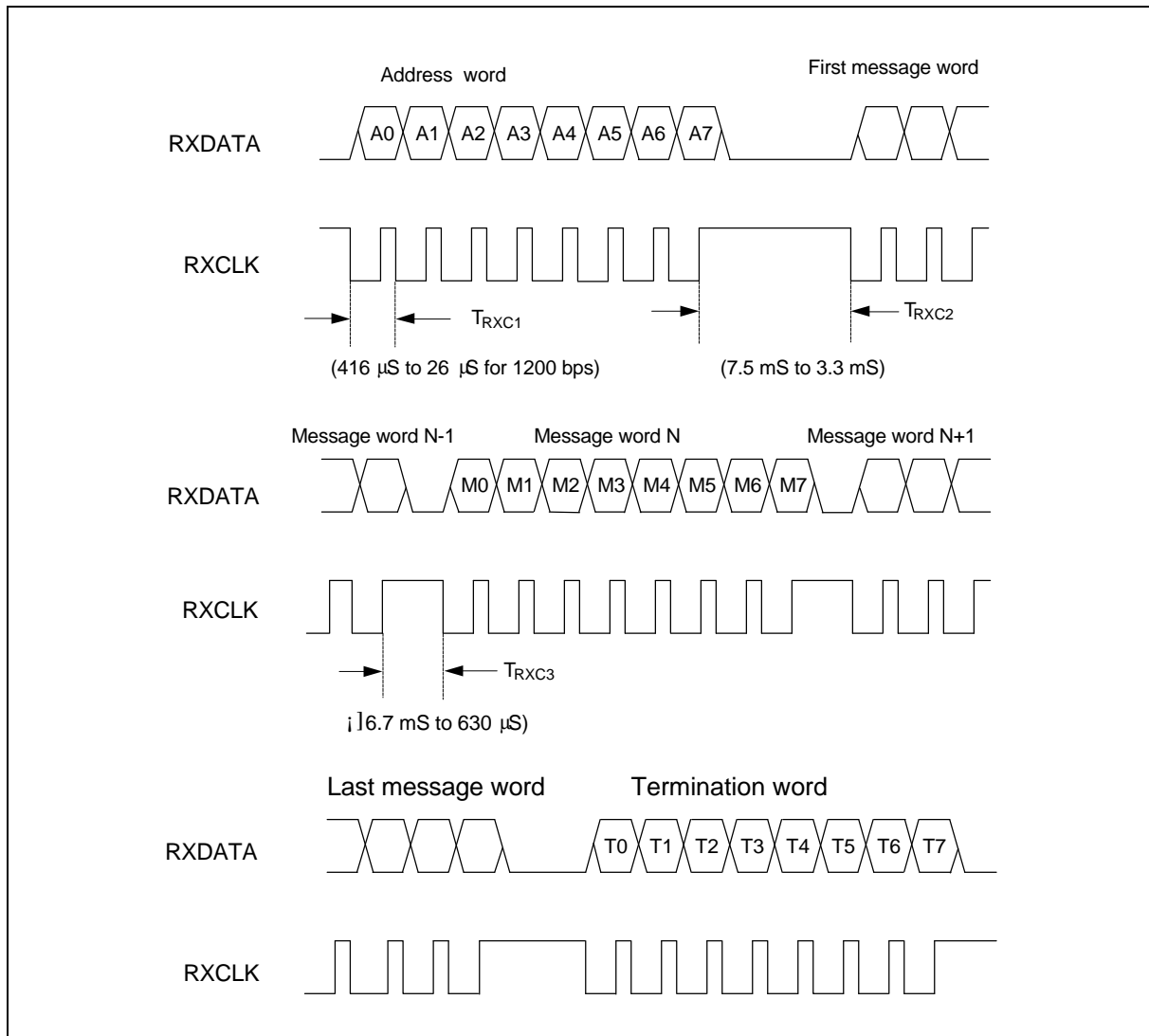


Figure 8

Note: The timing of TRXC1, TRXC2, and TRXC3 depends on the setting of Rate1 and Rate0.



RXCLK and RXDATA transmission rate option list:

FUNCTION	OPTION	
RXCLK rate (TRXC1)	Rate1	Rate0
2* data rate	0	0
8* data rate	0	1
16* data rate	1	0
32* data rate	1	1

Table 16

Address Word Format

FUNCTION CODE		CALL ADDRESS			CHECK BITS			ERROR BIT
Bit 0	Bit 1	Bit 2	Bit 3	Address	Bit 4	Bit 5	Bit 6	Bit 7
Bit 21 of address word	Bit 20 of address word	0	0	A	RA0	RA1	RA2	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 17

Notes:

1. If ERTR = 1, then RA0 indicates a parity error, RA1 indicates the error condition before correction, and RA2 indicates whether the address has been corrected. For example, if (RA0, RA1, RA2) = (0, 1, 0), then the codeword has no parity error, there is an error before error correction, but no error is found after correction.
2. The error bit for address code is set when this code matches the address assigned in the setting but is not correctable.

FUNCTION	OPTION
Package Method	NOPKG
With Package(4 / 7 / 8 bit format)	0
Without Package	1

Table 18

Note: When NOPKG = 1, 24 bits will be transferred to the CPU from the decoder and divided into three groups of eight bits. When NOPKG = 0, five groups of eight bits are transferred.

Message Word Format, NOPKG = 0

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Package
Message bits						Error flag (note)		7/8 bit
Message bits			ER0	ER1	ER2	ER3	4 bit	

Table 19

Note: Error flag = 1 indicates that an error condition has occurred.



Message Word Format, NOPKG = 1

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
M0	M1	M2	M3	M4	M5	M6	M7

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
M8	M9	M10	M11	M12	M13	M14	M15

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
M16	M17	M18	M19	ER0	ER1	ER2	ER3

Table 20

Termination Word format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	1	0	0	0	0	Error flag

Table 21

Note: If the alphanumeric format option is selected, then the termination words will be seven bits of zeros with error flag followed by the upper termination word. That is, when this option is selected, the ASCII format "04" (EOT) will be sent.

FUNCTION	OPTION
ADDDT polarity	Pint
Active low	0
Active high	1

Table 22

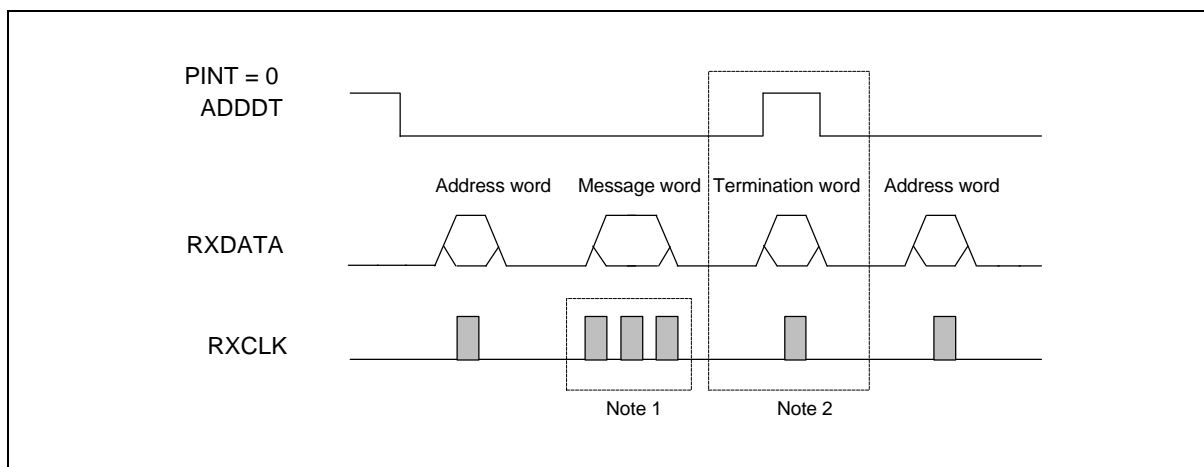


Figure 9

Note: When ERTR = 0, the ADDDT pin will remain low while addresses continue to be detected. When ERTR = 1, a high low pulse will be generated and addresses will continue to be received. If NOPKG = 1, a termination word will not be generated.



Data Format Options

The W93902 automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on the setting of Conv1, Conv2, PKGSEL, and the function bits in the received address codeword, conversion takes place as shown in Table 23.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks seven bits in length. After the error flag is added, the message blocks are transferred as message words. In this option, one message word may exceed two codewords in length.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks four bits in length, as shown in Table 24. After the error flag is added, the blocks are transferred as message words.

When a conversion from numeric format to 4-bit package takes place, the received message codewords are split into blocks four bits in length, as shown in Table 25. After the error status bits ER0 to ER3 are added, the blocks are transferred as message words.

When no conversion takes place, the received message codewords are split into blocks eight bits in length. The last four bits are combined with the error status bits ER0 to ER3, and then the blocks are transferred as message words.

Data Format Options

PKGSEL = 0

DATA FORMAT	OPTION	
	Conv1	Conv2
Txdata output data format		
Numeric 4-bit format	0	0
Numeric 8-bit format	0	1
Alphanumeric 7-bit format	1	0
Numeric/Alphanumeric format depends on function bits	1	1

Conv1 = 1, Conv2 = 1, PKGSEL = 0

DATA FORMAT	FUNCTION BIT	
	Bit 21	Bit 20
Txdata output data format		
Numeric 8-bit format	0	0
Alphanumeric 7-bit format	0	1
Alphanumeric 7-bit format	1	0
Alphanumeric 7-bit format	1	1

PKGSEL = 1

DATA FORMAT	OPTION	
Txdata output data format	Conv1	Conv2
Numeric 8-bit format	0	0
Alphanumeric 7-bit format	0	1
Alphanumeric 7-bit format	1	0
Alphanumeric 7-bit format	1	1

Table 23

Numeric 8-bit Format

INPUT DATA				CHARACTER	OUTPUT DATA							
Bit0	Bit1	Bit2	Bit3		Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
0	0	0	0	"0"	0	0	0	0	1	1	0	Error flag
1	0	0	0	"1"	1	0	0	0	1	1	0	"
0	1	0	0	"2"	0	1	0	0	1	1	0	"
1	1	0	0	"3"	1	1	0	0	1	1	0	"
0	0	1	0	"4"	0	0	1	0	1	1	0	"
1	0	1	0	"5"	1	0	1	0	1	1	0	"
0	1	1	0	"6"	0	1	1	0	1	1	0	"
1	1	1	0	"7"	1	1	1	0	1	1	0	"
0	0	0	1	"8"	0	0	0	1	1	1	0	"
1	0	0	1	"9"	1	0	0	1	1	1	0	"
0	1	0	1	"*"	0	1	0	1	0	1	0	"
1	1	0	1	"U"	1	0	1	0	1	0	1	"
0	0	1	1	" "	0	0	0	0	0	1	0	"
1	0	1	1	"-"	1	0	1	1	0	1	0	"
0	1	1	1	"j"	1	0	1	1	1	0	1	"
1	1	1	1	"i"	1	1	0	1	1	0	1	"

Table 24

Numeric 4-bit Format

INPUT DATA				CHARACTER	OUTPUT DATA							
Bit0	Bit1	Bit2	Bit3		Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
0	0	0	0	"0"	0	0	0	0	0	1	1	Error flag
1	0	0	0	"1"	1	0	0	0	0	1	1	"
0	1	0	0	"2"	0	1	0	0	0	1	1	"
1	1	0	0	"3"	1	1	0	0	0	1	1	"
0	0	1	0	"4"	0	0	1	0	0	1	1	"
1	0	1	0	"5"	1	0	1	0	0	1	1	"
0	1	1	0	"6"	0	1	1	0	0	1	1	"
1	1	1	0	"7"	1	1	1	0	0	1	1	"
0	0	0	1	"8"	0	0	0	1	0	1	1	"
1	0	0	1	"9"	1	0	0	1	0	1	1	"
0	1	0	1	"*"	0	1	0	1	0	1	1	"
1	1	0	1	"U"	1	1	0	1	0	1	1	"
0	0	1	1	" "	0	0	1	1	0	1	1	"
1	0	1	1	"-"	1	0	1	1	0	1	1	"
0	1	1	1	"j"	0	1	1	1	0	1	1	"
1	1	1	1	"i"	1	1	1	1	0	1	1	"

Table 25

Note: When ERTR = 1, then Bit4 = ER0, Bit5 = ER1, Bit6 = ER2, and Bit7 = ER3.

Frequency output option list:

FUNCTION	OPTION
FOUT1 output	EFOUT1
Output enable	0
Output disable	1

Table 26

Note: If FOUT1 is not used, the option EFOUT1 should be set to 1.

FUNCTION	OPTION	
FOUT1 output	SF11	SF10
32768 Hz	0	0
64 Hz	0	1
16 Hz	1	0
1/60 Hz	1	1

Table 27

FOUT2 will output frequency when EFOUT2 is high:

FUNCTION	OPTION	
FOUT2 output	SF21	SF20
16 KHz(32768Hz crystal)/19 KHz (76800Hz)	0	0
64 Hz	0	1
16 Hz	1	0
1/60 Hz	1	1

Table 28

Note: When FOUT1 and FOUT2 are assigned the same frequency, they will have a different phase.

Buzzer output operation (FBUZ1 and FBUZ2 normally pulled high):

FUNCTION	PIN	
FALM output	FBUZ2	FBUZ1
2 KHz	low	low
4 KHz	low	high
3.2 KHz	high	low
2.7 KHz	high	high

Table 29

Notes:

- 1.The frequency of FLAM output is controled by the voltage of FBUZ1 and FBUZ2 pin.
2. FBUZ2 is active only when EBTL = 1. If use the battery low detection function (EBTL = 0), the FBUZ2 is internally pull high and FALM can only output 2.7 KHz or 3.2 KHz.

Battery low detection circuit enable options:

FUNCTION	OPTION
FBUZ2/BTLIN	EBTL
BTLIN	0
FBUZ2	1

Table 30

The battery low detect function samples the BTLIN pin (when EBTL = 0) each time BS1 is active. If the level of this pin is detected to be high four times in a row, then a high signal will be output through the BTLDT pin, until the BTLIN pin is detected to be low four times in a row.

Buzzer, LED, and Timer Reference Clock Output

The W93902 provides an AI pin to enable the FALM pin output and frequency selection through the FBUZ1 and FBUZ2 pins, as shown in Table 29. When AI is low, FALM is at high impedance. When AI is high, FALM outputs the specified frequency with an N-channel open drain MOS architecture. FALM should be connected to an external pull-up resistor in normal usage, so that the power consumption can be controlled when the buzzer is active.



FOUT2 output control is similar, but the output stage is slightly different. When EFOUT2 is high, the FOUT2 output clock is selected by the SF20 and SF21 bits, as shown in Table 28. When EFOUT2 is low, FOUT2 provides a high-level dc output. Its output stage is a complementary CMOS output. It is not necessary to connect a pull-up resistor.

The W93902 also supports a 32768 Hz real-time clock reference output, which is active after the Txclk Wait Mode. When this clock output is not needed, the EFOUT1 bit should be set to 1.

FOUT1 and FOUT2 also provide a complementary clock output of 64 Hz, 16 Hz, or 1/60 Hz for use as a reference timer.

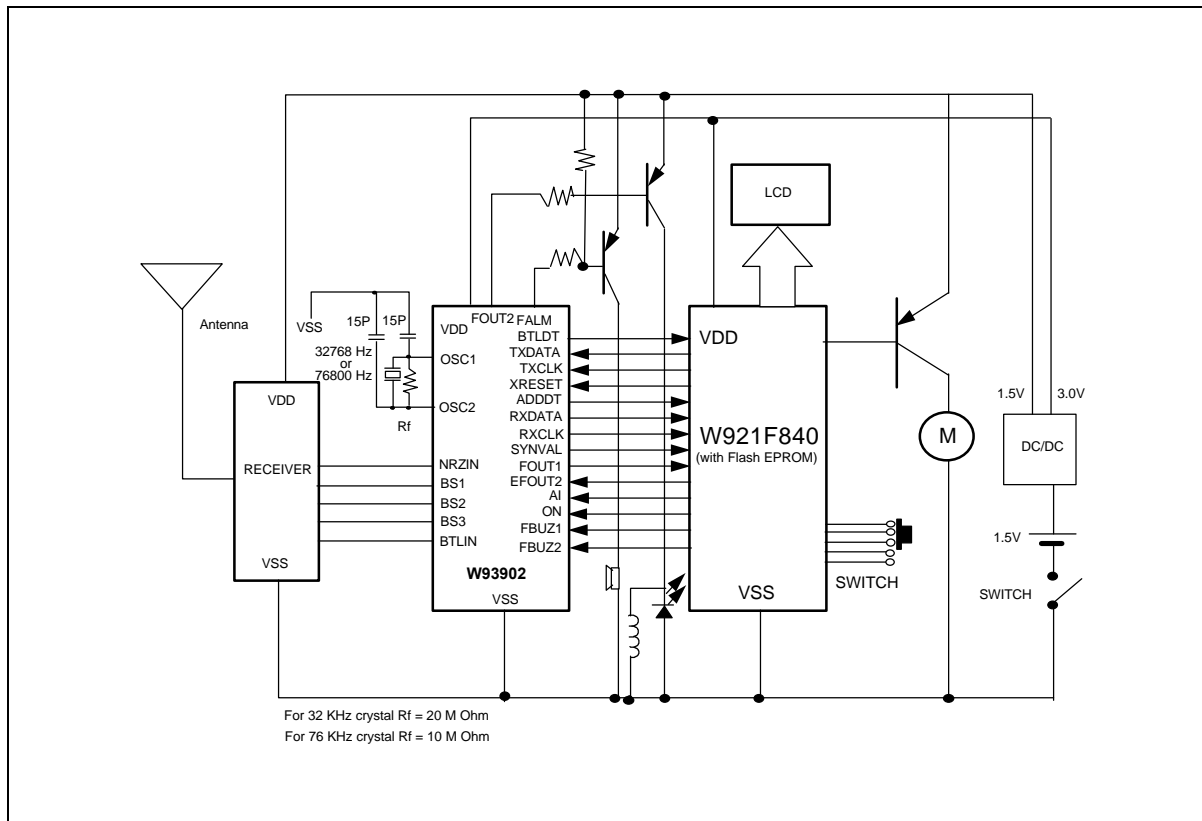
Option EXTADD is used for proprietary algorithm. For normal operation, EXTADD should be set to 0.

DC CHARACTERISTICS

SYM.	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
Supply						
VDD	Supply voltage		2.5	3.0	5.0	V
ISS	Supply current	VDD = 3 osc = 32 KHz		20	40	μA
		VDD = 3 osc = 76.8 KHz		25	45	μA
Input						
VIH	High-level input voltage NRZIN, TXCLK, TXDATA, ON, XRESET, EFOUT2, AI, FBUZ1, FBUZ2		0.8			VDD
VIL	Low-level input voltage NRZIN, TXCLK, TXDATA, ON, XRESET, EFOUT2, AI, FBUZ1, FBUZ2				0.2	VDD
IIL	Low-level input current XRESET, FBUZ1, FBUZ2	VDD = 3V, VIN = 0V			10.0	μA
IIH	High-level input current. AI, EFOUT2	VDD = 3V, VIN = 3V			10.0	μA
IOL	Low-level output current BS1, BS2, BS3, ADDDT, RXDATA, RXCLK, SYNVAL, FOUT1, FOUT2	VDD = 2.7V, VOUT = 1.35V		7.34		mA
IOL	Low-level sink current. FALM	VDD = 2.7V, VOUT = 1.35V		14.68		mA
IOH	High-level output current BS1, BS2, BS3, ADDDT RXDATA, RXCLK SYNVAL, FOUT1, FOUT2	VDD = 2.7V, VOUT = 1.35V		3.52		mA



TYPICAL APPLICATION CIRCUIT



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Note: All data and specifications are subject to change without notice.