To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

7470/7471 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7470/7471 group is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 32-pin shrink plastic molded DIP. The M37471M2-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 42-pin shrink plastic molded DIP or a 56-pin plastic molded QFP.

These single-chip microcomputer are useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming .

The differences between the M37471M2-XXXSP and the M37471M2-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

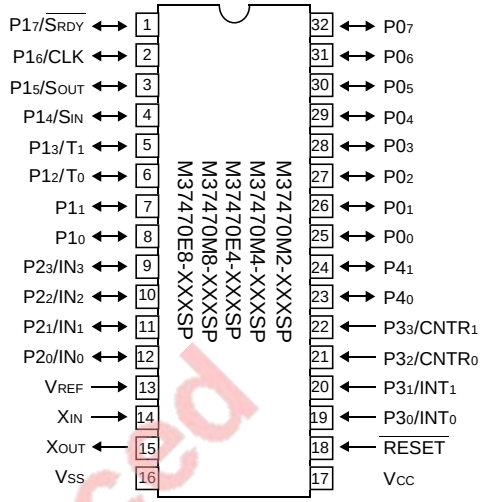
The differences among M37470M2-XXXSP, M37470M4-XXXSP, M37470M8-XXXSP, M37471M2-XXXSP/FP, M37471M4-XXXSP/FP and M37471M8-XXXSP/FP are noted below.

Type name	ROM size	RAM size	I/O ports
M37470M2-XXXSP	4096 bytes	128 bytes	26
M37471M2-XXXSP/FP			36
M37470M4-XXXSP	8192 bytes	192 bytes	26
M37471M4-XXXSP/FP			36
M37470M8-XXXSP	16384 bytes	384 bytes	26
M37471M8-XXXSP/FP			36

FEATURES

- Basic machine-language instructions 71
- Memory size
  - ROM ..... 4096 bytes (M37471M2)
  - RAM ..... 128 bytes (M37471M2)
- The minimum instruction execution time
  - ..... 0.5 µs (at 8 MHz oscillation frequency)
- Power source voltage
  - ..... 2.7 to 4.5 V (at 2.2Vcc–2.0 MHz oscillation frequency)
  - ..... 4.5 to 5.5 V (at 8 MHz oscillation frequency)
- Power dissipation in normal mode
  - ..... 35 mW (at 8.0 MHz oscillation frequency)
- Subroutine nesting ..... 64 levels max. (M37470M2, M37471M2)
- Interrupt ..... 12 sources, 10 vectors
- 8-bit timers 4
- Programmable I/O ports
  - (Ports P0, P1, P2, P4) ..... 22(7470 group)
  - 28(7471 group)
- Input port (Port P3) ..... 4(7470 group)
  - (Ports P3, P5) ..... 8(7471 group)
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit, 4channels (7470 group)
  - 8-bit, 8channels (7471 group)

PIN CONFIGURATION (TOP VIEW)

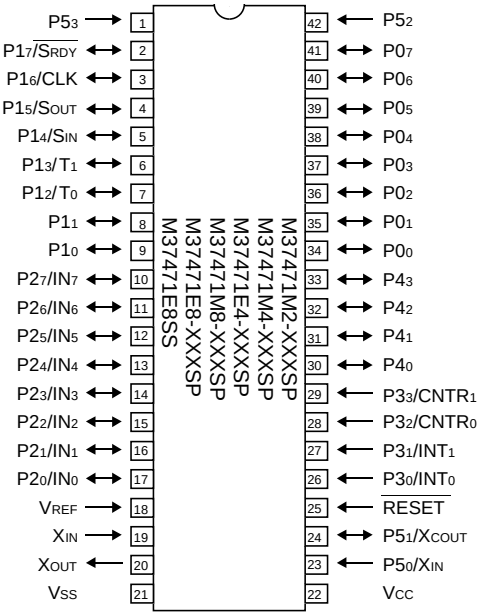


Outline 32P4B

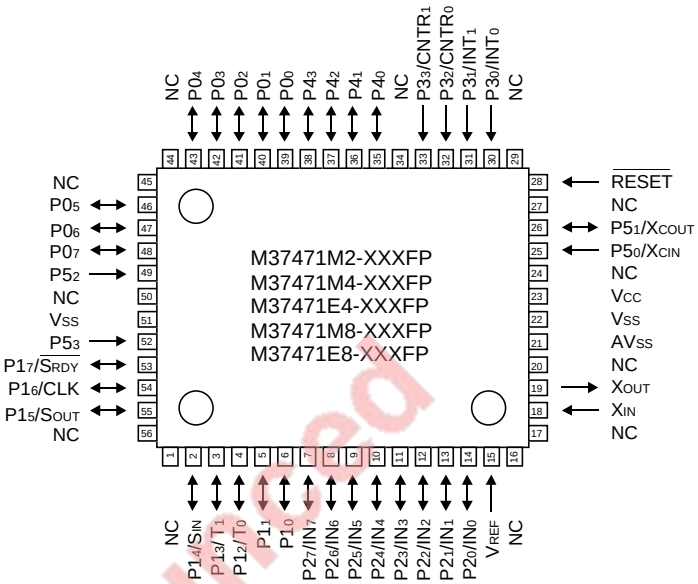
APPLICATION

Audio-visual equipment, VCR, Tuner,
Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 42P4B
42S1B-A (Window)

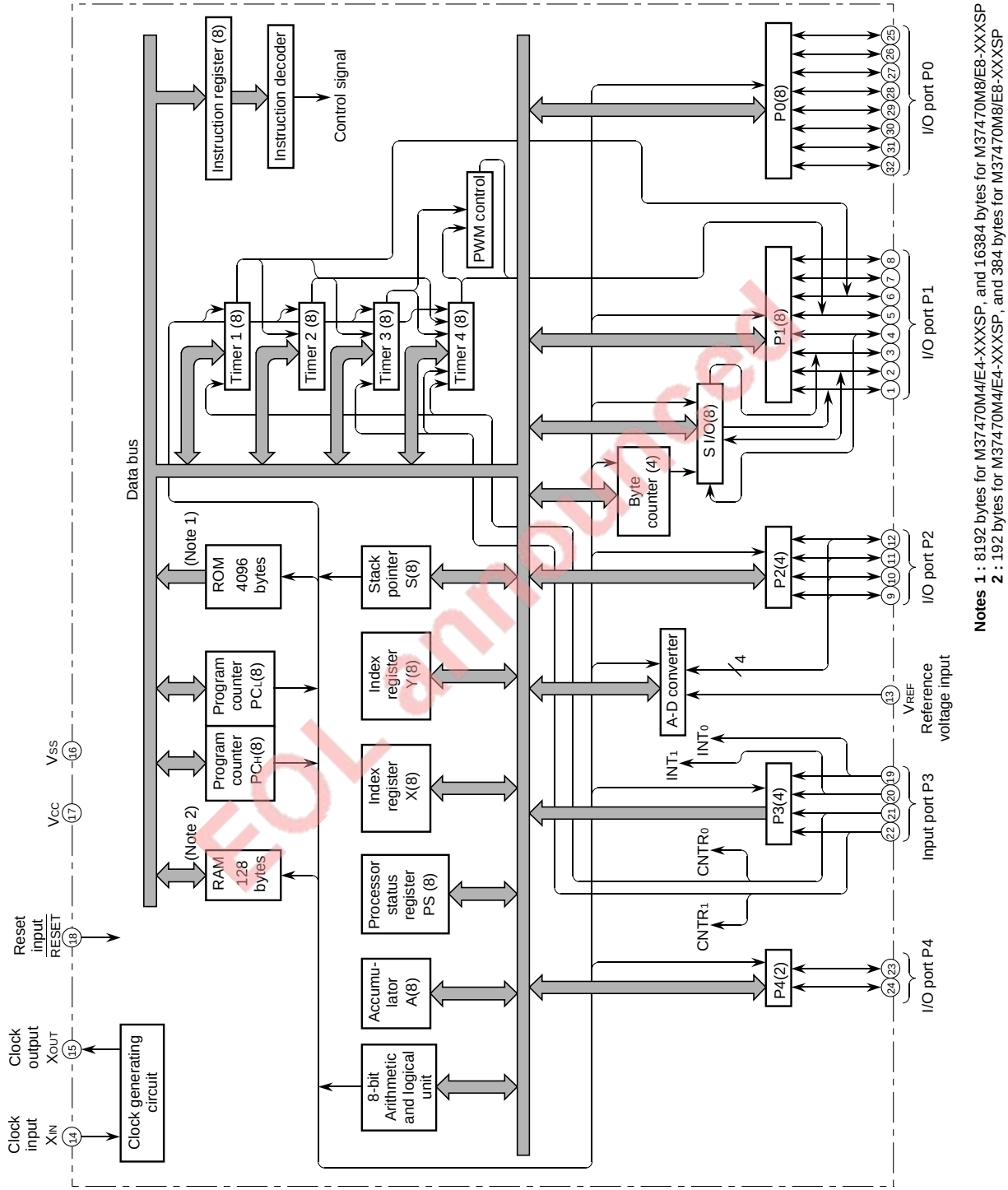


Outline 56P6N-A

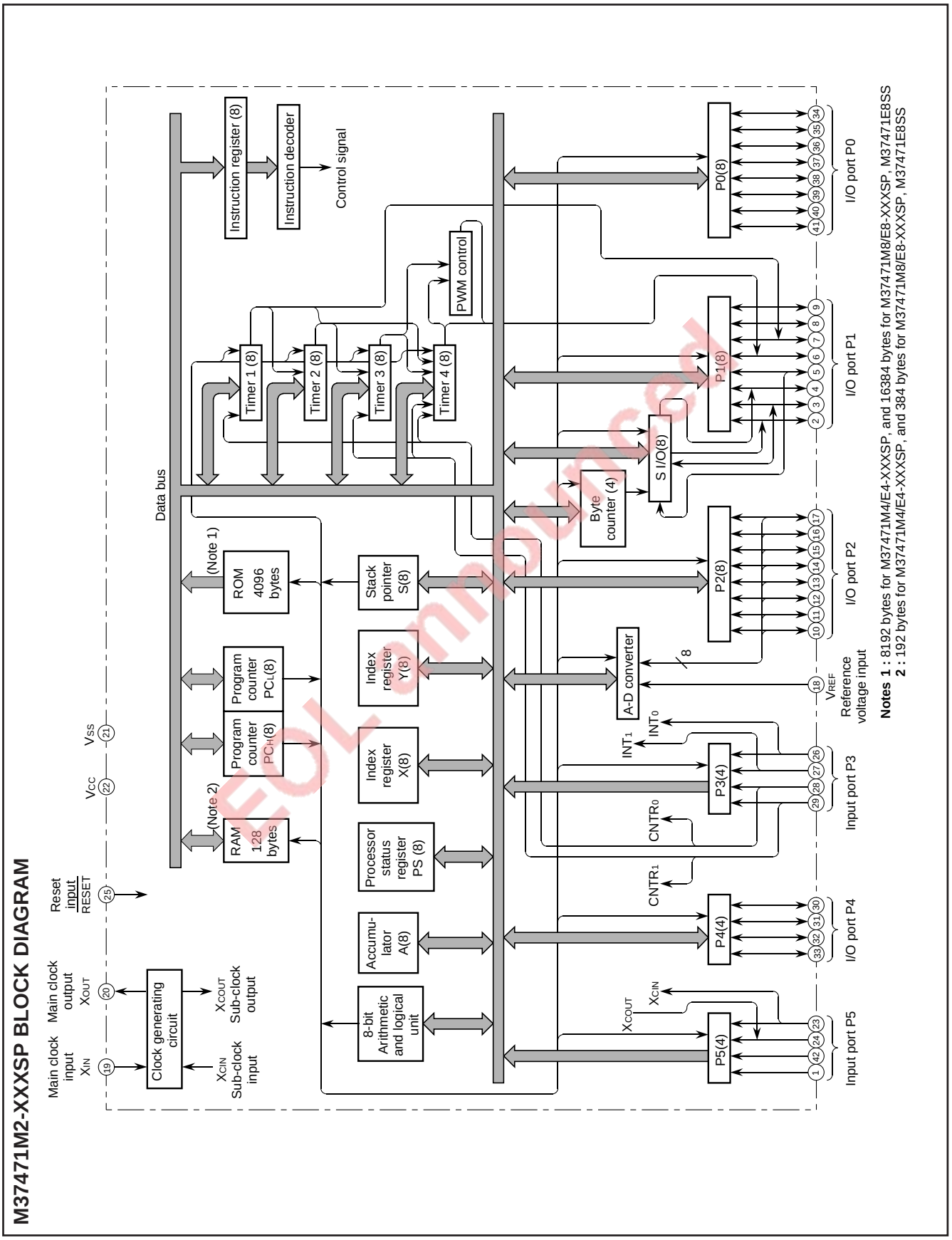
Note : The differences between 42P4B package type of 7471 group and 56P6N-A package type of 7471 group are package outline, power dissipation ability (absolute maximum ratings), and the provision of an AVSS pin by the 56P6N-A package type.

NC : No connection

M37470M2-XXXSP BLOCK DIAGRAM



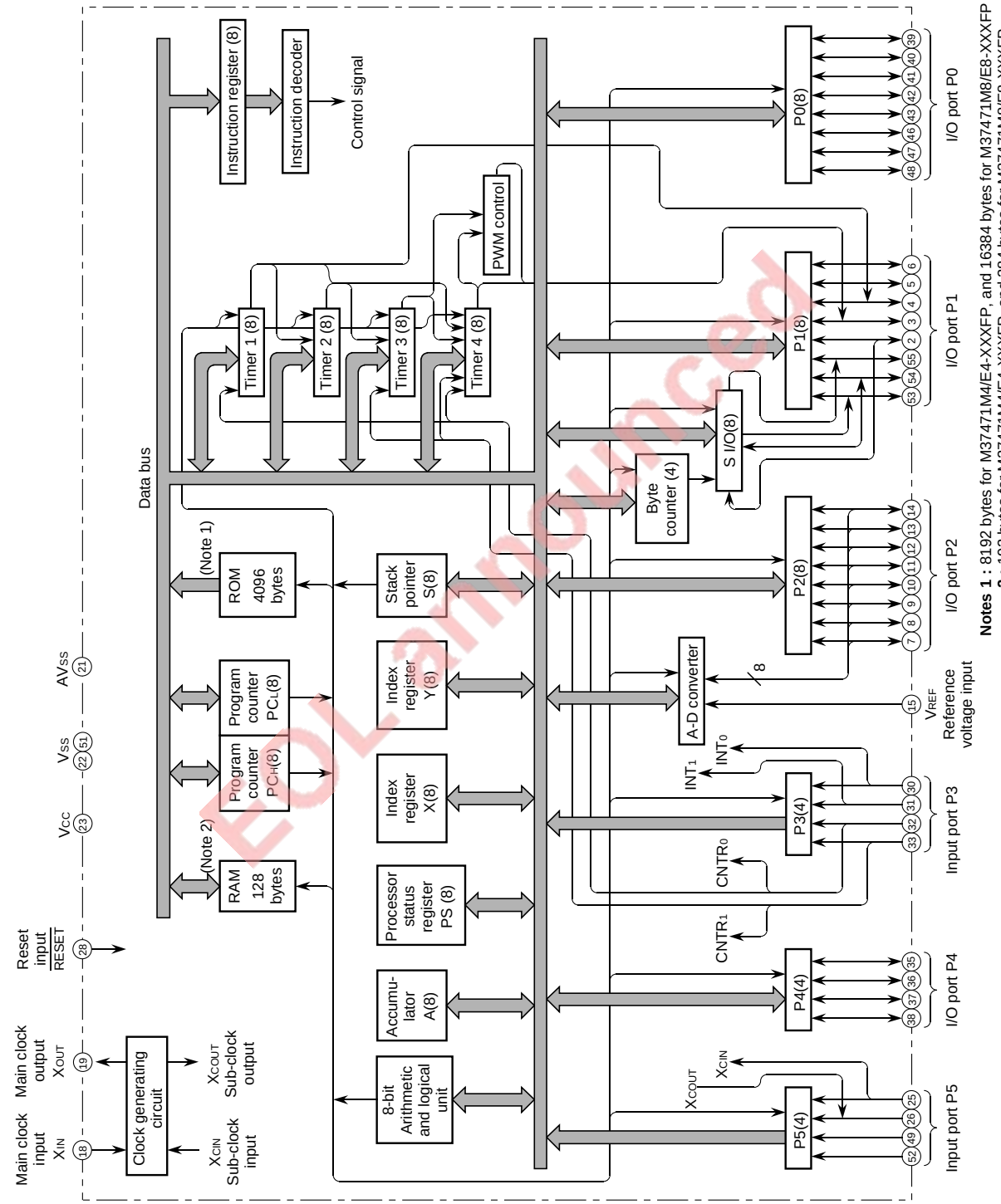
M37471M2-XXXSP BLOCK DIAGRAM



Notes 1 : 8192 bytes for M37471M4/E4-XXXSP, and 16384 bytes for M37471M8/E8-XXXSP, M37471E8SS
2 : 192 bytes for M37471M4/E4-XXXSP, and 384 bytes for M37471M8/E8-XXXSP, M37471E8SS

RENESAS
Renesas Technology Corp.

M37471M2-XXXFP BLOCK DIAGRAM



Notes 1 : 8192 bytes for M37471M4/E4-XXXFP, and 16384 bytes for M37471M8/E8-XXXFP
2 : 192 bytes for M37471M4/E4-XXXFP, and 384 bytes for M37471M8/E8-XXXFP

FUNCTIONS OF 7470/7471 GROUP

Parameter			Functions
Basic machine-language instructions			71
Instruction execution time			0.5 μs (the minimum instructions, at 8 MHz oscillation frequency)
Clock input oscillation frequency			8 MHz (max.)
Memory size	M37470M2	ROM	4096 bytes
	M37471M2	RAM	128 bytes
	M37470M4/E4	ROM	8192 bytes
	M37471M4/E4	RAM	192 bytes
	M37470M8/E8	ROM	16384 bytes
	M37471M8/E8	RAM	384 bytes
Input/Output port	P0, P1	I/O	8-bit × 2
	P2	I/O	8-bit × 1 (4-bit × 1 for 7470 group)
	P3, P5	Input	4-bit × 2 (Port P5 is not included in 7470 group)
	P4	I/O	4-bit × 1 (2-bit × 1 for 7470 group)
Serial I/O			8-bit × 1
Timers			8-bit timer × 4
A-D converter			8-bit × 1 (8 channels) (8-bit × 1 (4 channels) for M37470M2/M4/M8)
Subroutine nesting			64 level max. (M37470M2, M37471M2)
			96 level max. (M37470M4/E4, M37471M4/E4)
			192 level max. (M37470M8/E8, M37471M8/E8)
Interrupt			5 external interrupts, 6 internal interrupts, 1 software interrupt
Clock generating circuit			Built-in circuit with internal feedback resistor (a ceramic or a quartz-crystal oscillator)
Power source voltage			2.7 to 4.5 V (at 2.2Vcc–2.0 MHz oscillation frequency), 4.5 to 5.5 V (at 8 MHz oscillation frequency)
Power dissipation			35 mW (at 8 MHz oscillation frequency)
Input/Output characters	Input/Output voltage		5 V
	Output current		–5 to 10 mA (P0, P1, P2, P4 : CMOS tri-states)
Operating temperature range			–20 to 85°C
Device structure			CMOS silicon gate
Package	M37470M2/M4/M8/E4/E8-XXXSP		32-pin shrink plastic molded DIP
	M37471M2/M4/M8/E4/E8-XXXSP		42-pin shrink plastic molded DIP
	M37471M2/M4/M8/E4/E8-XXXFP		56-pin plastic molded QFP
	M37471E8SS		42-pin ceramic DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Power source voltage		Apply voltage of 2.7 to 5.5 V to V_{CC}, and 0 V to V_{SS}.
AV_{SS} (Note 1)	Analog power source		Ground level input pin for A-D converter. Same voltage as V_{SS} is applied.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at "L" for 2 µs or more (under normal V_{CC} conditions).
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz-crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open. Feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
V_{REF}	Reference voltage input	Input	Reference voltage input pin for the A-D converter.
$P0_0$–$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided.
$P1_0$–$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. $P1_2$, $P1_3$ are in common with timer output pins $\overline{T_0}$, $\overline{T_1}$, $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively. The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output.
$P2_0$–$P2_7$ (Note 2)	I/O port P2	I/O	Port P2 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. This port is in common with analog input pins IN_0–IN_7.
$P3_0$–$P3_3$	Input port P3	Input	Port P3 is a 4-bit input port. $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1, and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$.
$P4_0$–$P4_3$ (Note 3)	I/O port P4	I/O	Port P4 is a 4-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.
$P5_0$–$P5_3$ (Note 4)	Input port P5	Input	Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz-crystal oscillator between X_{CIN} and X_{COUT}. If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin. Feedback resistor is connected between X_{CIN} and X_{COUT} pins.

Notes 1 : AV_{SS} for M37471M2/M4/M8/E4/E8-XXXFP.
2 : Only $P2_0$–$P2_3$ (IN_0–IN_3) 4-bit for 7470 group.
3 : Only $P4_0$ and $P4_1$ 2-bit for 7470 group.
4 : This port is not included in 7470 group.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 7470/7471 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The MUL, DIV, WIT, and STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address 00FB16. This register contains the stack page selection bit.

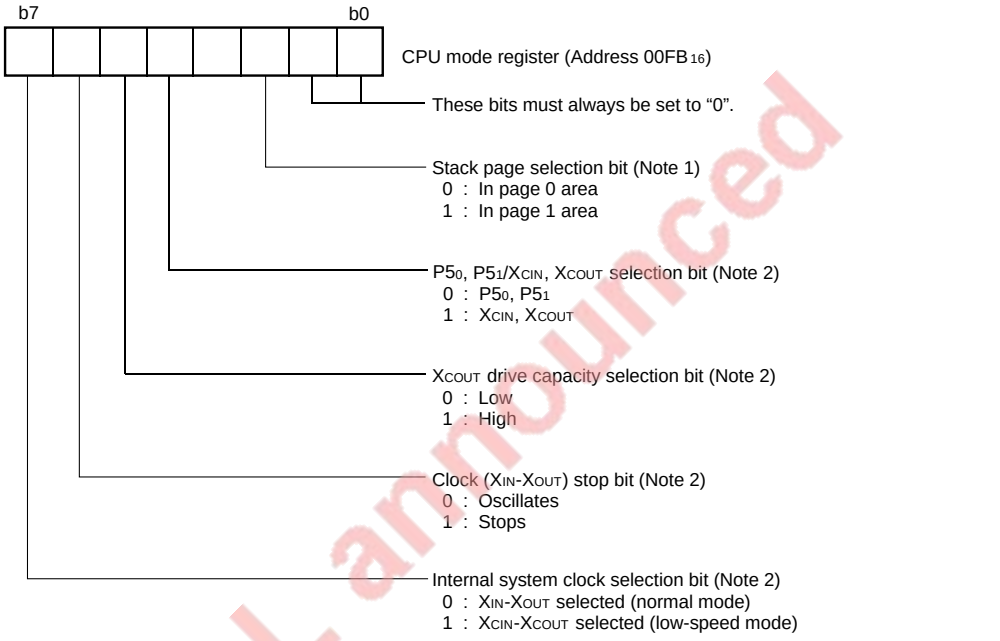


Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**
  The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.
- **RAM**
  RAM is used for data storage as well as a stack area.
- **ROM**
  ROM is used for storing user programs as well as the interrupt vector area.
- **Interrupt Vector Area**
  The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.
- **Zero Page**
  Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.
- **Special Page**
  Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

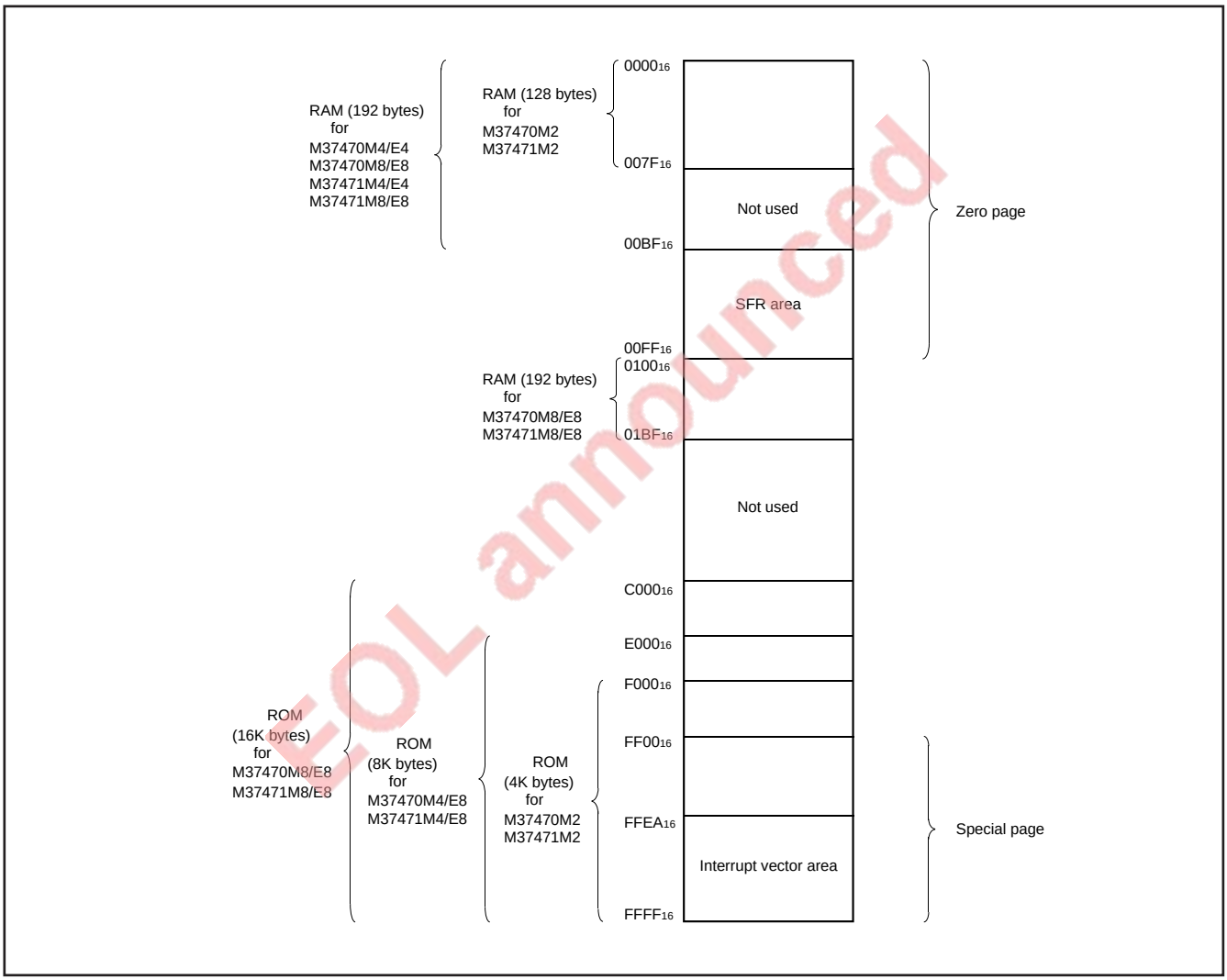


Fig. 2 Memory map

00C0₁₆	Port P0
00C1₁₆	Port P0 direction register
00C2₁₆	Port P1
00C3₁₆	Port P1 direction register
00C4₁₆	Port P2
00C5₁₆	Port P2 direction register
00C6₁₆	Port P3
00C7₁₆	
00C8₁₆	Port P4
00C9₁₆	Port P4 direction register
00CA₁₆	Port P5 (Note 1)
00CB₁₆	
00CC₁₆	
00CD₁₆	
00CE₁₆	
00CF₁₆	
00D0₁₆	P0 pull-up control register
00D1₁₆	P1–P5 pull-up control register (Note 2)
00D2₁₆	
00D3₁₆	
00D4₁₆	Edge polarity selection register
00D5₁₆	
00D6₁₆	Input latch register
00D7₁₆	
00D8₁₆	
00D9₁₆	A-D control register
00DA₁₆	A-D conversion register
00DB₁₆	
00DC₁₆	Serial I/O mode register
00DD₁₆	Serial I/O register
00DE₁₆	Serial I/O counter | Byte counter
00DF₁₆	

00E0₁₆	
00E1₁₆	
00E2₁₆	
00E3₁₆	
00E4₁₆	
00E5₁₆	
00E6₁₆	
00E7₁₆	
00E8₁₆	
00E9₁₆	
00EA₁₆	
00EB₁₆	
00EC₁₆	
00ED₁₆	
00EE₁₆	
00EF₁₆	
00F0₁₆	Timer 1
00F1₁₆	Timer 2
00F2₁₆	Timer 3
00F3₁₆	Timer 4
00F4₁₆	
00F5₁₆	
00F6₁₆	
00F7₁₆	Timer FF register
00F8₁₆	Timer 12 mode register
00F9₁₆	Timer 34 mode register
00FA₁₆	Timer mode register 2
00FB₁₆	CPU mode register
00FC₁₆	Interrupt request register 1
00FD₁₆	Interrupt request register 2
00FE₁₆	Interrupt control register 1
00FF₁₆	Interrupt control register 2

Notes 1 : This address is not used in the 7470 group.
2 : This address is allocated P1–P4 pull-up control register for the 7470 group.

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 12 different sources consisting of five external, six internal, and one software sources.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. External interrupts INT_0 and INT_1 can be asserted on either the falling or rising edge as set in the edge polarity selection register. When "0" is set to this register, the interrupt is activated on the falling edge; when "1" is set to the register, the interrupt is activated on the rising edge.

When the device is put into power-down state by the STP instruction or the WIT instruction, if bit 5 in the edge polarity selection register is "1", the INT_1 interrupt becomes a key on wake up interrupt. When a key on wake up interrupt is valid, an interrupt request is generated by applying the "L" level to any pin in port P0. In this case, the port used for interrupt must have been set for the input mode.

If bit 5 in the edge polarity selection register is "0" when the device is in power-down state, the INT_1 interrupt is selected. Also, if bit 5 in the edge polarity selection register is set to "1" when the device is not in a power-down state, neither key on wake up interrupt request nor INT_1 interrupt request is generated.

The $CNTR_0$/$CNTR_1$ interrupts function in the same as INT_0 and INT_1. The interrupt input pin can be specified for either $CNTR_0$ or $CNTR_1$ pin by setting bit 4 in the edge polarity selection register.

Figure 4 shows the structure of the edge polarity selection register, interrupt request registers 1 and 2, and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority

Interrupt source	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_0 interrupt	2	$FFFD_{16}$, $FFFC_{16}$	External interrupt (polarity programmable)
INT_1 interrupt or key on wake up interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt (INT_1 is polarity programmable)
$CNTR_0$ interrupt or $CNTR_1$ interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (polarity programmable)
Timer 1 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 2 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
Timer 3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 4 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Serial I/O interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
A-D conversion completion interrupt	10	$FFED_{16}$, $FFEC_{16}$	
BRK instruction interrupt	11	$FFEB_{16}$, $FFEA_{16}$	Non-maskable software interrupt

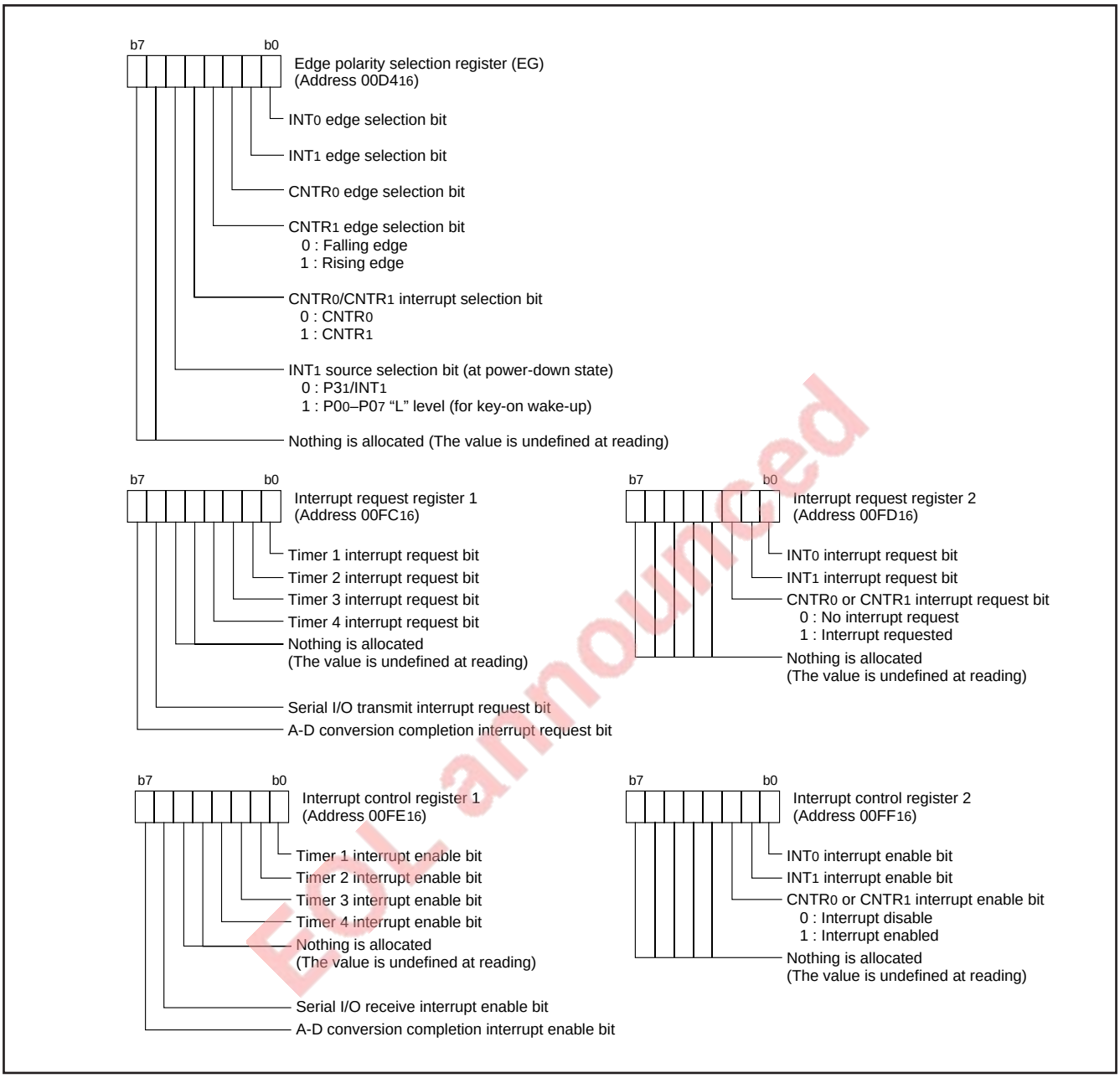


Fig. 4 Structure of registers related to interrupt

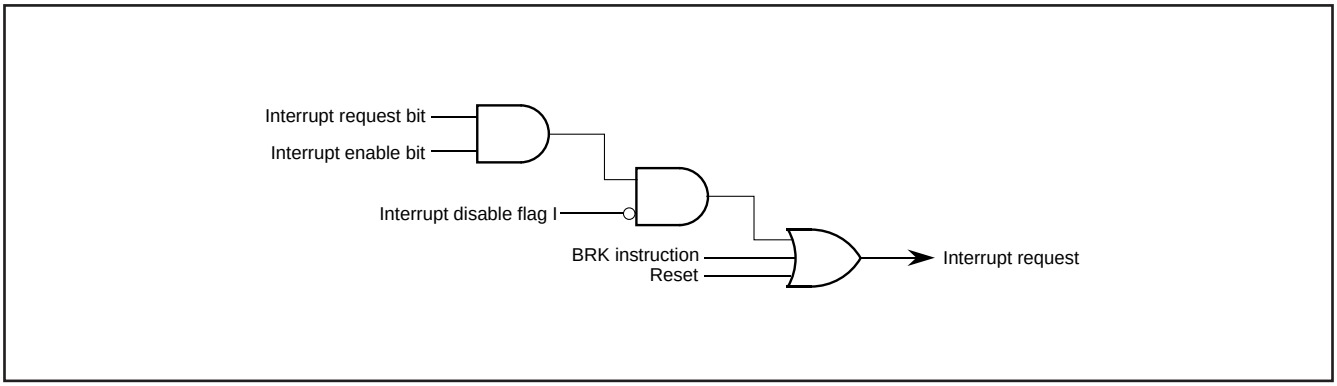


Fig. 5 Interrupt control

TIMER

The 7470/7471 group has four timers; timer 1, timer 2, timer 3, and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

Timer 1 can be operated in the timer mode, event count mode, or pulse output mode. Timer 1 starts counting when bit 0 in the timer 12 mode register (address $00F8_{16}$) is set to "0".

The count source can be selected from the f(XIN) divided by 16, f(XCIN) divided by 16, f(XCIN), or event input from $P3_2$/$CNTR_0$ pin. Do not select f(XCIN) as the count source in the 7470 group. When bit 1 and bit 2 in the timer 12 mode register are "0", f(XIN) divided by 16 or f(XCIN) divided by 16 is selected. Selection between f(XIN) and f(XCIN) is done by bit 7 in the CPU mode register (address $00FB_{16}$). When bit 1 in the timer 12 mode register is "0" and bit 2 is "1", f(XCIN) is selected. And, when bit 1 in the timer 12 mode register is "1", an event input from the $CNTR_0$ pin is selected. Event inputs are selected depending on bit 2 in the edge polarity selection register (address $00D4_{16}$). When this bit is "0", the inverted value of $CNTR_0$ input is selected; when the bit is "1", $CNTR_0$ input is selected.

When bit 3 in the timer 12 mode register is set to "1", the $P1_2$ pin becomes timer output T_0. When the direction register of $P1_2$ is set for the output mode at this time, the timer 1 overflow divided by 2 is output from T_0.

Please set the initial output value in the following procedure.

① Set "1" to bit 0 of the timer 12 mode register.
(Timer 1 count stop.)
② Set "1" to bit 0 of the timer mode register 2.
③ Set the output value to bit 0 of the timer FF register.
④ Set the count value to the timer 1.
⑤ Set "0" to bit 0 of the timer 12 mode register.
(Timer 1 count start.)

Timer 2 can only be operated in the timer mode. Timer 2 starts counting when bit 4 in the timer 12 mode register is set to "0".

The count source can be selected from the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of f(XIN) or f(XCIN), and timer 1 overflow. Do not select f(XCIN) as the count source in the 7470 group. When bit 5 in the timer 12 mode register is "0", any of the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of f(XIN) or (XCIN) is selected. The divide ratio is selected according to bit 6 and bit 7 in the timer 12 mode register, and selection between f(XIN) and f(XCIN) is made according to bit 7 in the CPU mode register. When bit 5 in the timer 12 mode register is "1", timer 1 overflow is selected as the count source.

Timer 3 can be operated in the timer mode, event count mode, or PWM mode. Timer 3 starts counting when bit 0 in the timer 34 mode register (address $00F9_{16}$) is set to "0".

The count source can be selected from the f(XIN) divided by 16, f(XCIN) divided by 16, f(XCIN), timer 1 or timer 2 overflow, or an event input from $P3_3$/$CNTR_1$ pin according to the statuses of bit 1 and bit 2 in the timer 34 mode register, bit 6 in the timer mode register 2 (address $00FA_{16}$) and bit 7 in the CPU mode register. Do not select f(XCIN) as the count source in the 7470 group. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 3 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

Timer 4 can be operated in the timer mode, event count mode, pulse output mode, pulse width measuring mode, or PWM mode. Timer 4 starts counting when bit 3 in the timer 34 mode register is set to "0" when bit 6 in this register is "0". When bit 6 is "1", the pulse width measuring mode is selected. The count source can be selected from timer 3 overflow, f(XIN) divided by 16, f(XCIN) divided by 16, f(XCIN), timer 1 or timer 2 overflow, or an event input from $P3_3$/$CNTR_1$ pin according to the statuses of bit 4 and bit 5 in the timer 34 mode register, bit 6 in the timer mode register 2, and bit 7 in the CPU mode register. Do not select f(XCIN) as the count source in the 7470 group. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 4 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register.

When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

When bit 7 in the timer 34 mode register is set to "1", the $P1_3$ pin becomes timer output T_1. When the direction register of $P1_3$ is set for the output mode at this time, the timer 4 overflow divided by 2 is output from T_1 when bit 7 in the timer mode register 2 is "0".

Please set the initial output value in the following procedure.

① Set "1" to bit 3 of the timer 34 mode register.
(Timer 4 count stop.)
② Set "1" to bit 1 of the timer mode register 2.
③ Set the output value to bit 1 of the timer FF register.
④ Set the count value to the timer 4.
⑤ Set "0" to bit 3 of the timer 34 mode register.
(Timer 4 count start.)

(1) Timer mode

Timer performs down count operations with the dividing ratio being 1/(n+1). Writing a value to the timer latch sets a value to the timer. When the value to be set to the timer latch is nn_{16}, the value to be set to a timer is nn_{16}, which is down counted at the falling edge of the count source from nn_{16} to (nn_{16}-1) to (nn_{16}-2) to ...01_{16} to 00_{16} to FF_{16}. At the falling edge of the count source immediately after timer value has reached FF_{16}, value (nn_{16}-1) obtained by subtracting one from the timer latch value is set (reloaded) to the timer to continue counting. At the rising edge of the count source immediately after the timer value has reached FF_{16}, an overflow occurs and an interrupt request is generated.

(2) Event count mode
Timer operates in the same way as in the timer mode except that it counts input from the $CNTR_0$ or $CNTR_1$ pin.
(3) Pulse output mode
In this mode, duty 50% pulses are output from the T_0 or T_1 pin. When the timer overflows, the polarity of the T_0 or T_1 pin output level is inverted.
(4) Pulse width measuring mode
The 7470/7471 group can measure the "H" or "L" width of the $CNTR_0$ or $CNTR_1$ input waveform by using the pulse width measuring mode of timer 4. The pulse width measuring mode is selected by writing "1" to bit 6 in the timer 34 mode register. In the pulse width measuring mode, the timer counts the count source while the $CNTR_0$ or $CNTR_1$ input is "H" or "L". Whether the $CNTR_0$ input or $CNTR_1$ input to be measured can be specified by the status of bit 4 in the edge polarity selection register; whether the "H" width or "L" width to be measured can be specified by the status of bit 2 ($CNTR_0$) and bit 3 ($CNTR_1$) in the edge polarity selection register.
(5) PWM mode
The PWM mode can be entered for timer 3 and timer 4 by setting bit 7 in the timer mode register 2 to "1". In the PWM mode, the $P1_3$ pin is set for timer output T_1 to output PWM waveforms by setting bit 7 in the timer 34 mode register to "1". The direction register of $P1_3$ must be set for the output mode before this can be done.
In the PWM mode, timer 3 is counting and timer 4 is idle while the PWM waveform is "L". When timer 3 overflows, the PWM waveform goes "H". At this time, timer 3 stops counting simultaneously and timer 4 starts counting. When timer 4 overflows, the PWM waveform goes "L", and timer 4 stops and timer 3 starts counting again. Consequently, the "L" duration of the PWM waveform is determined by the value of timer 3; the "H" duration of the PWM waveform is determined by the value of timer 4.
When a value is written to the timer in operation during the PWM mode, the value is only written to the timer latch, and not written to the timer. In this case, if the timer overflows, a value one less the value in the timer latch is written to the timer. When any value is written to an idle timer, the value is written to both the timer latch and the timer.
In this mode, do not select timer 3 overflow as the count source for timer 4.

INPUT LATCH FUNCTION

The 7470/7471 group can latch the $P3_0/INT_0$, $P3_1/INT_1$, $P3_2/CNTR_0$, and $P3_3/CNTR_1$ pin level into the input latch register (address $00D6_{16}$) when timer 4 overflows. The polarity of each pin latched to the input latch register can be selected by using the edge polarity selection register. When bit 0 in the edge polarity selection register is "0", the inverted value of the $P3_0/INT_0$ pin level is latched; when the bit is "1", the $P3_0/INT_0$ pin level is latched as it is. When bit 1 in the edge polarity selection register is "0", the inverted value of the $P3_1/INT_1$ pin level is latched; when the bit is "1", the $P3_1/INT_1$ pin level is latched as it is. When bit 2 in the edge polarity selection register is "0", the inverted value of the $P3_2/CNTR_0$ pin level is latched; when the bit is "1", the $P3_2/CNTR_0$ pin level is latched as it is. When bit 3 in the edge polarity selection register is "0", the inverted value of the $P3_3/CNTR_1$ pin level is latched; when the bit is "1", the $P3_3/CNTR_1$ pin level is latched as it is.

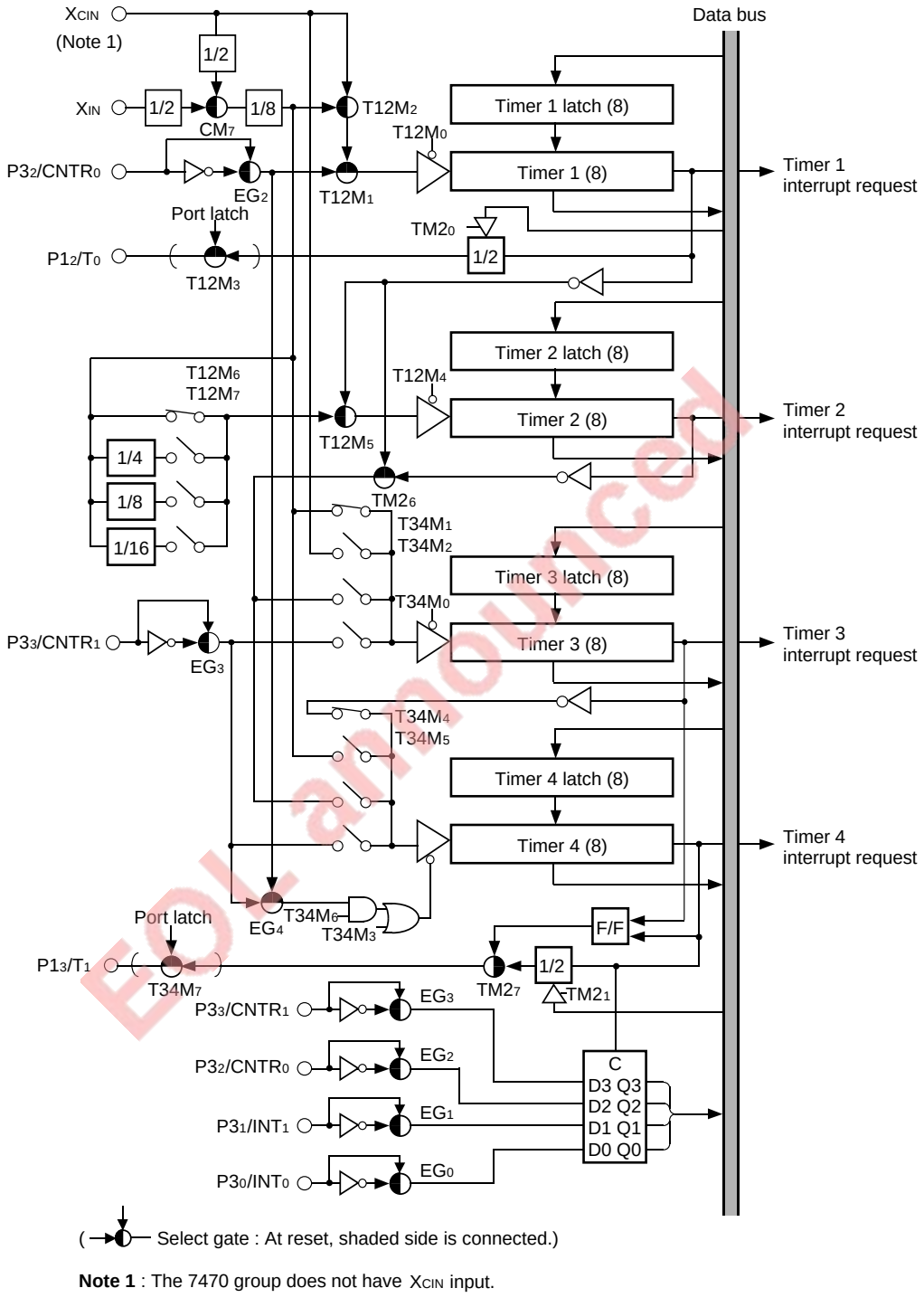
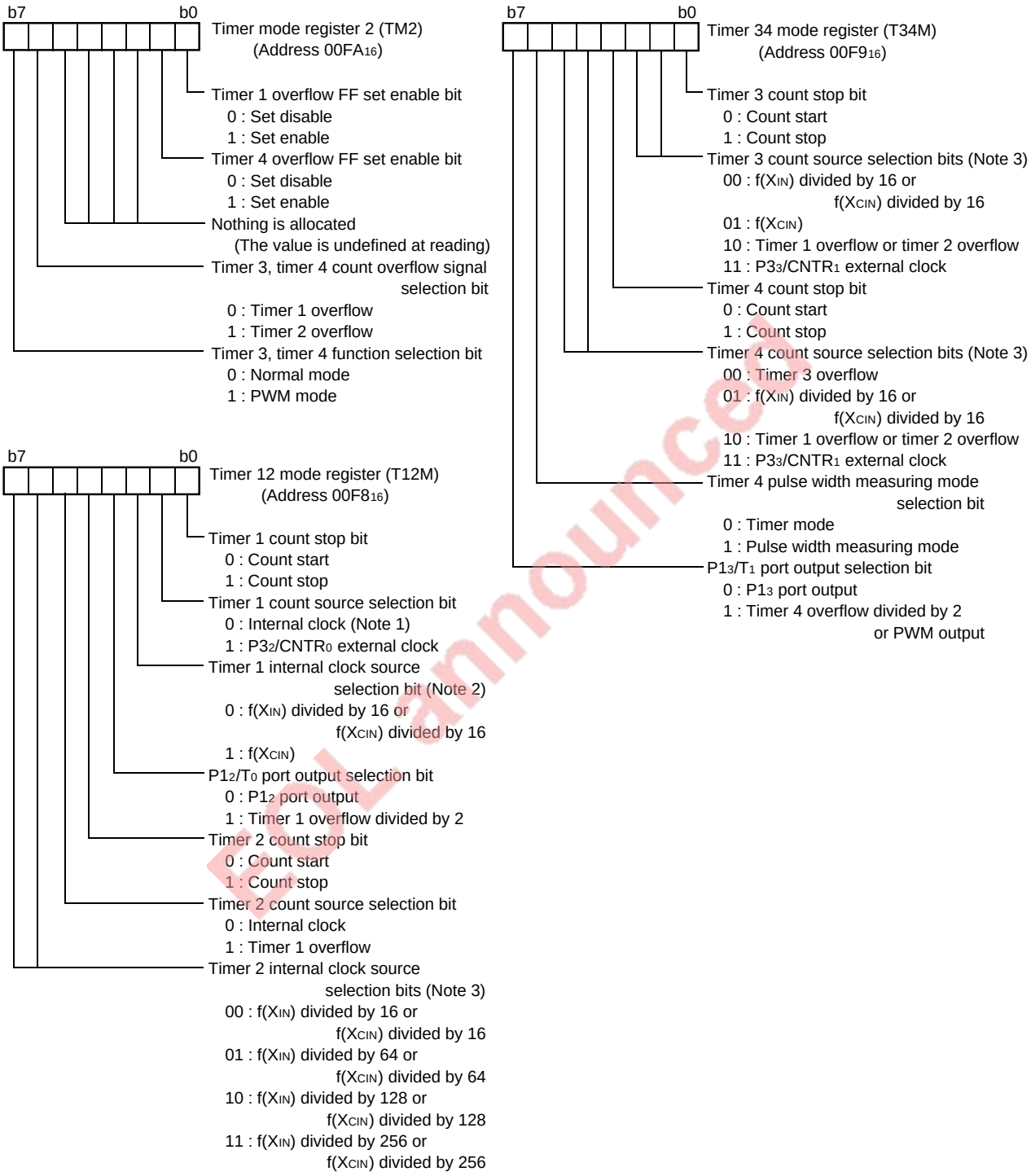


Fig. 6 Block diagram of timer 1 through 4



Notes 1 : f(XIN) divided by 16 in the 7470 group.
2 : The 7470 group does not use this bit (bit 2). Set this bit to "0".
3 : Do not select f(XCIN) as the count source in the 7470 group.

Fig. 7 Structure of timer mode registers

SERIAL I/O

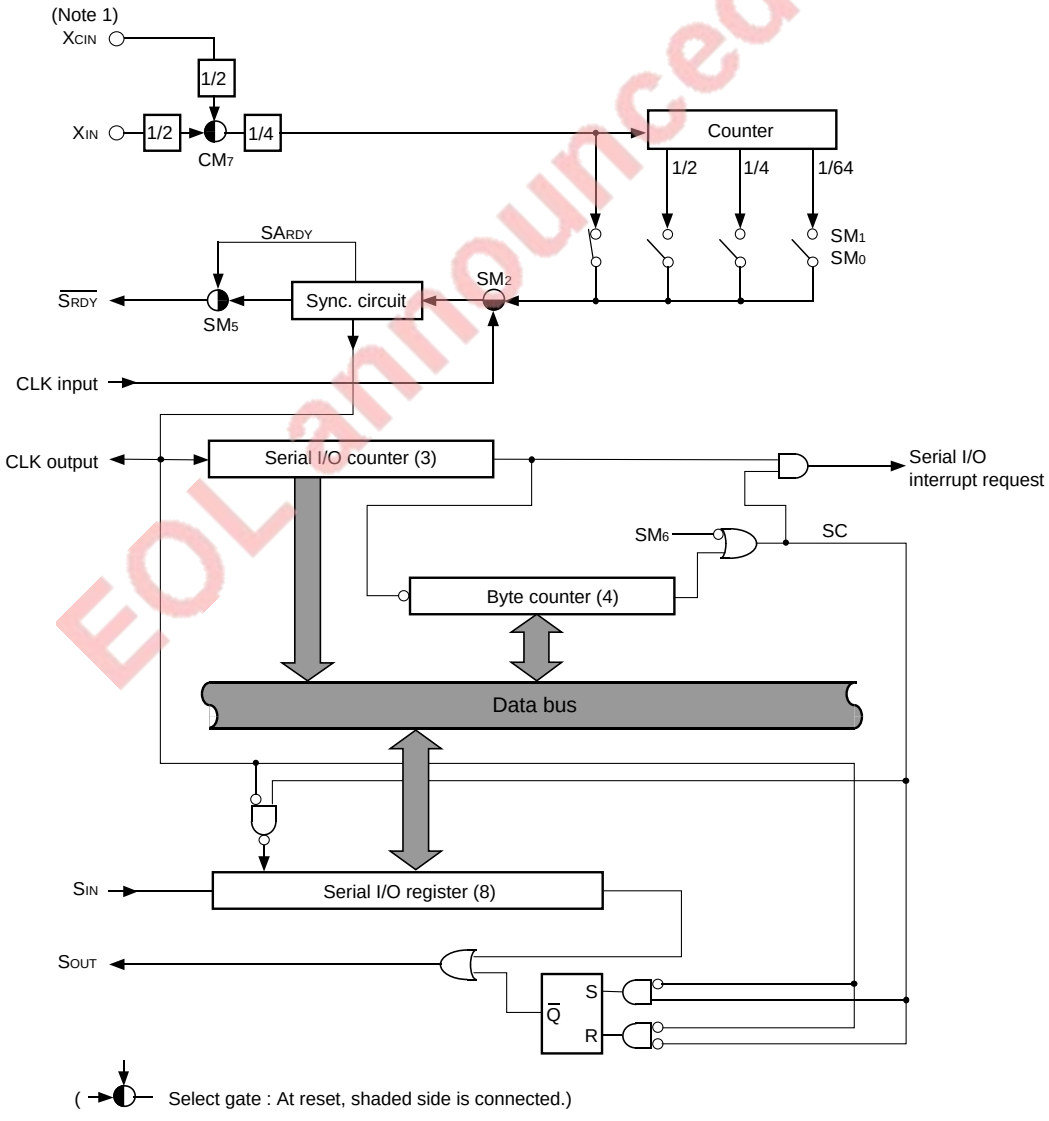
The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode, the receive ready signal ($\overline{SRDY}$), synchronous input/output clock (CLK), and the serial I/O (SOUT, SIN) pins are used as $P1_7$, $P1_6$, $P1_5$, and $P1_4$, respectively.

The serial I/O mode register (address $00DC_{16}$) is an 8-bit register. Bit 2 of this register is used to select a synchronous clock source. When this bit is "0", an external clock from $P1_6$ is selected. When this bit is "1", an internal clock is selected.

The internal clock can be selected from among the divide by 8, divide by 16, divide by 32, divide by 512 frequency of the oscillator frequency f(XIN) or f(XCIN). Do not select f(XCIN) as the count source in the 7470 group. The divide ratio is selected according to bit 0 and bit 1 in the serial I/O mode register, and selection between f(XIN) and f(XCIN) is mode according to bit 7 in the CPU mode register.

Bits 3 and 4 decide whether parts of P1 will be used as a serial I/O or not. When bit 3 is "1", $P1_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P1_6$. If the external synchronous clock is selected, the clock is input to $P1_6$.

And $P1_5$ will be a serial output. To use $P1_4$ as a serial input, set the direction register bit which corresponds to $P1_4$, to "0". For more information on the direction register, refer to the I/O pin section.



Note 1 : The 7470 group does not have XCIN input.

Fig. 8 Block diagram of serial I/O

Bit 4 determines if P17 is used as an output pin for the receive ready signal (bit 4="1", $\overline{\text{SRDY}}$) or used as a normal I/O pin (bit 4="0").

When the P17 pin is used as the $\overline{\text{SRDY}}$ output pin, output signal can be selected between $\overline{\text{SRDY}}$ signal and SARDY signal by using bit 5 in the serial I/O mode register. The $\overline{\text{SRDY}}$ signal is driven "L" by a signal written into the serial I/O register to inform that the device is ready to receive. Then, the $\overline{\text{SRDY}}$ signal is driven "H" on the first falling edge of the transfer clock.

The SARDY signal is driven "H" by a signal written into the serial I/O register, and driven "L" on the last rising edge of the transfer clock.

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock – The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P15. During the rising edge of this clock, data can be input from P14 and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock – If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside.

Timing diagrams are shown in Figure 9.

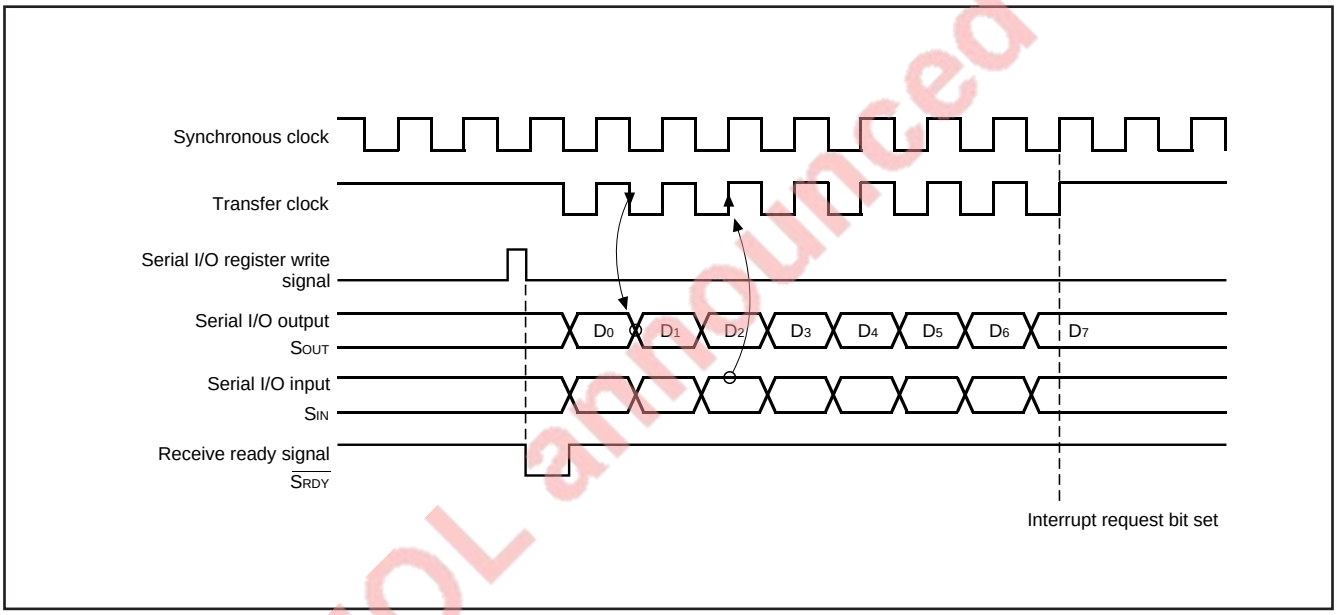
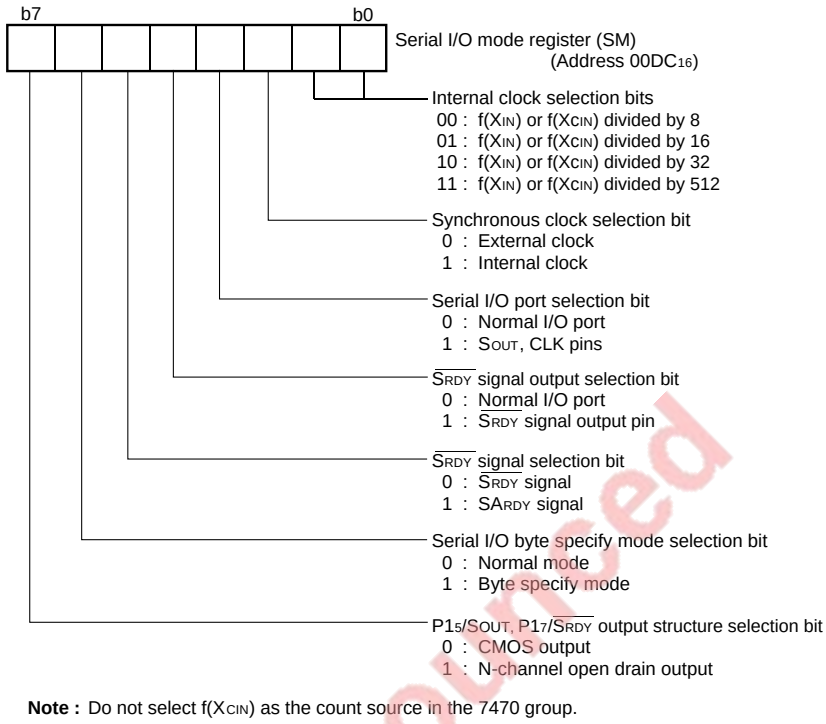


Fig. 9 Serial I/O timing



Note : Do not select f(XCIN) as the count source in the 7470 group.

Fig. 10 Structure of serial I/O mode register

BYTE SPECIFY MODE

The serial I/O has a byte specify mode that allows one specific byte data to be selected for transmission or reception when serial I/O circuits of two or more microcomputers are connected to send or receive data through one bus. The data to be sent or received can be specified by writing a value into the byte counter. The value written in the byte counter is decremented by one each time eight cycles of transfer clock are input. When the value in the byte counter becomes “0”, serial transmission/reception is done by the next eight cycles of transfer clock. When the value in the byte counter is not “0”, the output on the SOUT pin is driven “H” by the falling edge of the first transfer clock pulse to inhibit transmission/reception.

Serial I/O interrupt requests are generated only when serial transmission/reception is done after the value in the byte counter is decremented to “0”. When the SARDY signal output is selected, the SARDY signal is driven “L” by the last rising edge of the transfer clock after the value in the byte counter is decremented to “0”.

Note that in the byte mode, an external clock must be used as the sync. clock for the purpose of the mode.

A-D CONVERTER

The A-D conversion uses an 8-bit successive comparison method. Figure 11 shows a block diagram of the A-D conversion circuit. Conversion is automatically carried out once started by the program.

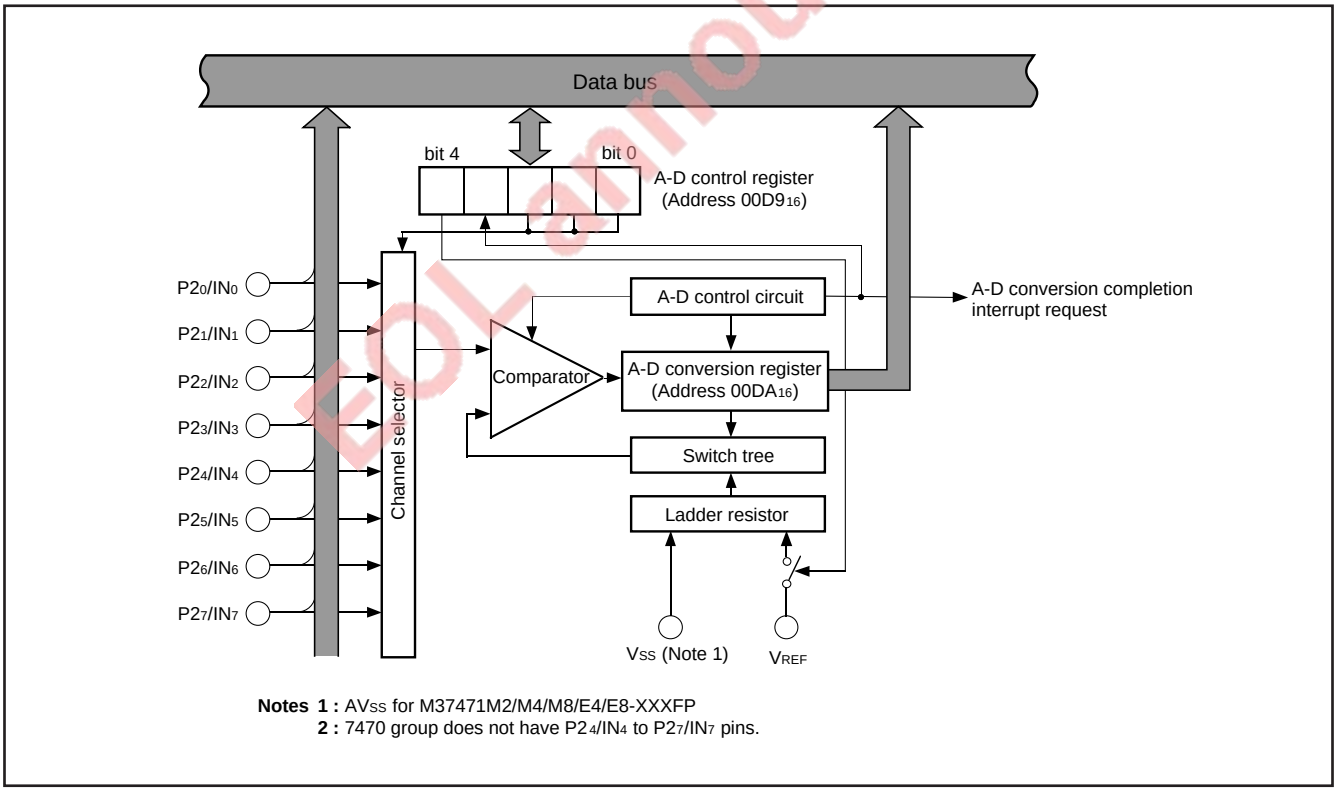
There are eight analog input pins which are shared with $P2_0$ to $P2_7$ of port P2 (Only $P2_0$ to $P2_3$ 4-bit for 7470 group. Which analog inputs are to be A-D converted is specified by using bit 2 to bit 0 in the A-D control register (address $00D9_{16}$). Pins for inputs to be A-D converted must be set for input by setting the direction register bit to "0". Bit 3 in the A-D control register is an A-D conversion end bit. This is "0" during A-D conversion; it is set to "1" when the conversion is terminated. Therefore, it is possible to know whether A-D conversion is terminated by checking this bit. Bit 4 in the A-D control register is a V_{REF} connection selection bit.

During A-D conversion, this bit must be set "1" for the ladder resistor and V_{REF} pin to be connected; after the A-D conversion is terminated, this bit can be reset to "0" to separate the ladder resistor from the V_{REF} pin. In this way, power consumption in the ladder resistor can be suppressed while no A-D conversion is performed. Figure 13 shows the relationship between the contents of A-D control register and the selected input pins.

The A-D conversion register (address $00DA_{16}$) contains information on the results of conversion, so that it is possible to know the results of conversion by reading the contents of this register.

The following explains the procedure to execute A-D conversion. First, set values to bit 2 to bit 0 in the A-D control register to select the pins that you want to execute A-D conversion. Next, clear the A-D conversion end bit to "0".

When the above is done, A-D conversion is initiated. The A-D conversion is completed after an elapse of 50 machine cycles (12.5 µs when $f(X_{IN})$= 8 MHz), the A-D conversion end bit is set to "1", and the interrupt request bit is set to "1". The results of conversion are contained in the A-D conversion register.



Notes 1 : AV_{SS} for M37471M2/M4/M8/E4/E8-XXXFP
2 : 7470 group does not have $P2_4/IN_4$ to $P2_7/IN_7$ pins.

Fig. 11 A-D converter circuit

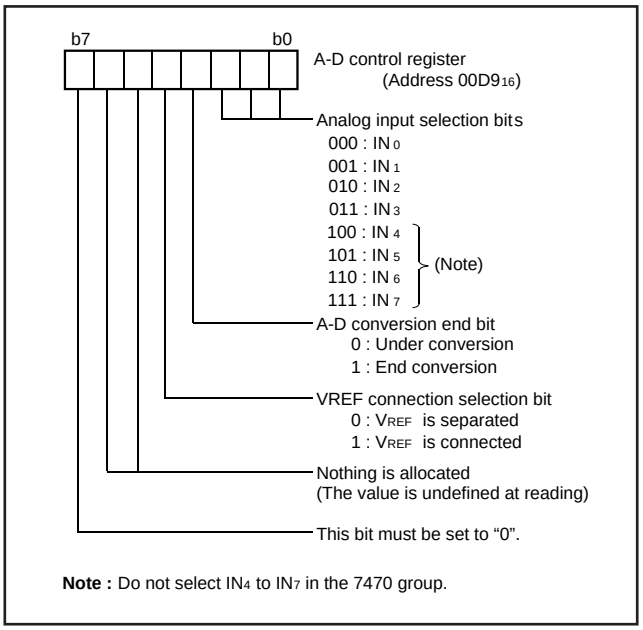
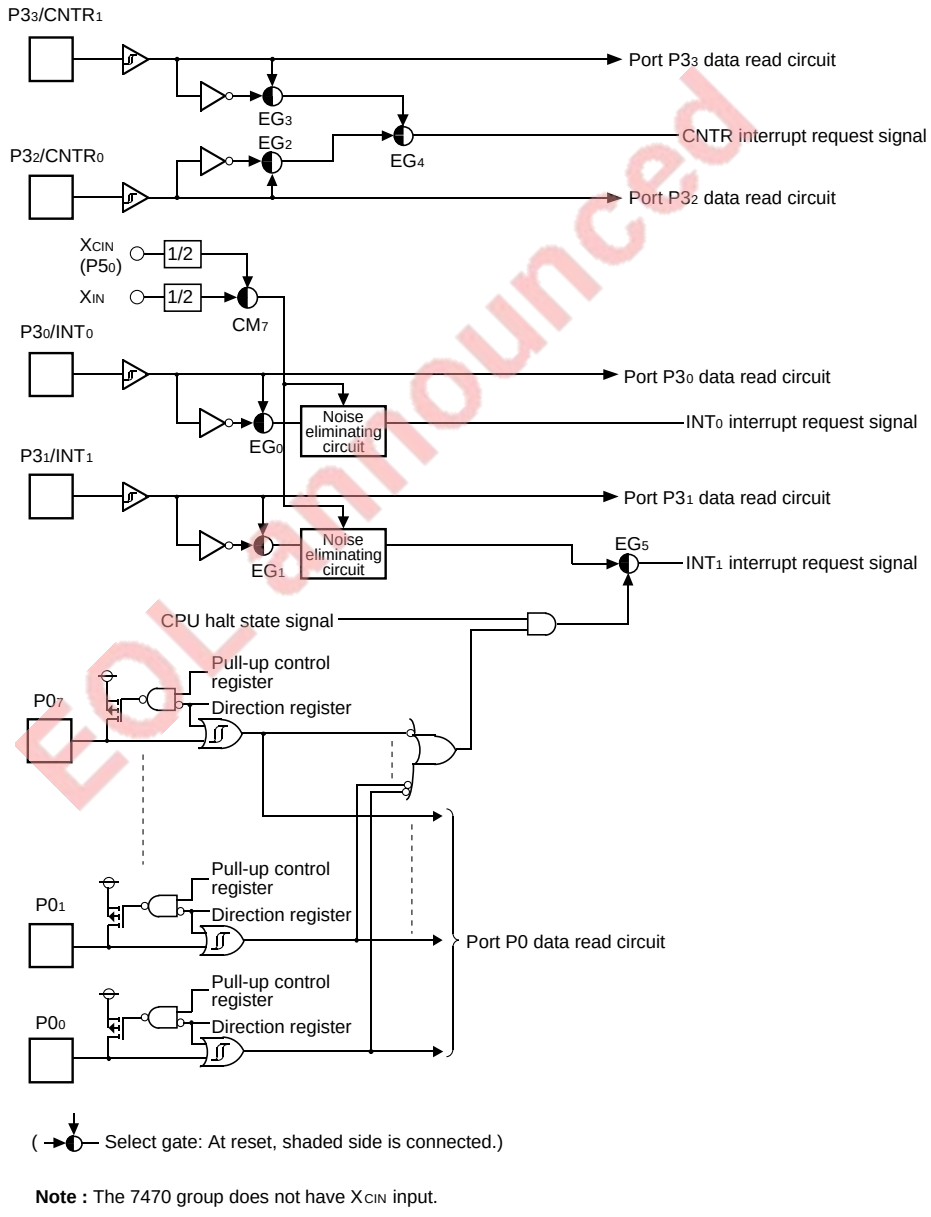


Fig. 12 Structure of A-D control register

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P0 has "L" level applied, after bit 5 of the edge polarity selection register (EG_5) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. A key matrix can be connected to port P0 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_1}$ interrupt. When EG_5 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_1}$ are invalid.



Note : The 7470 group does not have X_{CIN} input.

Fig. 13 Block diagram of interrupt input and key on wake up circuit

RESET CIRCUIT

The 7470/7471 group are reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address FFFF16 as the high order address and the content of the address FFFE16 as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 2 µs while the power voltage is in the recommended operating condition and then returned to "H" level.

The internal initializations following reset are shown in Figure 16. Example of reset circuit is Figure 14. Immediately after reset, timer 3 and timer 4 are connected, and counts the f(XIN) divided by 16. At this time, FF16 is set to timer 3, and 0716 is set to timer 4. The reset is cleared when timer 4 overflows.

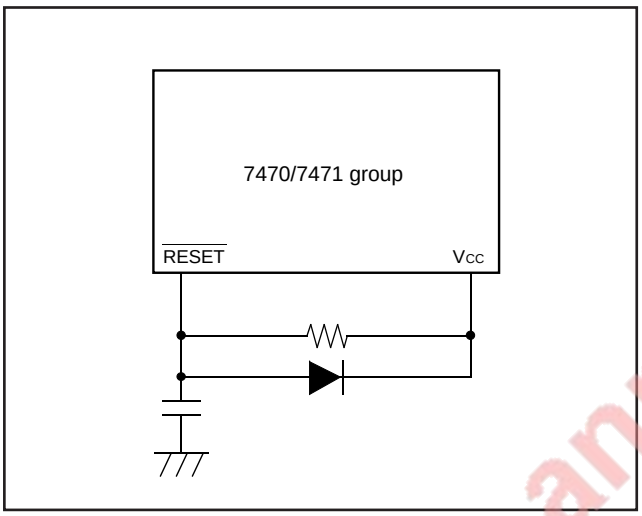
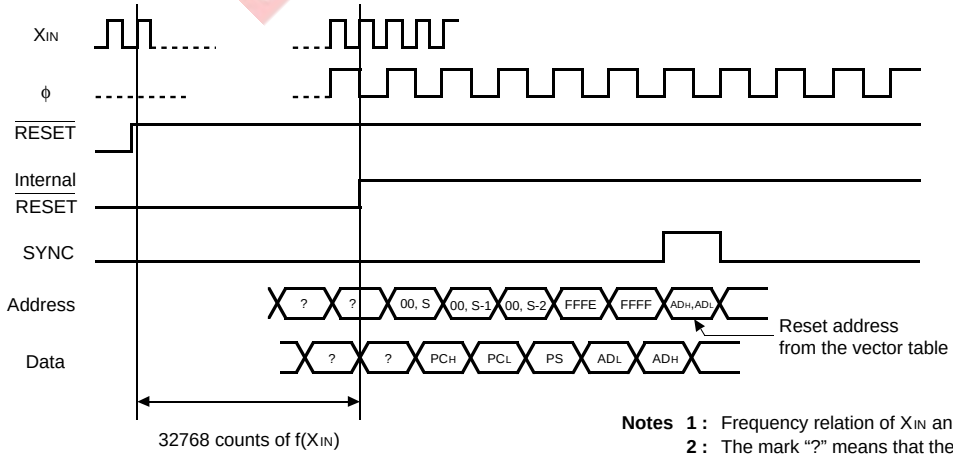


Fig. 14 Example of reset circuit

		Address	
(1)	Port P0 direction register	(C116) …	0016
(2)	Port P1 direction register	(C316) …	0016
(3)	Port P2 direction register	(C516) …	0016
(4)	Port P4 direction register	(C916) …	0 0 0 0
(5)	P0 pull-up control register	(D016) …	0016
(6)	P1–P5 pull-up control register (Note 1)	(D116) …	0 0 0 0 0 0
(7)	Edge selection register	(EG) (D416) …	0 0 0 0 0 0
(8)	A-D control register	(D916) …	0 0 1 0 0 0
(9)	Serial I/O mode register	(SM) (DC16) …	0016
(10)	Timer 12 mode register	(T12M) (F816) …	0016
(11)	Timer 34 mode register	(T34M) (F916) …	0016
(12)	Timer mode register 2	(TM2) (FA16) …	0 0 0 0
(13)	CPU mode register	(CM) (FB16) …	0 0 0 0 0 0 0 0
(14)	Interrupt request register 1	(FC16) …	0 0 0 0 0 0 0 0
(15)	Interrupt request register 2	(FD16) …	0 0 0 0
(16)	Interrupt control register 1	(FE16) …	0 0 0 0 0 0 0 0
(17)	Interrupt control register 2	(FF16) …	0 0 0 0
(18)	Program counter	(PCH) …	Contents of address FFFF16
		(PCL) …	Contents of address FFFE16
(19)	Processor status register	(PS) …	1

Notes 1 : This address is allocated P1–P4 pull-up control register for 7470 group. Bit 6 is not used.
2 : Since the contents of both registers other than those listed above (including timers and the serial I/O register) are undefined at reset, it is necessary to set initial values.

Fig. 16 Internal state of microcomputer at reset



Notes 1 : Frequency relation of XIN and ϕ is f(XIN)=2·ϕ.
2 : The mark "?" means that the address is changeable depending upon the previous state.

Fig. 15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs. As shown in Figure 2, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's direction register allows each bit to be programmed individually as input or output. The direction register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port latch and output. When data is read from the output port, the output pin level is not read, only the latched data of the port latch is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output latch and the pin still remains in the high impedance state. Following the execution of STP or WIT instruction, key matrix with port P0 can be used to generate the interrupt to bring the microcomputer back in its normal state. When this port is selected for input, pull-up transistor can be connected in units of 1-bit.

(2) Port P1

Port P1 has the same function as port P0. $P1_2$–$P1_7$ serve dual functions, and the desired function can be selected by the program. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(3) Port P2

Port P2 has the same function as port P0. In the 7470 group, this port is $P2_0$–$P2_3$, a 4-bit I/O port. This port can also be used as the analog voltage input pins. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(4) Port P3

Port P3 is a 4-bit input port.

(5) Port P4

Port P4 is a 4-bit I/O port and has basically the same functions as port P0. In the 7470 group, this port is $P4_0$ and $P4_1$, a 2-bit I/O port. When this port is selected for input, pull-up transistor can be connected in units of 4-bit .

(6) Port P5

Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$ and $P5_1$ are shared with clock generating circuit input/output pins.

The 7470 group does not have this port.

(7) INT_0 pin ($P3_0$/INT_0 pin)

This is an interrupt input pin, and is shared with port $P3_0$. When "H" to "L" or "L" to "H" transition input is applied to this pin, the INT_0 interrupt request bit (bit 0 of address $00FD_{16}$) is set to "1".

(8) INT_1 pin ($P3_1$/INT_1 pin)

This is an interrupt input pin, and is shared with port $P3_1$. When "H" to "L" or "L" to "H" transition input is applied to this pin, the INT_1 interrupt request bit (bit 1 of address $00FD_{16}$) is set to "1".

(9) Counter input $CNTR_0$ pin ($P3_2$/$CNTR_0$ pin)

This is a timer input pin, and is shared with port $P3_2$.

When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and "H" to "L" or "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

(10) Counter input $CNTR_1$ pin ($P3_3$/$CNTR_1$ pin)

This is a timer input pin, and is shared with port $P3_3$.

When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and "H" to "L" or "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

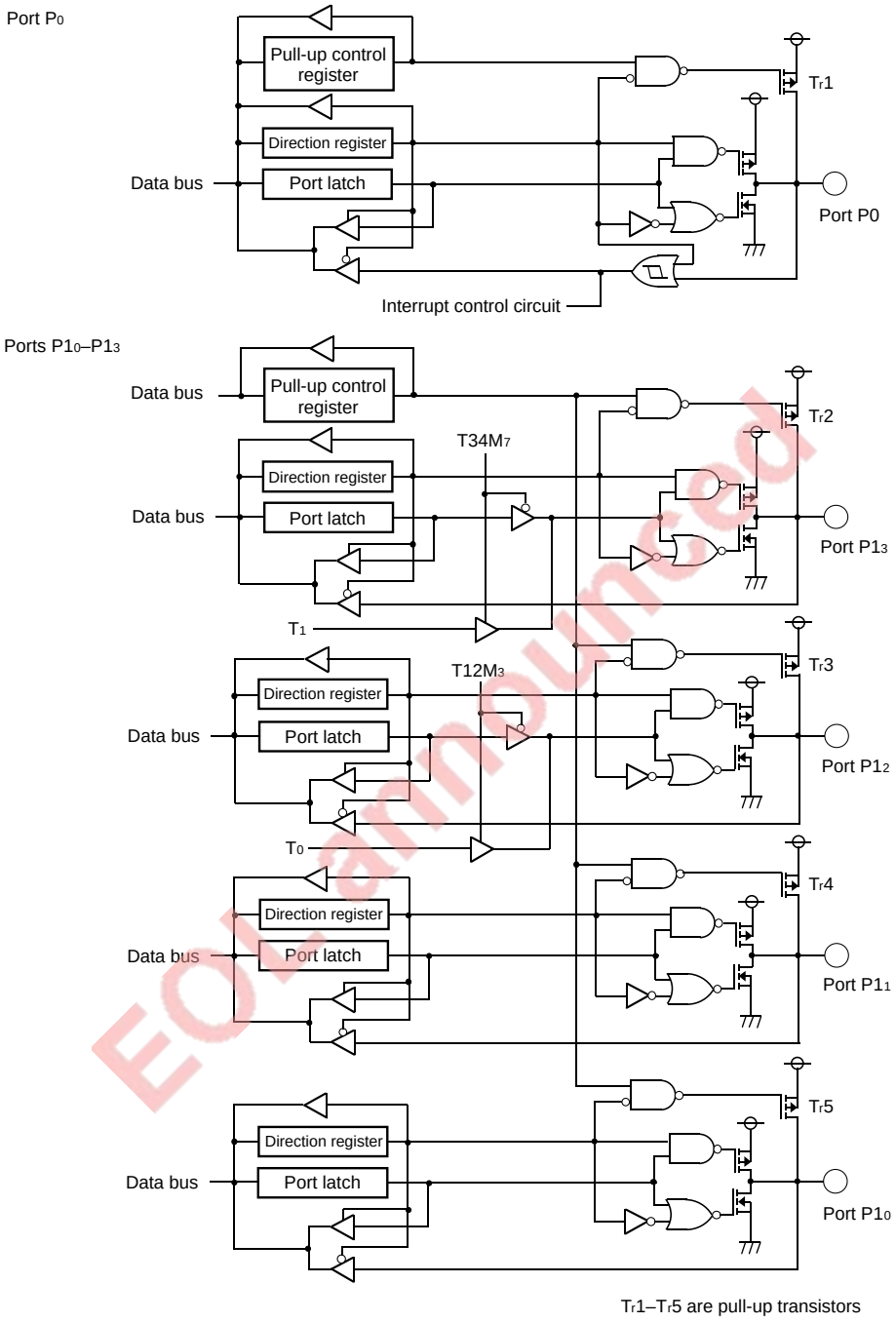


Fig. 17 Block diagram of ports P0, P10–P13

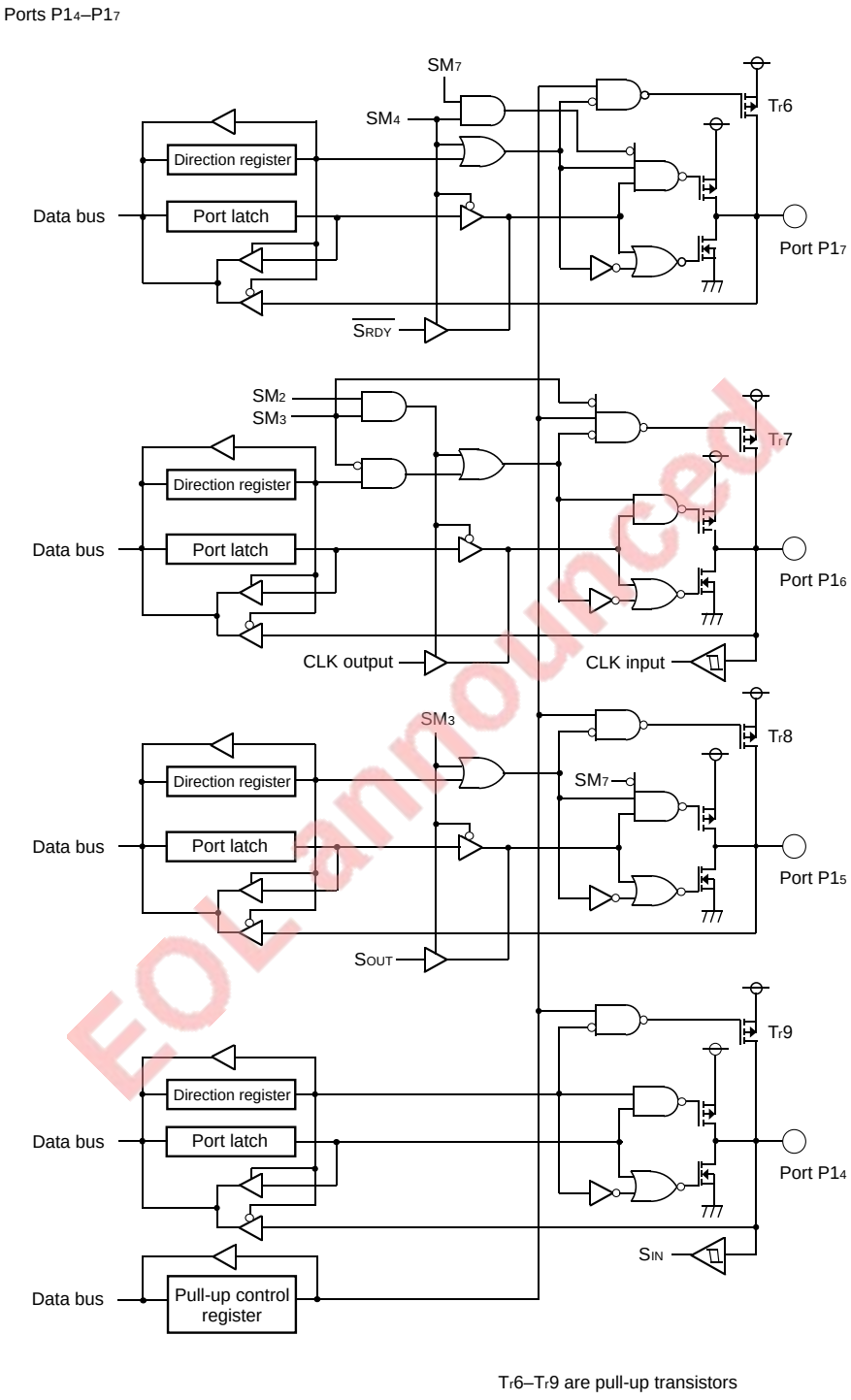


Fig. 18 Block diagram of ports P14–P17

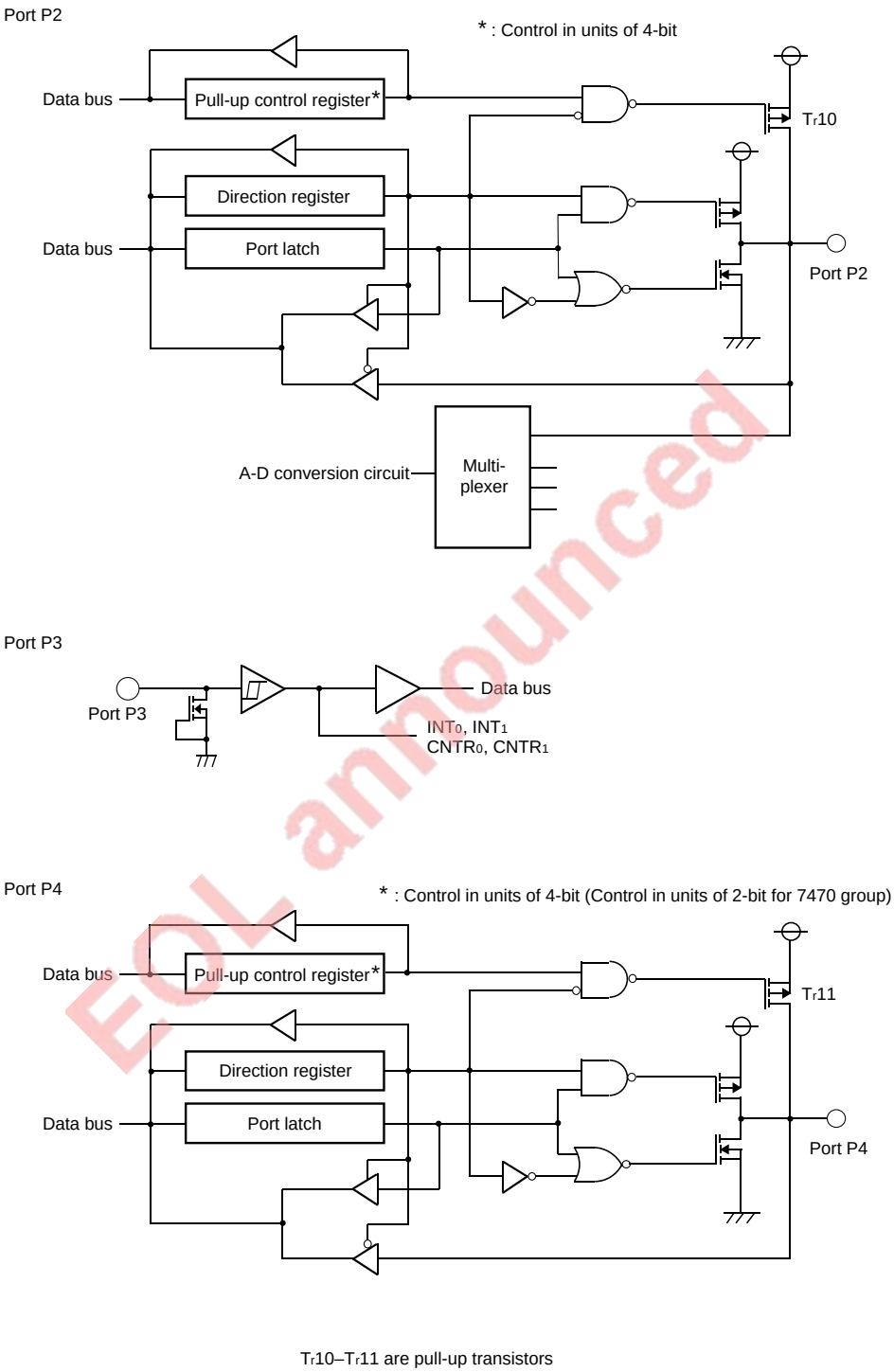
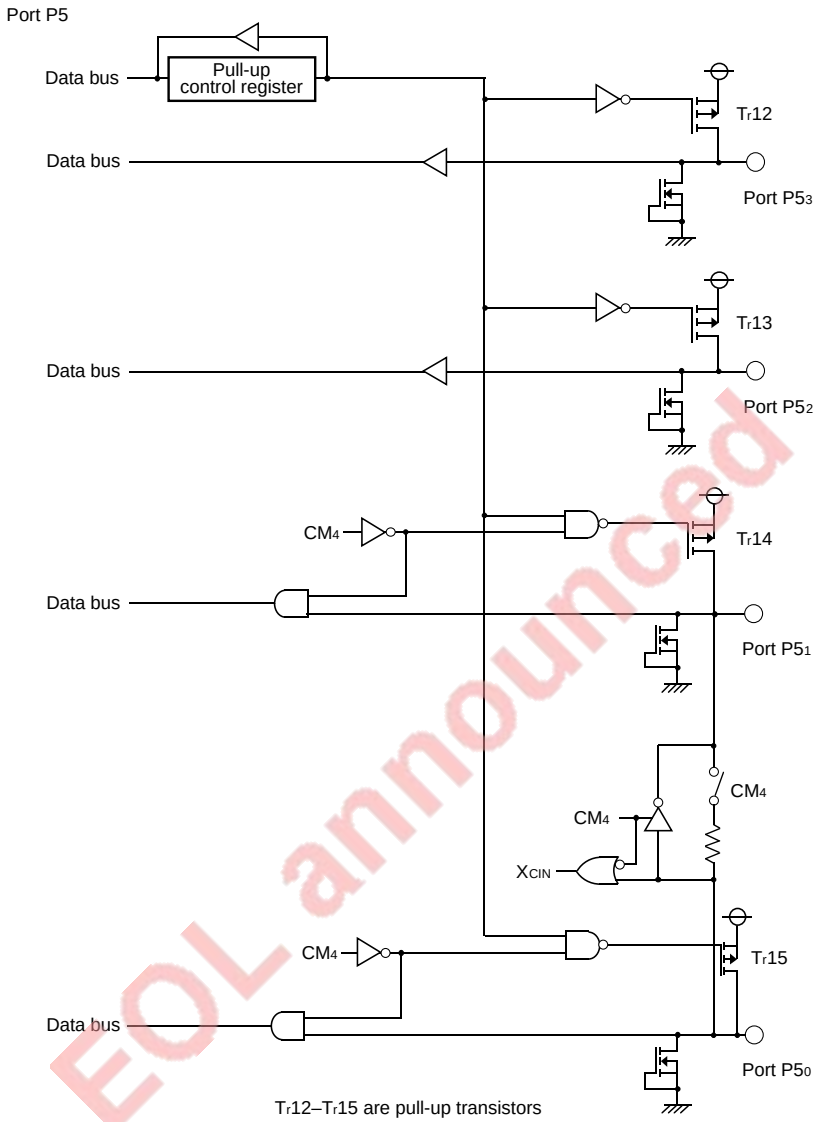


Fig. 19 Block diagram of ports P2–P4



Note : 7470 group does not have this port.

Fig. 20 Block diagram of port P5

CLOCK GENERATING CIRCUIT

The 7470 group has one internal clock generating circuit and 7471 group has two internal clock generating circuits.

Figure 25 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin XIN divided by two is used as the internal clock ϕ. Bit 7 of CPU mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin XCIN in the 7471 group.

Figure 21, 22 show a circuit example using a ceramic resonator (or a quartz-crystal oscillator). Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the XIN(XCIN) pin and leave the XOUT(XCOUT) pin open. A circuit example is shown in Figure 23, 24.

The 7470/7471 group has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both XIN clock and XCIN clock) stops with the internal clock ϕ held at "H" level. In this case timer 3 and timer 4 are forcibly connected and FF_{16} is automatically set in timer 3 and 07_{16} in timer 4.

Although oscillation is restarted when an external interrupt is accepted, the internal clock ϕ remains in the "H" state until timer 4 overflows. In other words, the internal clock ϕ is not supplied until timer 4 overflows. This is because when a ceramic or similar other oscillator is used, a finite time is required until stable oscillation is obtained after restart.

The microcomputer enters an wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode or the stop mode must be set to "1" before executing the WIT or the STP instruction.

Low power dissipation operation is also achieved when the XIN clock is stopped and the internal clock ϕ is generated from the XCIN clock (30 μA typ. at f(XCIN) = 32 kHz). This operation is only 7471 group. XIN clock oscillation is stopped when the bit 6 of CPU mode register is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 27 shows the transition of states for the system clock.

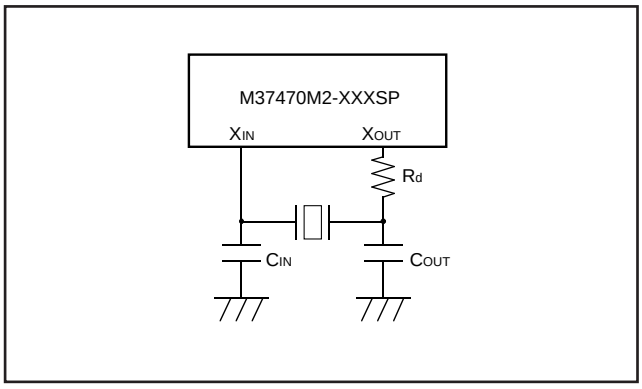


Fig. 21 Example of ceramic resonator circuit (7470 group)

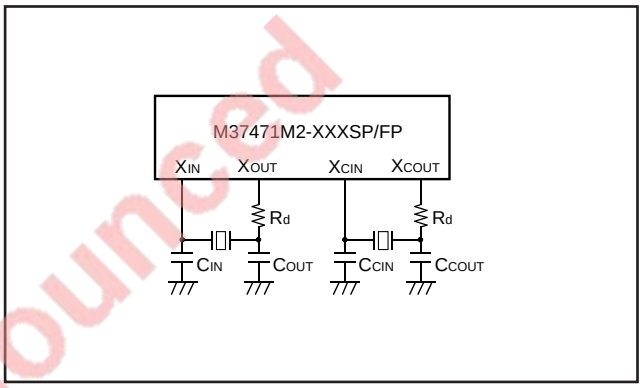


Fig. 22 Example of ceramic resonator circuit (7471 group)

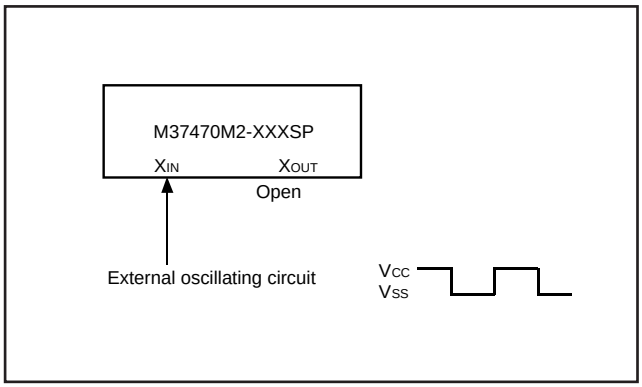


Fig. 23 External clock input circuit (7470 group)

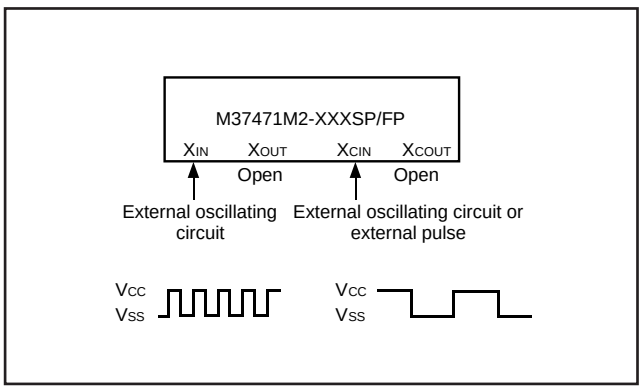
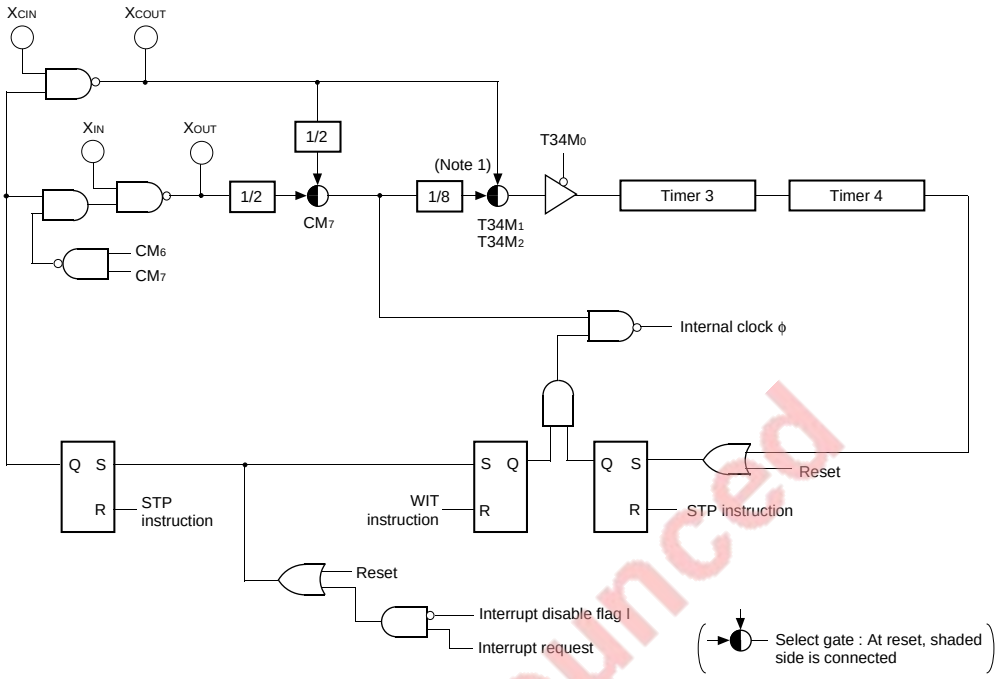
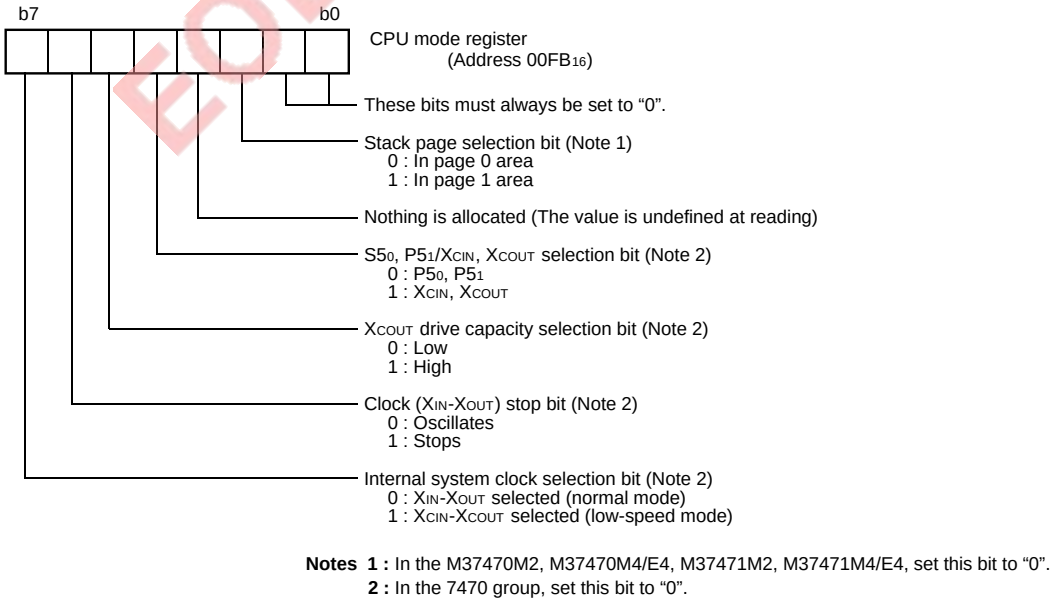


Fig. 24 External clock input circuit (7471 group)



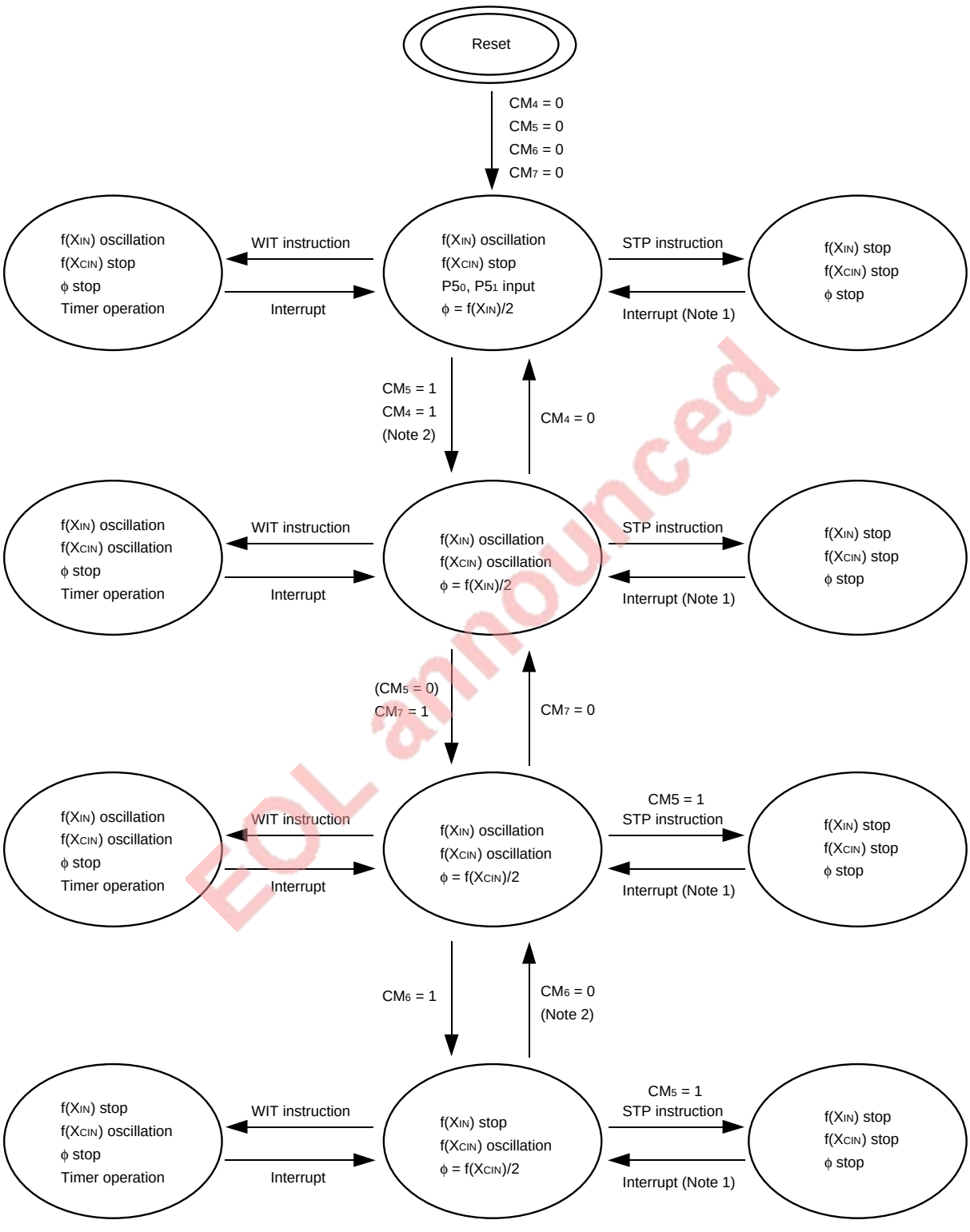
Notes 1 : Refer to Timer 3 of [Figure 6 Block diagram of timer 1 through 4]
2 : 7470 group does not have X_{CIN} input and X_{COUT} output.

Fig. 25 Block diagram of clock generating circuit



Notes 1 : In the M37470M2, M37470M4/E4, M37471M2, M37471M4/E4, set this bit to “0”.
2 : In the 7470 group, set this bit to “0”.

Fig. 26 Structure of CPU mode register

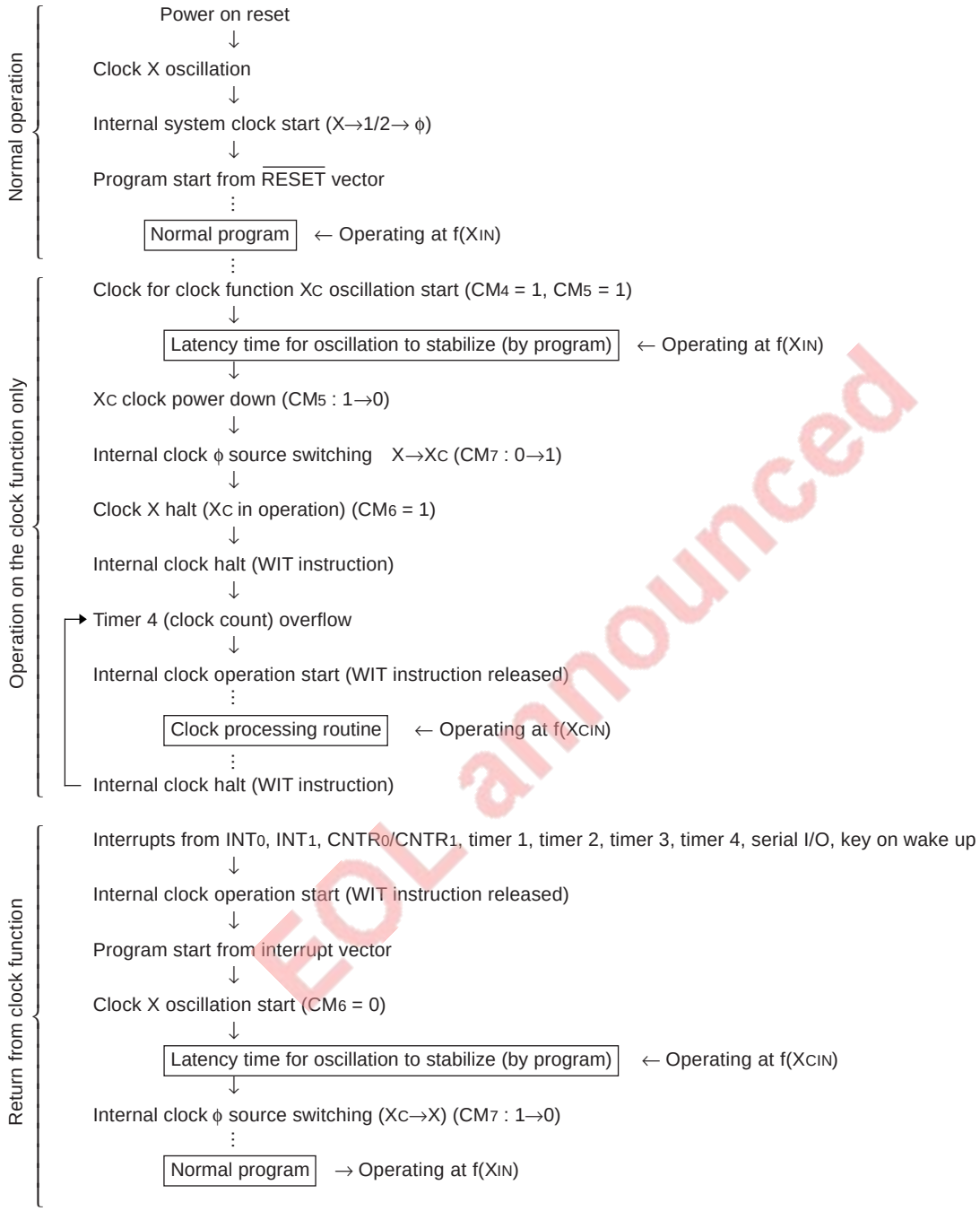


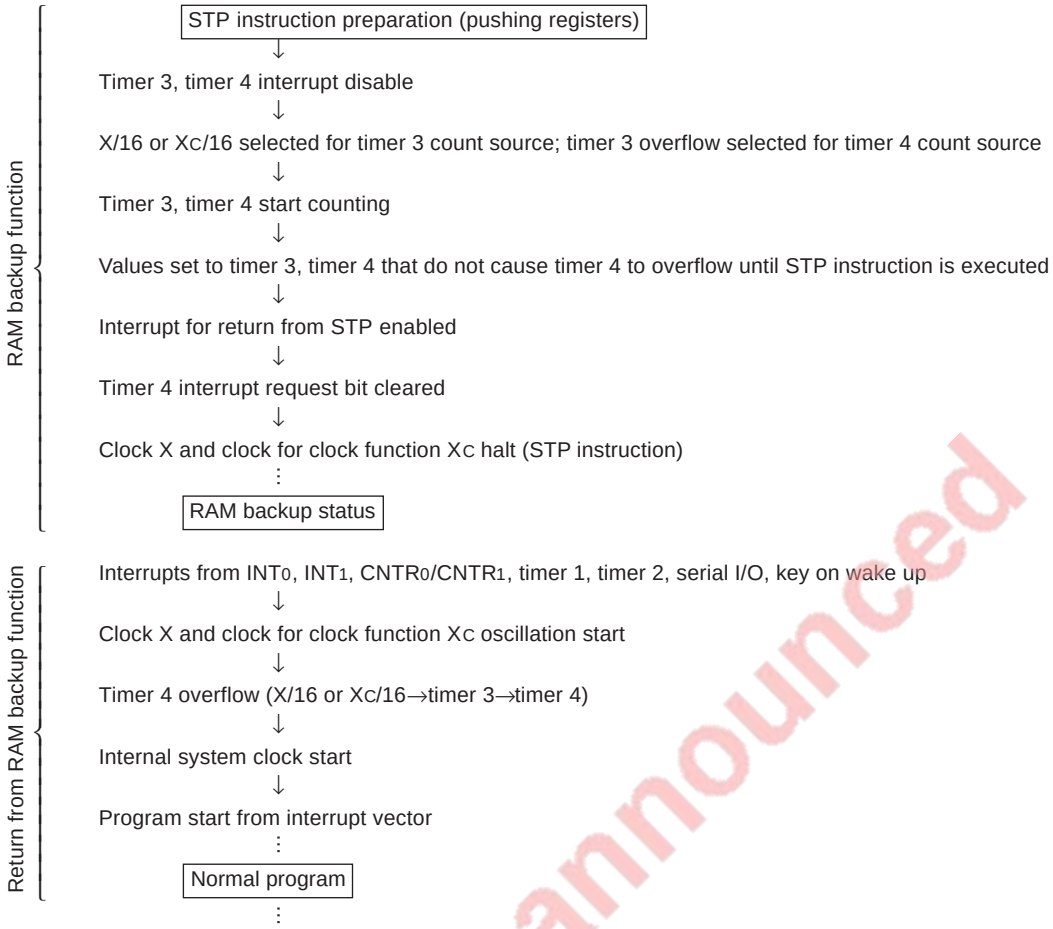
Notes 1 : Latency time is automatically generated upon release from the STP instruction due to the connections of timer 3 and 4.

2 : When the system clock is switched over by restarting clock oscillation, a certain wait time required for oscillation to stabilize must be inserted by the program.

Fig. 27 Transition of states for the system clock

<An example of flow for system>





BUILT-IN PROM TYPE MICROCOMPUTERS
PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC},V_{SS}	Single-chip /EPROM	Power source		Power source voltage inputs 2.7 to 5.5 V to V_{CC} and 0 V to V_{SS}.
AV_{SS} (Note 1)	Single-chip /EPROM	Analog power source		Ground level input pin for A-D converter. Same voltage as V_{SS} is applied.
$\overline{RESET}$	Single-chip	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2 μs or more (under normal V_{CC} conditions).
	EPROM	Reset input		Connect to V_{SS}.
X_{IN}	Single-chip /EPROM	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz-crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open. Feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}		Clock output	Output	
V_{REF}	Single-chip	Reference voltage input	Input	Reference voltage input pin for the A-D converter.
	EPROM	Select mode	Input	V_{REF} works as $\overline{CE}$ input.
$P0_0$–$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided.
	EPROM	Data input/output D_0–D_7	I/O	Port P0 works as an 8-bit data bus (D_0–D_7).
$P1_0$–$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1. $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively. The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output.
	EPROM	Address input A_4–A_{10}	Input	$P1_1$–$P1_7$ works as the 7-bit address input (A_4–A_{10}). $P1_0$ must be opened.
$P2_0$–$P2_7$ (Note 2)	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit input port. This port is in common with analog input pins IN_0–IN_7.
	EPROM	Address input A_0–A_3	Input	$P2_0$–$P2_3$ works as the lower 4-bit address input (A_0–A_3). $P2_4$–$P2_7$ must be opened.
$P3_0$–$P3_3$	Single-chip	Input port P3	Input	Port P3 is a 4-bit input port. $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$.
	EPROM	Address input A_{11}, A_{12} Select mode V_{PP} input	Input	$P3_0$, $P3_1$ works as the 2-bit address input (A_{11}, A_{12}). $P3_2$ works as $\overline{OE}$ input. Connect to $P3_3$ to V_{PP} when programming or verifying.
$P4_0$–$P4_3$ (Note 3)	Single-chip	I/O port P4	I/O	Port P4 is a 4-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.
	EPROM	Address input A_{13}, A_{14}	Input	$P4_0$, $P4_1$ works as the higher 2-bit address input (A_{13}, A_{14}). $P4_2$, $P4_3$ must be opened.
$P5_0$–$P5_3$ (Note 4)	Single-chip	Input port P5	Input	Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz-crystal oscillator between X_{CIN} and X_{COUT}. If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin. Feedback resistor is connected between X_{CIN} and X_{COUT} pins.
	EPROM			Open.

Notes 1 : AV_{SS} for M37471M2/M4/M8/E4/E8-XXXFP.
2 : Only $P2_0$–$P2_3$ (IN_0–IN_3) 4-bit for the 7470 group.
3 : Only $P4_0$ and $P4_1$ 2-bit for the 7470 group.
4 : This port is not included in the 7470 group.

EPROM MODE

The M37470E4/E8, M37471E4/E8 feature an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 2 lists the correspondence between pins and Figure 30 to 32 give the pin connection in the EPROM mode. When in the EPROM mode, ports P0, P11–P17, P20–P23, P3, P40, P41, VREF are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the XIN and XOUT pins, or external clock should be connected to the XIN pin.

Table 2. Pin function in EPROM mode

	M37470E4/E8, M37471E4/E8	M5L27256
VCC	VCC	VCC
VPP	P33	VPP
VSS	VSS	VSS
Address input	Ports P11–P17, P20–P23, P30, P31, P40, P41	A0–A14
Data I/O	Port P0	D0–D7
$\overline{\text{CE}}$	VREF	$\overline{\text{CE}}$
$\overline{\text{OE}}$	P32	$\overline{\text{OE}}$

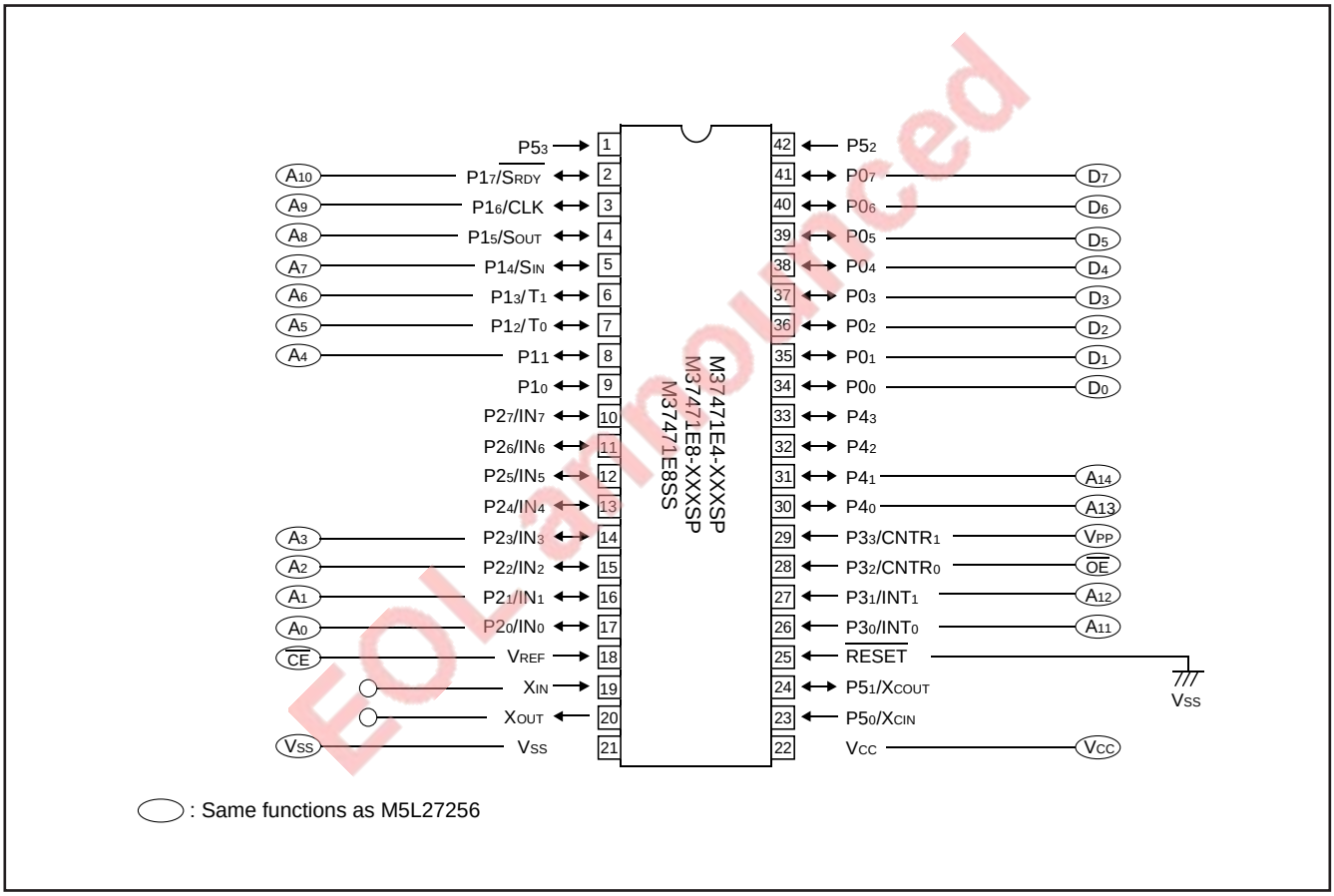


Fig. 28 Pin connection in EPROM mode

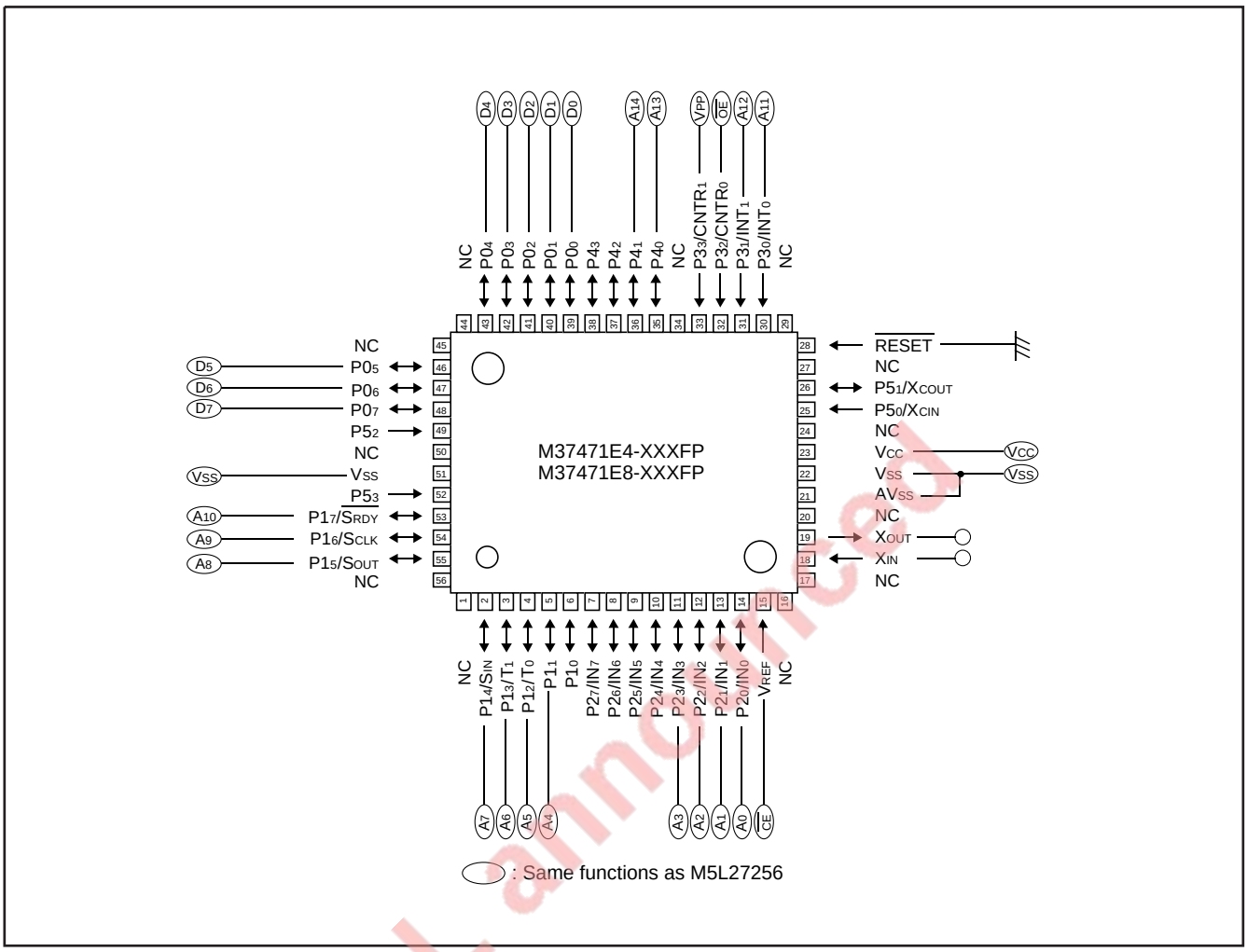


Fig. 29 Pin connection in EPROM mode

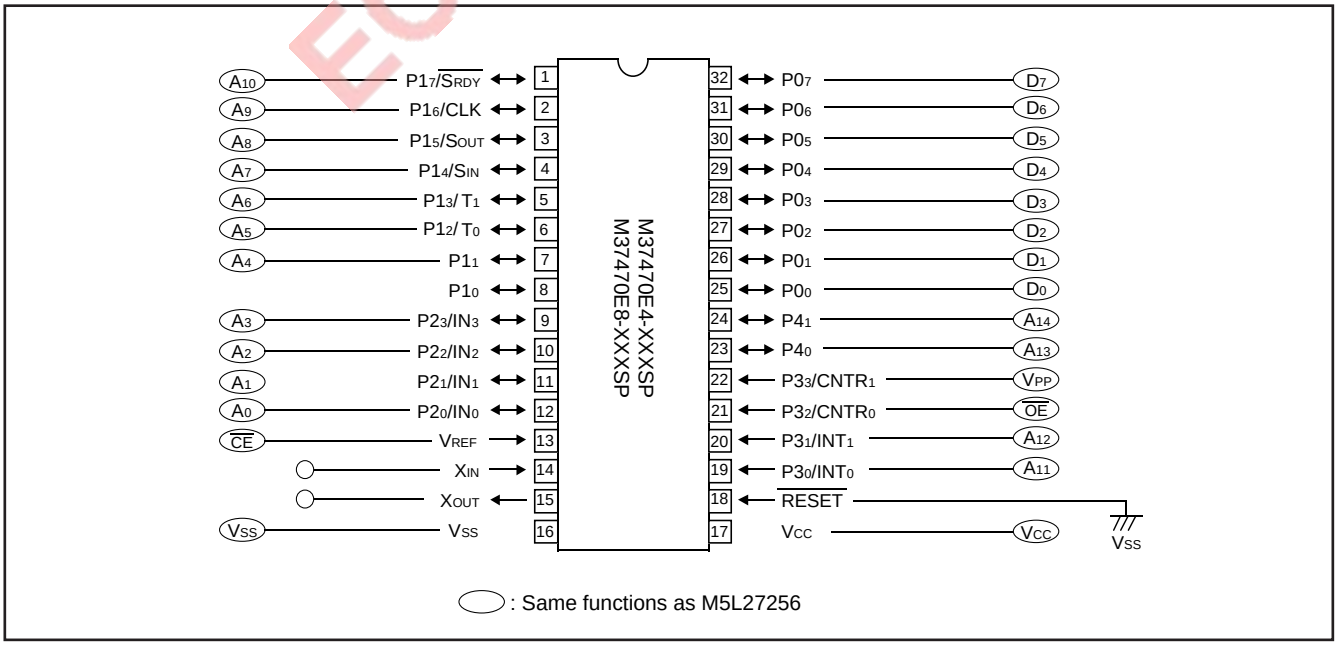


Fig. 30 Pin connection in EPROM mode

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to "L" level. Input the address of the data (A_0–A_{14}) to be read and the data will be output to the I/O pins (D_0–D_7). The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pin is in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0–A_{14}, and the data to be written is input to pins D_0–D_7. Set the $\overline{CE}$ pin to "L" level to begin writing.

Notes on Writing

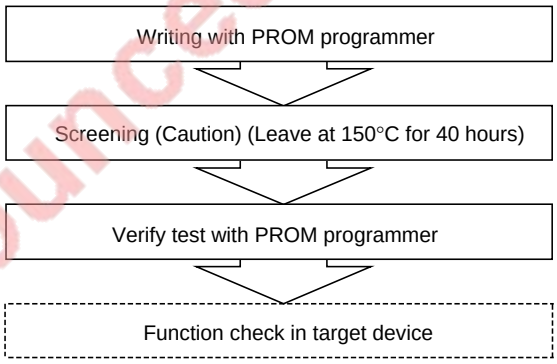
- M37470E4, M37471E4
  When using a PROM programmer, the address range should be between 6000_{16} and $7FFF_{16}$. Addresses 0000_{16} to $5FFF_{16}$ cannot be written to or read from correctly.
- M37470E8, M37471E8
  When using a PROM programmer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16}.

Erasing

Data can only erased on the M37471E8SS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is $15W \cdot s/cm^2$.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.
(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.
(3) Since a high voltage (12.5 V) is used to write data, care should be taken when turning on the PROM programmer's power.
(4) For the programmable microcomputer (shipped in One Time PROM version), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Caution : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 3. I/O signal in each mode

Pin / Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).
(2) The contents of the interrupt request bits are not modified immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.
(3) To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
(4) An NOP instruction must be used after the execution of a PLP instruction.
(5) Do not execute the STP instruction during A-D conversion.
(6) In the M37470, set bit 0, bit 1, and bit 3–bit 7 to "0" of the CPU mode register.
(7) Multiply/Divide instructions
The index X mode (T) and the decimal mode (D) flag do not affect the MUL and DIV instruction.
The execution of these instructions does not modify the contents of the processor status register.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3 sets

M37470M2/M4/M8-XXXSP, M37470E4/E8-XXXSP
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7	V
V_I	Input voltage X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_3$, $P4_0$, $P4_1$, V_{REF}, $\overline{RESET}$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$, X_{OUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = 25°C	1000	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X_{IN}) = 2.2V_{CC}–2.0 MHz	2.7		4.5	V
		f(X_{IN}) = 8 MHz	4.5	5	5.5	
V_{SS}	Power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$, $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$–$P2_3$, $P4_0$, $P4_1$		0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$–$P2_3$, $P4_0$, $P4_1$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$–$P0_7$, $P4_0$, $P4_1$				–30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_3$				–30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$–$P0_7$, $P4_0$, $P4_1$				60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_3$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$				–10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$ (Note 2)				–5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$ (Note 2)				10	mA
f(C_{NTR})	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 1)	f(X_{IN}) = 4 MHz			1	MHz
		f(X_{IN}) = 8 MHz			2	
f(C_{LK})	Serial I/O clock input frequency S_{CLK} ($P1_6$) (Note 1)	f(X_{IN}) = 4 MHz			1	MHz
		f(X_{IN}) = 8 MHz			2	
f(X_{IN})	Clock input oscillation frequency (Note 1)	V_{CC} = 2.7 to 4.5 V			2.2V_{CC} – 2.0	MHz
		V_{CC} = 4.5 to 5.5 V			8	

Notes 1 : Oscillation frequency is at 50% duty cycle.
2 : The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100 ms.

M37470M2/M4/M8-XXXSP, M37470E4/E8-XXXSP
ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P4$_0$, P4$_1$	V_{CC} = 5 V, I_{OH} = –5 mA		3			V
		V_{CC} = 3 V, I_{OH} = –1.5 mA		2			
V_{OL}	"L" output voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P4$_0$, P4$_1$	V_{CC} = 5 V, I_{OL} = 10 mA				2	V
		V_{CC} = 3 V, I_{OL} = 3 mA				1	
V_{T+} – V_{T-}	Hysteresis P0$_0$ – P0$_7$, P3$_0$ – P3$_3$	V_{CC} = 5 V			0.5		V
		V_{CC} = 3 V			0.3		
V_{T+} – V_{T-}	Hysteresis $\overline{\text{RESET}}$	V_{CC} = 5 V			0.5		V
		V_{CC} = 3 V			0.3		
V_{T+} – V_{T-}	Hysteresis P1$_6$/CLK	use as CLK input	V_{CC} = 5 V		0.5		V
			V_{CC} = 3 V		0.3		
I_{IL}	"L" input current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P3$_0$–P3$_2$, P4$_0$–P4$_1$	V_I = 0 V, not use pull-up transistor	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
		V_I = 0 V, use pull-up transistor	V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
			V_{CC} = 3 V	–0.08	–0.18	–0.35	
I_{IL}	"L" input current P3$_3$	V_I = 0 V	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
I_{IL}	"L" input current P2$_0$–P2$_3$	V_I = 0 V, not use as analog input, not use pull-up transistor	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
		V_I = 0 V, not use as analog input, use pull-up transistor	V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
			V_{CC} = 3 V	–0.08	–0.18	–0.35	
I_{IL}	"L" input current $\overline{\text{RESET}}$, X_{IN}	V_I = 0 V (X_{IN} is at stop mode)	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
I_{IH}	"H" input current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P3$_0$–P3$_2$, P4$_0$, P4$_1$	V_I = V_{CC}, not use pull-up transistor	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{IH}	"H" input current P3$_3$	V_I = V_{CC}	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{IH}	"H" input current P2$_0$–P2$_3$	V_I = V_{CC}, not use as analog input, not use pull-up transistor	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{IH}	"H" input current $\overline{\text{RESET}}$, X_{IN}	V_I = V_{CC}, (X_{IN} is at stop mode)	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{CC}	Power source current	At normal mode, A-D conversion is not executed.	f(X_{IN})=8 MHz, V_{CC} = 5 V		7	14	mA
			f(X_{IN})=4 MHz, V_{CC} = 5 V		3.5	7	
			f(X_{IN})=4 MHz, V_{CC} = 3 V		1.8	3.6	
		At normal mode, A-D conversion is executed.	f(X_{IN})=8 MHz, V_{CC} = 5 V		7.5	15	mA
			f(X_{IN})=4 MHz, V_{CC} = 5 V		4	8	
			f(X_{IN})=4 MHz, V_{CC} = 3 V		2	4	
		At wait mode.	f(X_{IN})=8 MHz, V_{CC} = 5 V		2	4	mA
			f(X_{IN})=4 MHz, V_{CC} = 5 V		1	2	
			f(X_{IN})=4 MHz, V_{CC} = 3 V		0.5	1	
		At stop mode, f(X_{IN})=0, V_{CC}=5 V	T_a = 25°C		0.1	1	µA
			T_a = 85°C		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2		5.5	V

A-D CONVERTER CHARACTERISTICS

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, f(X_{IN})=4 MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	bits
–	Non-linearity error				±2	LSB
–	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC} = V_{REF} = 5.12 V, I_{OL}(sum) = 0 mA			2	LSB
		V_{CC} = V_{REF} = 3.072 V, I_{OL}(sum) = 0 mA			3	
V_{FST}	Full-scale transition error	V_{CC} = V_{REF} = 5.12 V			4	LSB
		V_{CC} = V_{REF} = 3.072 V			7	
t_{CONV}	Conversion time	V_{CC} = 2.7 to 5.5 V, f(X_{IN}) = 4 MHz			25	µs
		V_{CC} = 4.5 to 5.5 V, f(X_{IN}) = 8 MHz			12.5	
V_{REF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

M37471M2/M4/M8-XXXSP/FP, M37471E4/E8-XXXSP/FP, M37471E8SS ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7	V
V_I	Input voltage X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_3$, V_{REF}, $\overline{RESET}$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$, X_{OUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = 25°C	1000 (Note 1)	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 150	°C

Note 1 : 500 mW for M37471M2/M4/M8-XXXFP.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85°C unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X_{IN}) = 2.2V_{CC} – 2.0 MHz	2.7		4.5	V
		f(X_{IN}) = 8 MHz	4.5	5	5.5	
V_{SS}	Power source voltage			0		V
AV_{SS}	Analog power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$, $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$–$P2_7$, $P4_0$–$P4_3$, $P5_0$–$P5_3$ (Note 1)		0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$–$P2_7$, $P4_0$–$P4_3$, $P5_0$–$P5_3$ (Note 1)		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$–$P0_7$, $P4_0$–$P4_3$				– 30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_7$				– 30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$–$P0_7$, $P4_0$–$P4_3$				60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_7$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$				– 10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$ (Note 2)				– 5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$ (Note 2)				10	mA
f(C_{NTR})	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 3)	f(X_{IN}) = 4 MHz			1	MHz
		f(X_{IN}) = 8 MHz			2	
f(C_{LK})	Serial I/O clock input frequency S_{CLK} ($P1_6$) (Note 3)	f(X_{IN}) = 4 MHz			1	MHz
		f(X_{IN}) = 8 MHz			2	
f(X_{IN})	Main clock input oscillation frequency (Note 3)	V_{CC} = 2.7 to 4.5 V			2.2V_{CC} – 2.0	MHz
		V_{CC} = 4.5 to 5.5 V			8	
f(X_{CIN})	Sub-clock input oscillation frequency for clock function (Note 3, 4)			32	50	kHz

Notes 1 : It is except to use $P5_0$ as X_{CIN}.
2 : The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100 ms.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the clock oscillation frequency for clock function should be f(X_{CIN}) < f(X_{IN}) / 3.

M37471M2/M4/M8-XXXSP/FP, M37471E4/E8-XXXSP/FP, M37471E8SS
ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage P0₀–P0₇, P1₀–P1₇, P2₀–P2₇, P4₀–P4₃	V_{CC} = 5 V, I_{OH} = –5 mA		3			V
		V_{CC} = 3 V, I_{OH} = –1.5 mA		2			
V_{OL}	"L" output voltage P0₀–P0₇, P1₀–P1₇, P2₀–P2₇, P4₀–P4₃	V_{CC} = 5 V, I_{OL} = 10 mA				2	V
		V_{CC} = 3 V, I_{OL} = 3 mA				1	
V_{T+} – V_{T-}	Hysteresis P0₀–P0₇, P3₀–P3₃	V_{CC} = 5 V			0.5		V
		V_{CC} = 3 V			0.3		
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 5 V			0.5		V
		V_{CC} = 3 V			0.3		
V_{T+} – V_{T-}	Hysteresis P1₆/CLK	used as CLK input	V_{CC} = 5 V		0.5		V
			V_{CC} = 3 V		0.3		
I_{IL}	"L" input current P0₀–P0₇, P1₀–P1₇, P3₀–P3₂, P4₀–P4₃, P5₀–P5₃	V_I = 0 V, not use pull-up transistor	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
		V_I = 0 V, use pull-up transistor	V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
			V_{CC} = 3 V	–0.08	–0.18	–0.35	
I_{IL}	"L" input current P3₃	V_I = 0 V	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
I_{IL}	"L" input current P2₀–P2₇	V_I = 0 V, not use as analog input, not use pull-up transistor	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
		V_I = 0 V, not use as analog input, use pull-up transistor	V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
			V_{CC} = 3 V	–0.08	–0.18	–0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I = 0 V (X_{IN} is at stop mode)	V_{CC} = 5 V			–5	µA
			V_{CC} = 3 V			–3	
I_{IH}	"H" input current P0₀–P0₇, P1₀–P1₇, P3₀–P3₂, P4₀–P4₃, P5₀–P5₃	V_I = V_{CC}, not use pull-up transistor	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{IH}	"H" input current P3₃	V_I = V_{CC}	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{IH}	"H" input current P2₀–P2₇	V_I = V_{CC}, not use as analog input, not use pull-up transistor	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I = V_{CC}, (X_{IN} is at stop mode)	V_{CC} = 5 V			5	µA
			V_{CC} = 3 V			3	
I_{CC}	Power source current	At normal mode, A-D conversion is not executed.	f(X_{IN})=8 MHz, V_{CC} = 5 V		7	14	mA
			f(X_{IN})=4 MHz, V_{CC} = 5 V		3.5	7	
			V_{CC} = 3 V		1.8	3.6	
		At normal mode, A-D conversion is executed.	f(X_{IN})=8 MHz, V_{CC} = 5 V		7.5	15	mA
			f(X_{IN})=4 MHz, V_{CC} = 5 V		4	8	
			V_{CC} = 3 V		2	4	
		At low-speed mode, T_a=25°C, f(X_{IN})=0, f(X_{CIN})=32 kHz, X_{COUT} drive capacity is low, A-D conversion is not executed.	V_{CC} = 5 V		30	80	µA
			V_{CC} = 3 V		15	40	
		At wait mode.	f(X_{IN})=8 MHz, V_{CC} = 5 V		2	4	mA
			f(X_{IN})=4 MHz, V_{CC} = 5 V		1	2	
			V_{CC} = 3 V		0.5	1	
		At wait mode, X_{IN} = 0 Hz, X_{CIN} = 32 kHz, X_{COUT} is low-power mode, T_a=25°C	V_{CC} = 5 V		3	12	µA
			V_{CC} = 3 V		2	8	
		Stop all oscillation V_{CC} = 5 V	T_a = 25°C		0.1	1	
			T_a = 85°C		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS

(V_{CC} = 2.7 to 5.5 V, V_{SS} =AV_{SS}= 0 V, T_a = –20 to 85°C, f(X_{IN}) = 4 MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	bits
–	Non-linearity error				±2	LSB
–	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC} = V_{REF} = 5.12 V, I_{OL}(sum) = 0 mA			2	LSB
		V_{CC} = V_{REF} = 3.072 V, I_{OL}(sum) = 0 mA			3	
V_{FST}	Full-scale transition error	V_{CC} = V_{REF} = 5.12 V			4	LSB
		V_{CC} = V_{REF} = 3.072 V			7	
t_{CONV}	Conversion time	V_{CC} = 2.7 to 5.5 V, f(X_{IN}) = 4 MHz			25	µs
		V_{CC} = 4.5 to 5.5 V, f(X_{IN}) = 8 MHz			12.5	
V_{REF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

7470/7471 Group

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