Product Features

- Using external 32.768kHz quartz crystal
- Supports I^2C-Bus's high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Operating range: 1.8V to 5.5V

Ordering Information

Part Number	Package
PT7C4337PE	Lead free 8-Pin DIP
PT7C4337WE	Lead free 8-Pin SOIC
PT7C4337UE	Lead free 8-Pin MSOP

Product Description

The PT7C4337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output.

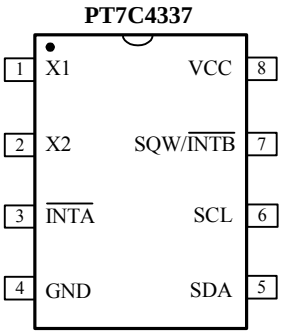
Address and data are transferred serially via a 2-wire, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

Table 1 shows the basic functions of PT7C4337. More details are shown in section: overview of functions.

Table 1. Basic functions of PT7C4337

Item	Function			PT7C4337
1	Oscillator	Source	Crystal: 32.768kHz	√
			External input	√
		Oscillator enable/disable		√
		Oscillator fail detect		√
2	Time	Time display	12-hour	√
			24-hour	√
		Century bit		√
3	Alarm interrupt			√ 2
4	Programmable square wave output (Hz)			1, 4.096k, 8.192k, 32.768k

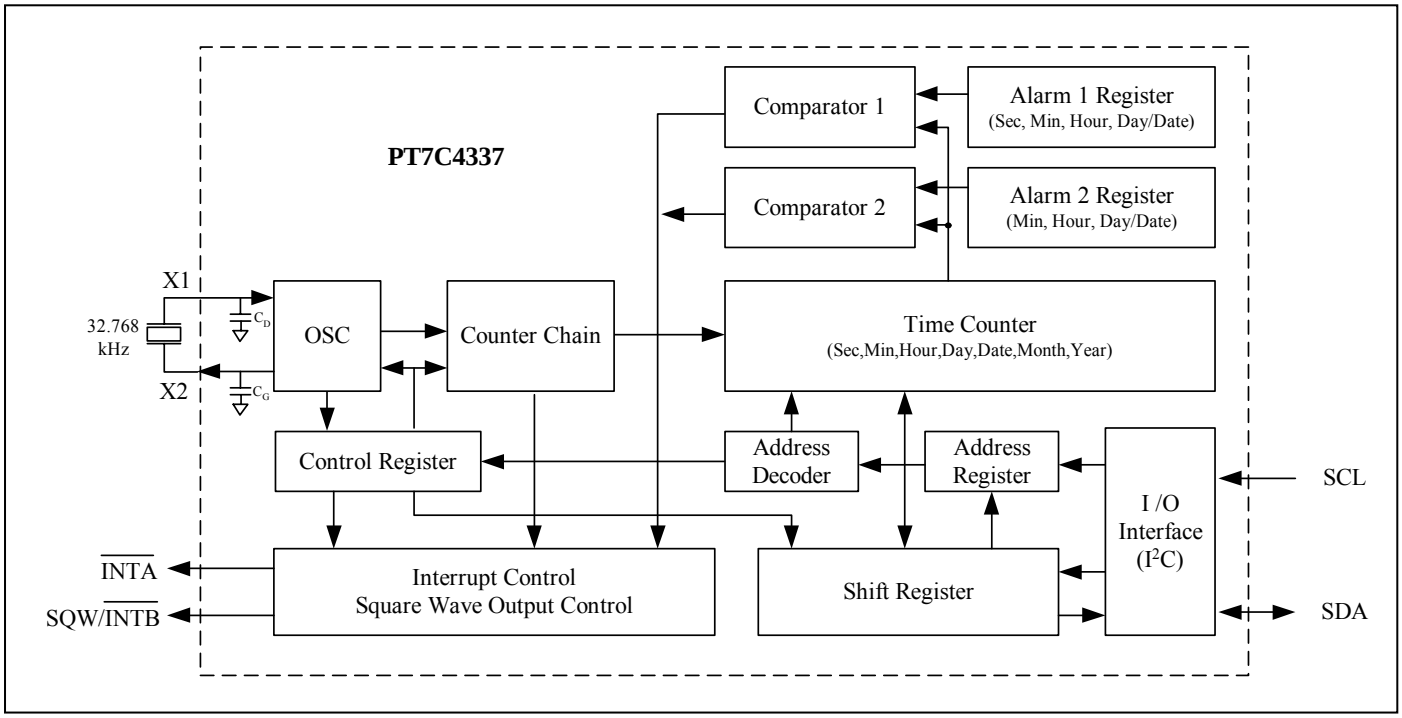
Pin Assignment



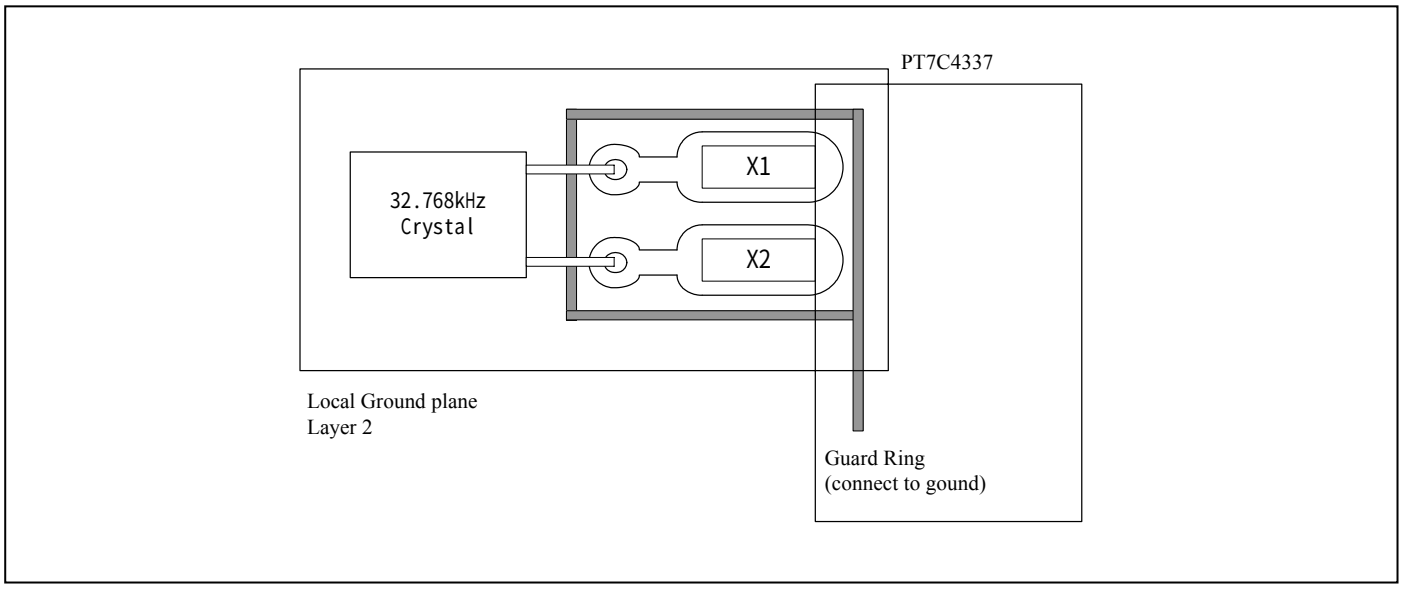
Pin Description

Pin no.	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them. Or external clock input.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
3	$\overline{\text{INTA}}$	O	**Interrupt Output.** When enabled, $\overline{\text{INTA}}$ is asserted low when the time matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull up resistor.
7	SQW/$\overline{\text{INTB}}$	O	**Square-Wave/Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor.
8	VCC	P	**Power.**
4	GND	P	**Ground.**

Function Block



Recommended Layout for Crystal



Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	45	kΩ
Load Capacitance	C_L	-	12.5	-	pF

The crystal, traces and crystal input pins should be isolated from RF generating signals.

Function Description

Overview of Functions

Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

Alarm function

This device has two alarm system (Alarm 1 and Alarm 2) that outputs interrupt signals from INTA or INTB to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

Oscillator fail detect

When oscillator fail, PT7C4337 OSF bit will be set.

Oscillator enable/disable

Oscillator and time count chain can be enabled or disabled at the same time by /ETIME bit.

Registers

Allocation of registers

Addr. (hex)[*1]	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	Century	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Alarm 1: Seconds	A1M1[*2]	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2[*2]	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3[*2]	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4[*2]	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2[*3]	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3[*3]	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4[*3]	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/ETIME[*4]	0	0	RS2[*5]	RS1[*5]	INTCN[*6]	A2IE[*7]	A1IE[*7]
0F	Status	OSF[*9]	0	0	0	0	0	A2F[*8]	A1F[*8]

Caution points:
*1. PT7C4337 uses 8 bits for address. For excess 0FH address, PT7C4337 will not respond (no acknowledge signal was given).
*2. Alarm 1 mask bits. Select alarm repeated rate when an alarm occurs.
*3. Alarm 2 mask bits. Select alarm repeated rate when an alarm occurs.
*4. Oscillator and time count chain enable/disable bit.
*5. Square wave output frequency select.
*6. Interrupt output pin select bit.
*7. Alarm 1 and alarm 2 enable bits.
*8. Alarm 1 and alarm 2 flag bits.
*9. Oscillator stop flag.
*10. All bits marked with "0" are read-only bits. Their value when read is always "0".

Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
0E	Control	/ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
	(default)	0	0	0	1	1	0	0	0
0F	Status	OSF	0	0	0	0	0	A2F	A1F
	(default)	1	0	0	0	0	0	Undefined	Undefined

Oscillator related bits

- **/ETIME**

Enable oscillator and time count chain bit.

/ETIME	Data	Description
Read / Write	0	Enable oscillator and time count chain. Default
	1	Disable oscillator and time count chain.

- **OSF**

Oscillator Stop Flag.

A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC is insufficient to support oscillation.
3) The /ETIME bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Square wave frequency selection bits

- **RS2, RS1**

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

RS2, RS1	Data	SQW output freq. (Hz)
Read / Write	00	1
	01	4.096k
	10	8.192k
	11	32.768k Default

Interrupt related bits

- **INTCN**

Interrupt Output pin select bit. This bit controls the relationship between the two alarms and the interrupt output pins.

INTCN	Data	Description
Read / Write	1	A match between the timekeeping registers and the alarm 1 registers activates the $\overline{\text{INTA}}$ pin (if the alarm 1 is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{\text{INTB}}$ pin (if the alarm 2 is enabled).
	0	A match between the timekeeping registers and either alarm 1 or alarm 2 registers activates the $\overline{\text{INTA}}$ pin (if the alarms are enabled). In this configuration, a square wave is output on the SQW/$\overline{\text{INTB}}$ pin. Default

- **A1IE**

Alarm 1 Interrupt Enable.

A1IE	Data	Description
Read / Write	0	The A1F bit does not initiate the $\overline{\text{INTA}}$ signal. Default
	1	Permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{\text{INTA}}$.

- **A1F**

Alarm 1 Flag.

A1F	Data	Description
Read / Write	0	The time do not match the alarm 1 registers. Default
Read	1	Indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the $\overline{\text{INTA}}$ pin goes low. A1F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

- **A2IE**

Alarm 2 Interrupt Enable.

A2IE	Data	Description
Read / Write	0	The A2F bit does not initiate an interrupt signal. Default
	1	Permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{\text{INTA}}$ (when INTCN = 0) or to assert SQW/$\overline{\text{INTB}}$ (when INTCN = 1).

- **A2F**

Alarm 2 Flag.

A1F	Data	Description
Read / Write	0	The time do not match the alarm 2 registers. Default
Read	1	Indicates that the time matched the alarm 1 registers. This flag can be used to generate an interrupt on either $\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$ depending on the status of the INTCN bit. If the INTCN = 0 and A2F = 1 (and A2IE = 1), the $\overline{\text{INTA}}$ pin goes low. If the INTCN = 1 and A2F = 1 (and A2IE = 1), the SQW/$\overline{\text{INTB}}$ pin goes low. A2F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
02	Hours	0	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced with correct time, otherwise it will cause the clock counter malfunction.

- **12, /24 bit**

This bit is used to select between 12-hour clock system and 24-hour clock system.

12, /24	Data	Description
Read / Write	0	24-hour system
	1	12-hour system

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register
0	24-hour time display	
1	12-hour time display	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	52 (AM 12)	12	72 (PM 12)
01	41 (AM 01)	13	61 (PM 01)
02	42 (AM 02)	14	62 (PM 02)
03	43 (AM 03)	15	63 (PM 03)
04	44 (AM 04)	16	64 (PM 04)
05	45 (AM 05)	17	65 (PM 05)
06	46 (AM 06)	18	66 (PM 06)
07	47 (AM 07)	19	67 (PM 07)
08	48 (AM 08)	20	68 (PM 08)
09	49 (AM 09)	21	69 (PM 09)
10	50 (AM 10)	22	70 (PM 10)
11	51 (AM 11)	23	71 (PM 11)

***** Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

Days of the week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
05	Months	Century*1	0	0	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1:** The century bit is toggled when the years register overflows from 99 to 00.

Alarm Register

- **Alarm 1, Alarm 2 Register**

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Alarm 1: Seconds	A1M1*1	S40	S20	S10	S8	S4	S2	S1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
08	Alarm 1: Minutes	A1M2*1	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
09	Alarm 1: Hours	A1M3*1	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm 1: Day, Date	A1M4*1	Day, /Date*1	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm 2: Minutes	A2M2*2	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm 2: Hours	A2M3*2	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0D	Alarm 2: Day, Date	A2M4*2	Day, /Date*2	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1** Note: Alarm mask bit, using to select Alarm 1 alarm rate.

***2** Note: Alarm mask bit, using to select Alarm 2 alarm rate.

Alarm Function

Related register

Addr. (hex)	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
02	Hours	0	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
03	Days of the week	0	0	0	0	0	W4	W2	W1
04	Dates	0	0	D20	D10	D8	D4	D2	D1
07	Alarm 1: Seconds	A1M1	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0B	Alarm 2: Minutes	A2M2	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4	Day, /Date	0, D20	0, D10	0, D8	W4, D4	W2, D2	W1, D1
0E	Control	/ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
0F	Status	OSF	0	0	0	0	0	A2F	A1F

Note: Alarm function does not support different hour system adopted in time and alarm register.

The PT7C4337 contains two time-of-day/date alarms. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes - each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits.
When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h ~ 04h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 and Table 3 shows the possible settings.

The Day, /Date bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 ~ 5 of that register reflects the day of the week or the date of the month. If the bit is written to logic 0, the alarm is the result of a match with date of the month. If the bit is written to logic 1, the alarm is the result of a match with day of the week.

When the PT7C4337 register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$) signals. The match is tested on the once-per-second update of the time and date registers.

Table 1. Alarm 1 Mask Bits

Day, /Date	Alarm 1 register mask bits				Alarm rate
	A1M4	A1M3	A1M2	A1M1	
×	1	1	1	1	Alarm once per second
×	1	1	1	0	Alarm when seconds match
×	1	1	0	0	Alarm when minutes and seconds match
×	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
Others					Ignored.

Table 2. Alarm 2 Mask Bits

Day, /Date	Alarm 2 register mask bits			Alarm rate
	A2M4	A2M3	A2M2	
×	1	1	1	Alarm once per minute (00 seconds of every minute)
×	1	1	0	Alarm when minutes match
×	1	0	0	Alarm when hours, minutes
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match
Others				Ignored.

I²C Bus Interface

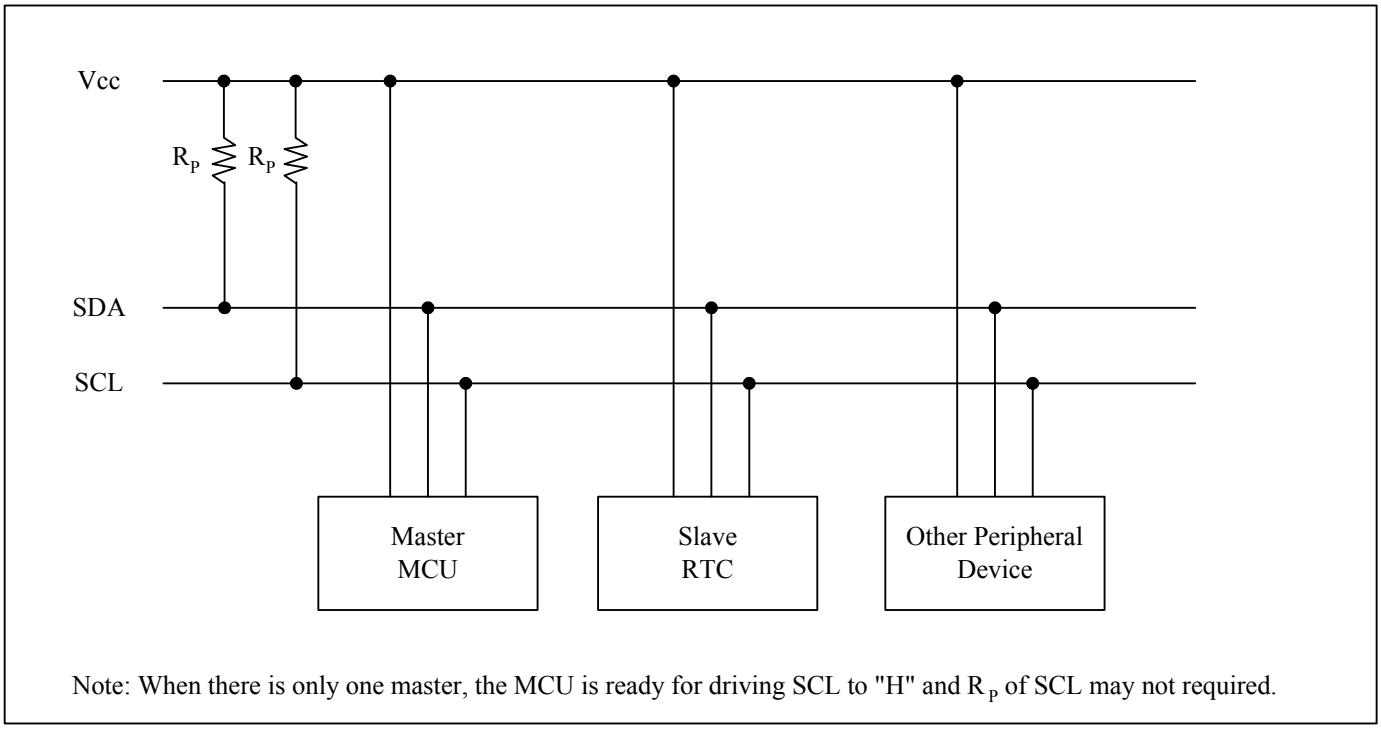
Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

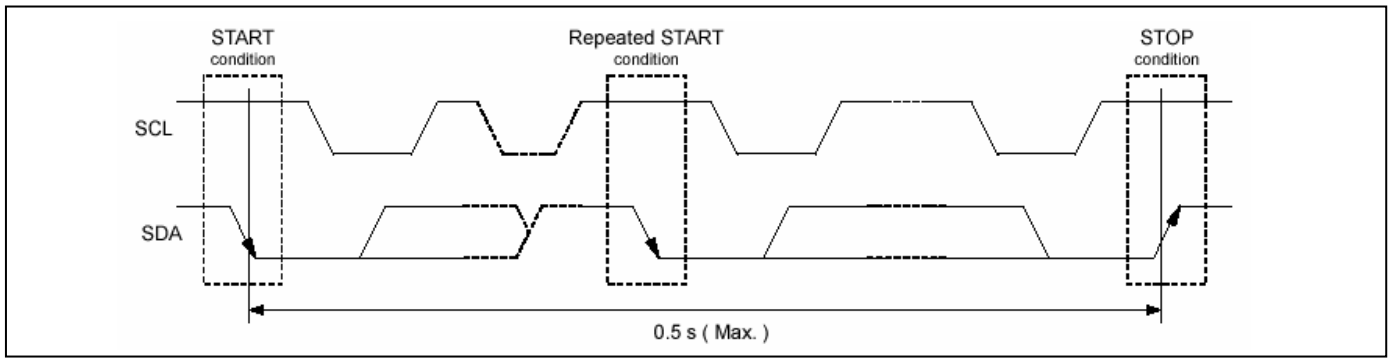
Fig 1. System configuration



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_P of SCL may not required.

Starting and Stopping I²C Bus Communications

Fig 2. Starting and stopping on I²C bus



1) START condition, repeated START condition, and STOP condition

a) START condition
SDA level changes from high to low while SCL is at high level

b) STOP condition
SDA level changes from low to high while SCL is at high level

c) Repeated START condition (RESTART condition)
In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

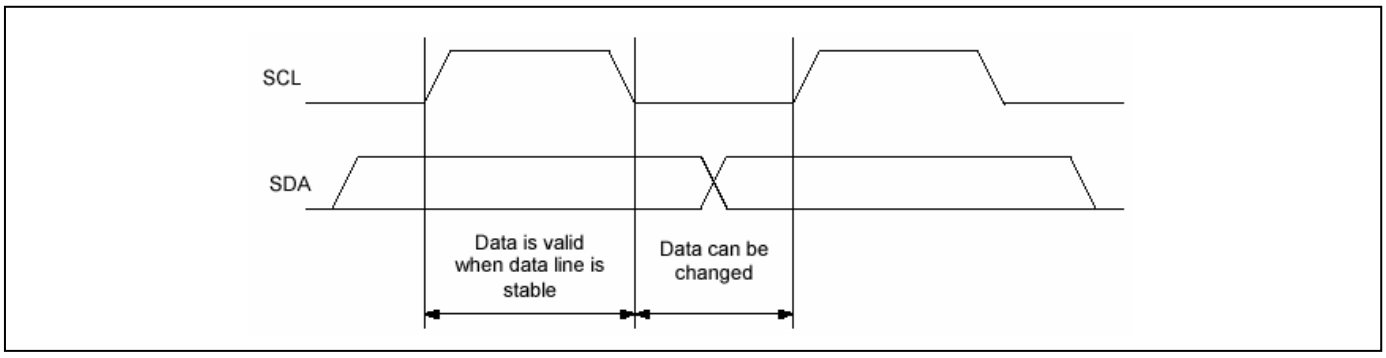
2) Data Transfers and Acknowledge Responses during I²C-BUS Communication

a) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

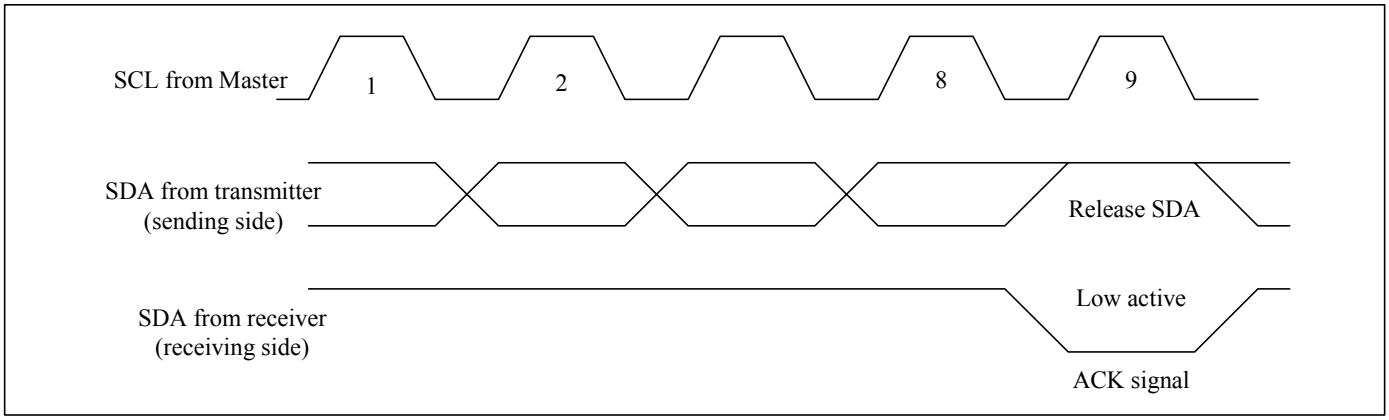


*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

b) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

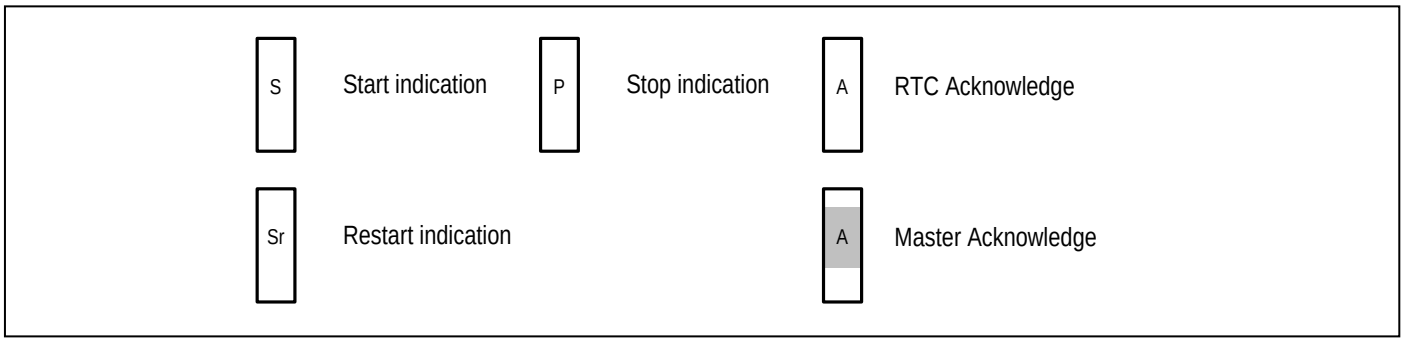
Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/$\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.
Slave addresses have a fixed length of 7 bits. See table for the details.
An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

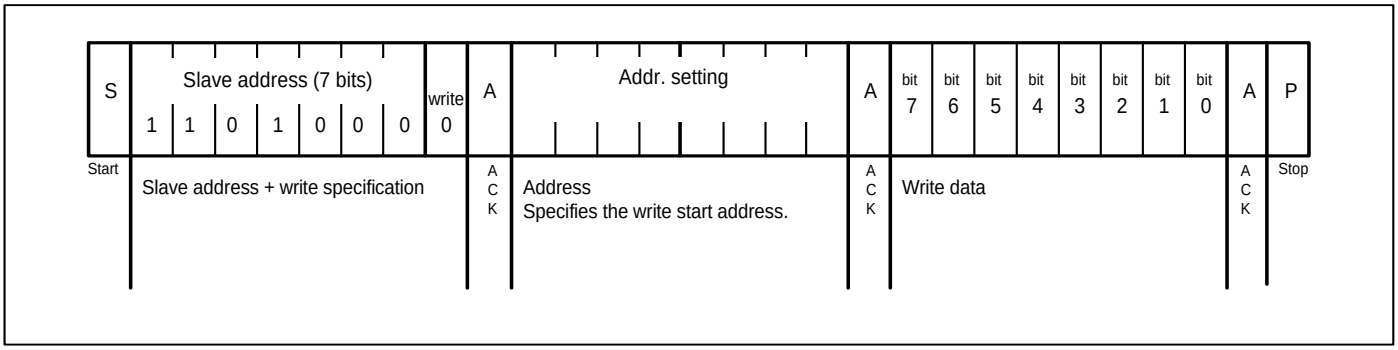
Table

Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h								0 (= Write)

I²C Bus's Basic Transfer Format

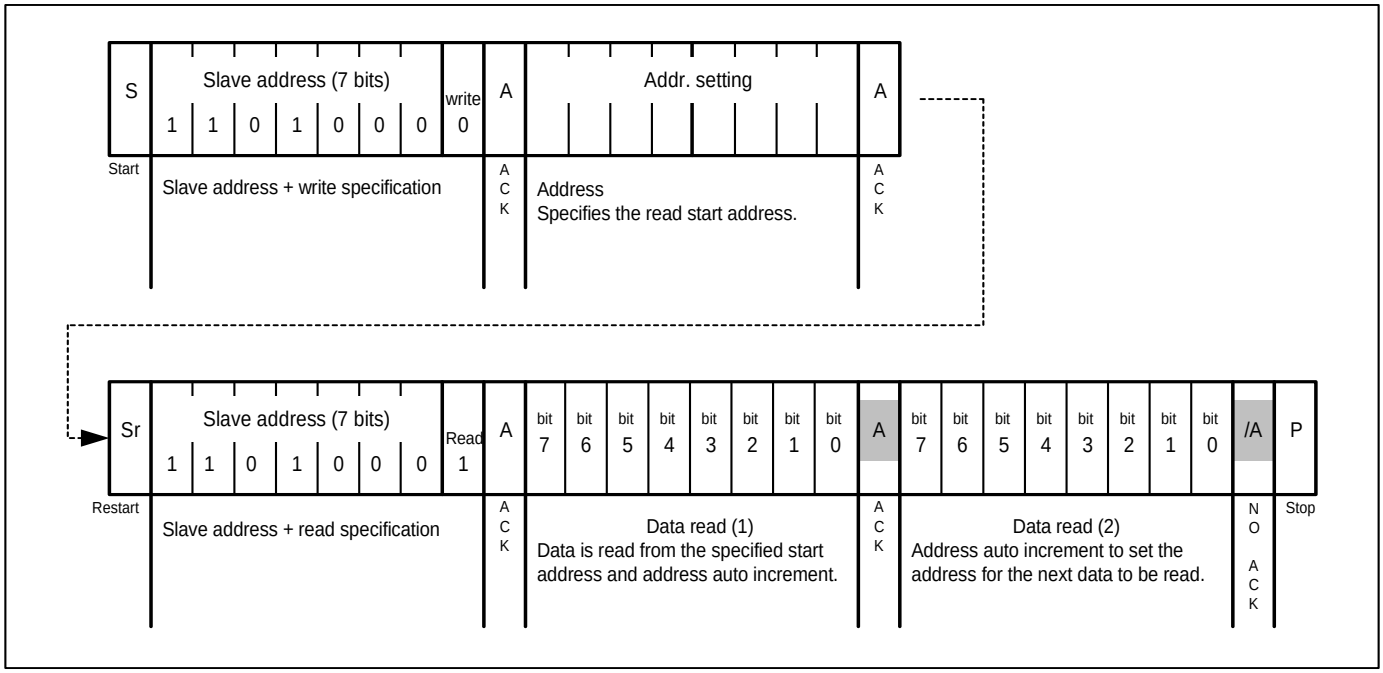


1) Write via I²C bus

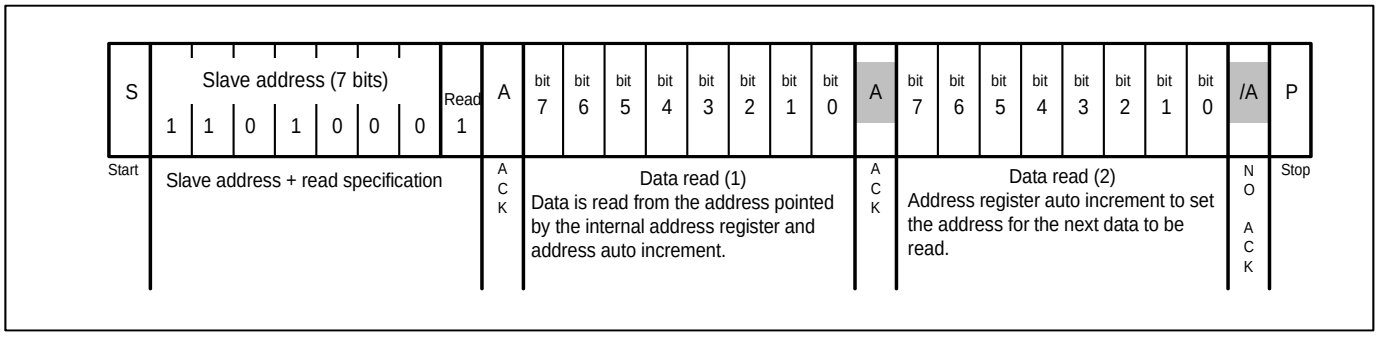


2) Read via I²C bus

a) Standard read



b) Simplified read



Note:

1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to (V_{cc}+0.3V)
DC Output Voltage (SDA, /INTA, /INTB pins)	-0.3V to +6.5V
DC Output Current (FOUT)	-0.3V to (V_{cc}+0.3V)
Power Dissipation	320mW (depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Part No.	Symbol	Description		Min	Type	Max	Unit
PT7C4337	V_{CC}	Power voltage		1.8	-	5.5	V
	V_{OSC}	Oscillator voltage		1.7	-	5.5	
	V_{IH}	Input high level	SCL, SDA	$0.7V_{CC}$	-	V_{CC}+0.3	
			$\overline{INTA}$, SQW/$\overline{INTB}$	-	-	5.5	
	V_{IL}	Input low level		-0.3	-	$0.3V_{CC}$	
	T_A	Operating temperature		-40	-	85	ºC

DC Electrical Characteristics

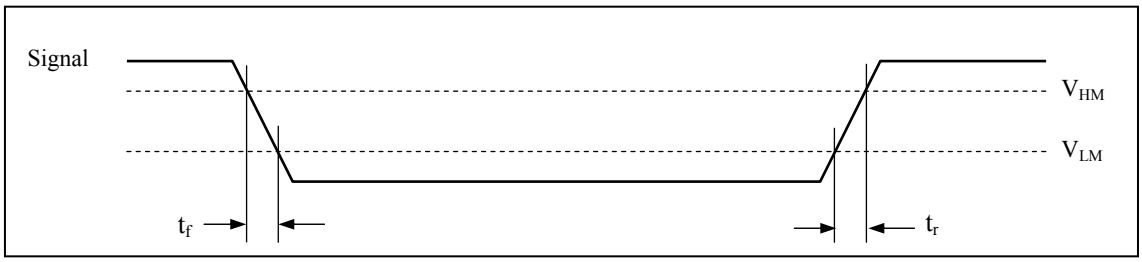
Unless otherwise specified, V_{CC} = 1.8~5.5V, T_A = -40 °C to +85 °C

Sym.	Item	Pin	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage	V_{CC}		1.8	-	5.5	V
V_{OSC}	Oscillator voltage	V_{CC}		1.7	-	5.5	V
I_{CC}	Active supply current	V_{CC}	Note 1, 5	-	-	150	µA
	Standby current	V_{CC}	Note 2, 3, 5	-	0.5	0.8	
	Timekeeping current	V_{CC}	Note 2, 4, 5	-	350	600	nA
	Data retention current	V_{CC}	Note 2, 6	-	-	150	
V_{IL1}	Low-level input voltage	SCL		-0.3	-	$0.3V_{CC}$	V
V_{IH1}	High-level input voltage	SCL		$0.7V_{CC}$	-	V_{CC}+0.3	
V_{IL2}	Low-level input voltage	X1		-	0.53	-	V
V_{IH2}	High-level input voltage	X1		-	0.53	-	
I_{OL}	Low-level output current	SDA, /INTA, /INTB	V_{OL} = 0.4V	-	-	3	mA
I_{IL}	Input leakage current	SCL		-	-	1	µA
I_{OZ}	Output current when OFF	SDA, /INTA, /INTB		-	-	1	µA

Note:
1. SCL clocking at max frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = VCC.
2. Specified with 2-wire bus inactive, V_{IL} = 0.0V, V_{IH} = VCC.
3. SQW enabled.
4. Specified with the SQW function disabled by setting INTCN = 1.
5. Using recommended crystal on X1 and X2.
6. Crystal oscillator is disabled.

AC Electrical Characteristics

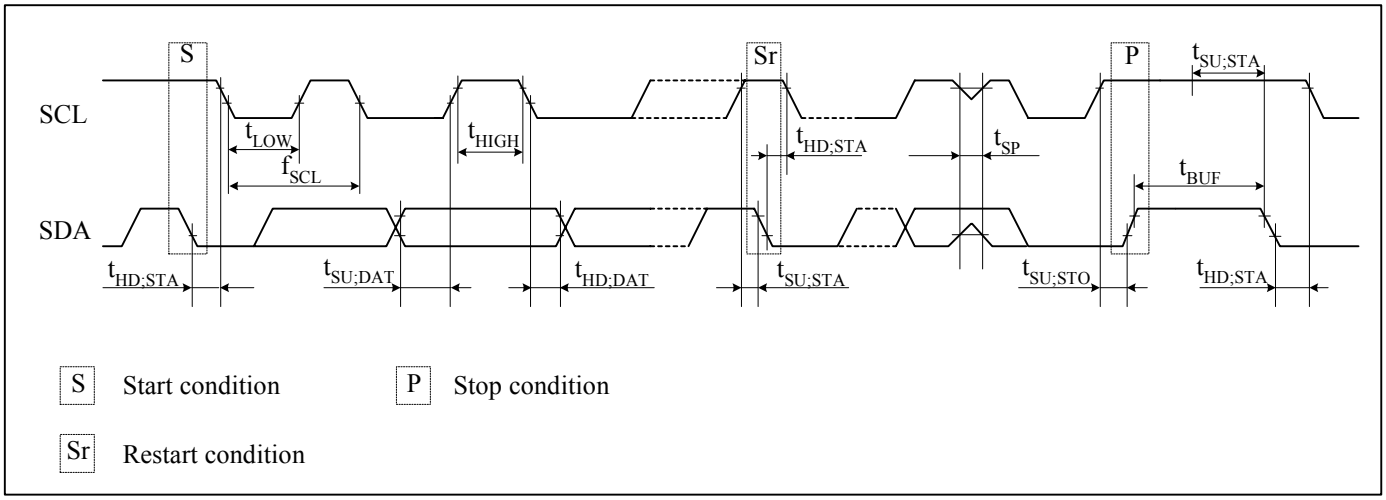
Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



Over the operating range

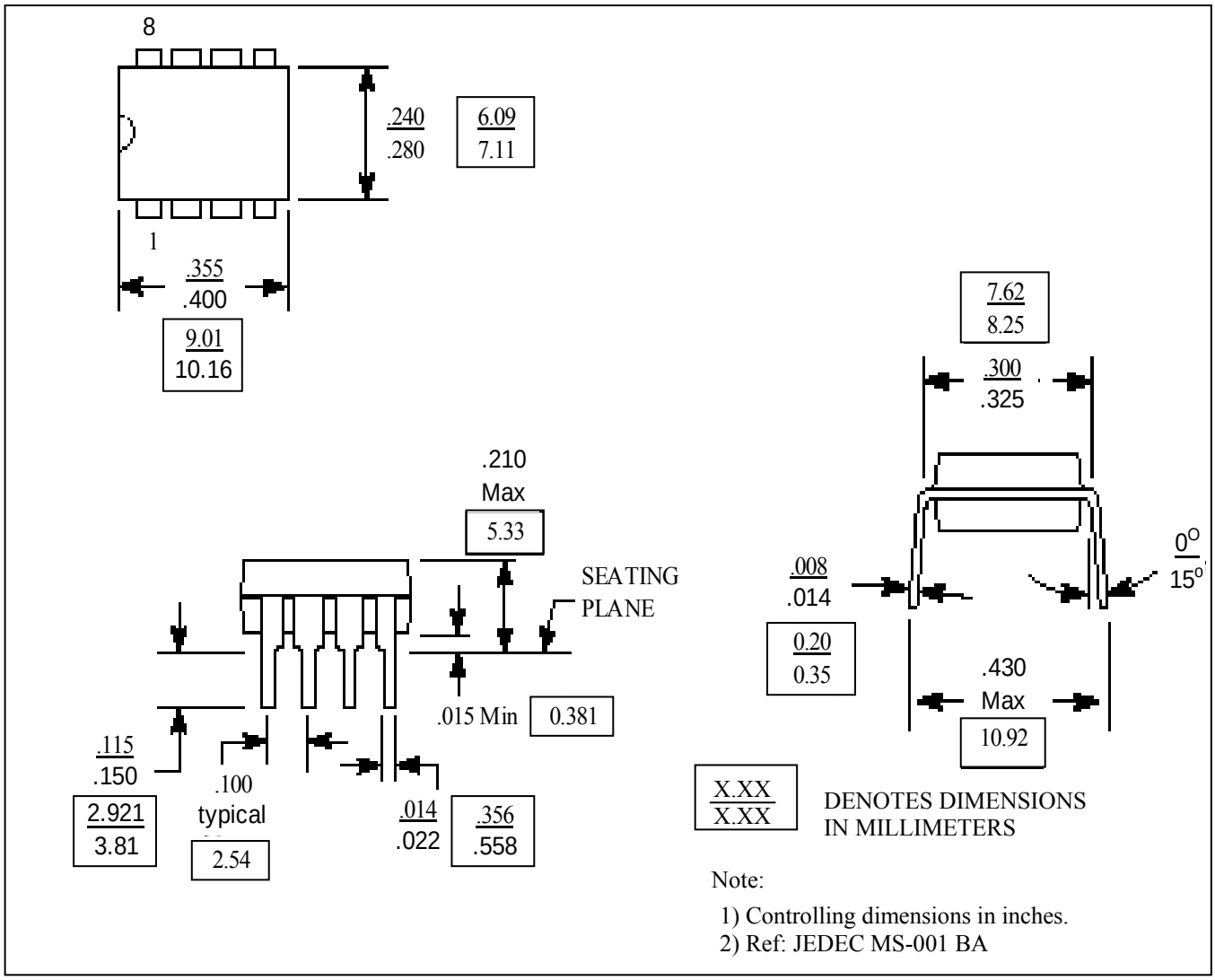
Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency			400	kHz
$t_{SU;STA}$	START condition set-up time	0.6			µs
$t_{HD;STA}$	START condition hold time	0.6			µs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200			ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35			ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0			µs
$t_{SU;STO}$	STOP condition setup time	0.6			µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3			µs
t_{LOW}	When SCL = "L"	1.3			µs
t_{HIGH}	When SCL = "H"	0.6			µs
t_r	Rise time for SCL and SDA			0.3	µs
t_f	Fall time for SCL and SDA			0.3	µs
t_{SP}*	Allowable spike time on bus			50	ns
C_B	Capacitance load for each bus line			400	pF

*** Note:** only reference for design



Mechanical Information

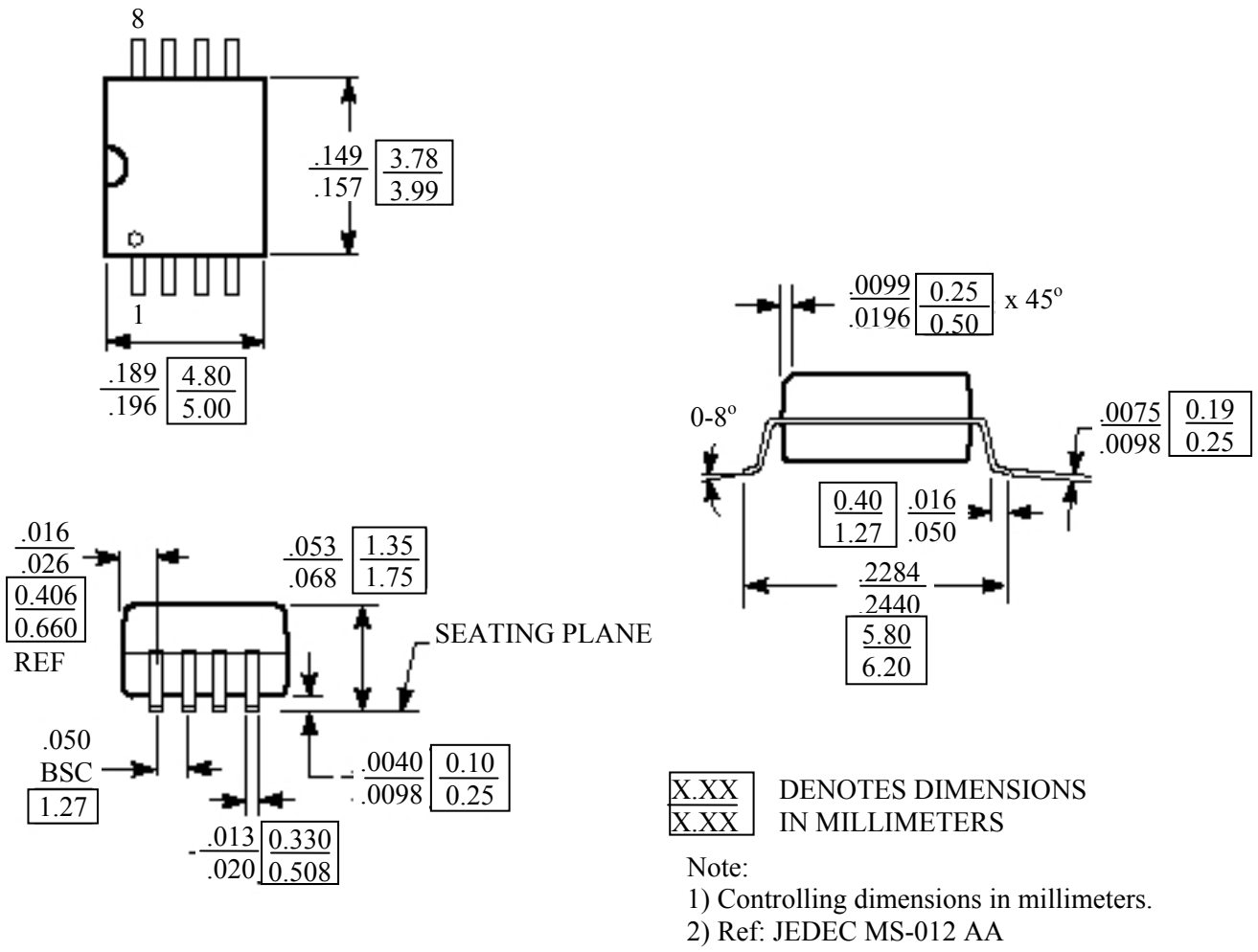
PE (Lead free DIP-8)



Note:

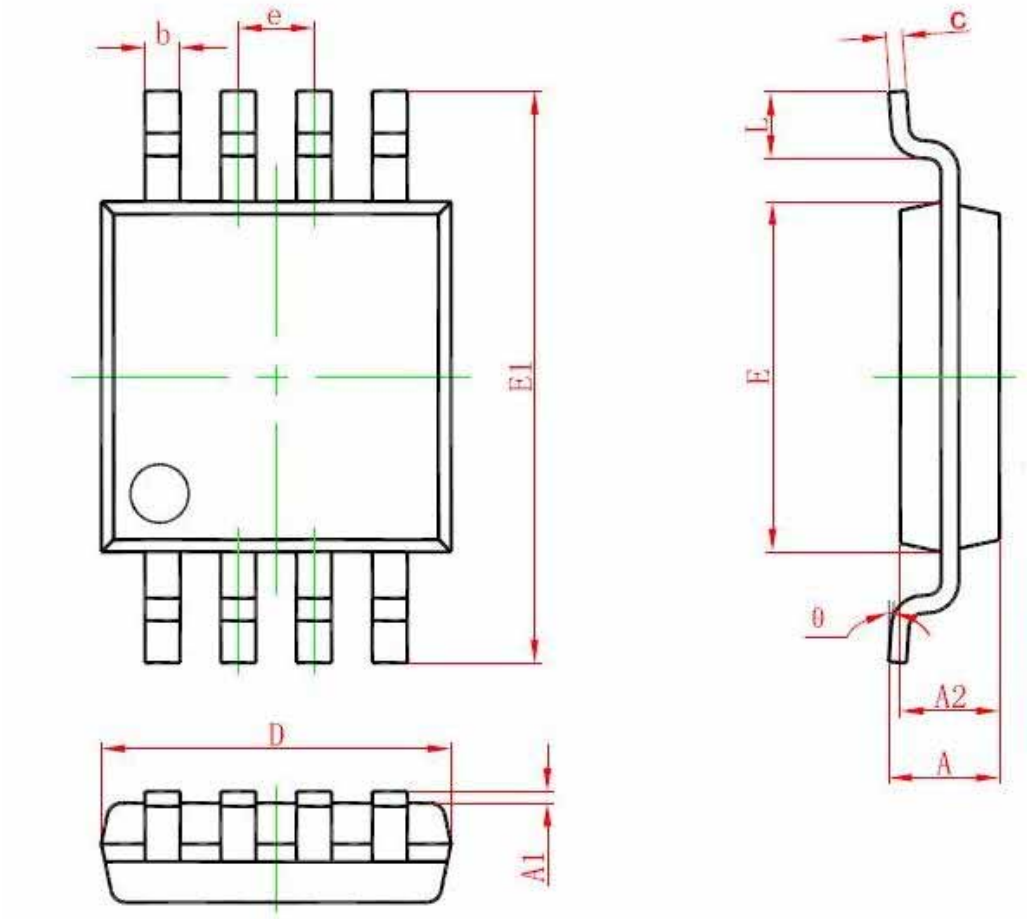
1) Controlling dimensions in inches.
2) Ref: JEDEC MS-001 BA

WE (Lead free SOIC-8)



Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012 AA

UE(Lead free MSOP-8)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Notes

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