



## P-CHANNEL MOSFET

Qualified per **MIL-PRF-19500/564**

Qualified Levels:  
JAN, JANTX, JANTXV  
and JANS

### DESCRIPTION

This 2N6849 switching transistor is military qualified up to the JANS level for high-reliability applications. This device is also available in a low profile U surface mount package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

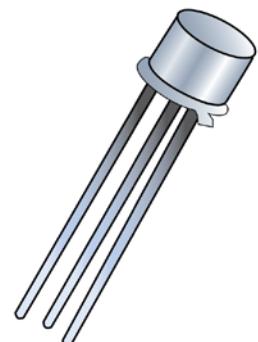
**Important:** For the latest information, visit our website <http://www.microsemi.com>.

### FEATURES

- JEDEC registered 2N6849 number.
- JAN, JANTX, JANTXV and JANS qualifications are available per MIL-PRF-19500/564.  
(See [part nomenclature](#) for all available options.)
- RoHS compliant versions available (commercial grade only).

### APPLICATIONS / BENEFITS

- Lightweight top-hat design with flexible terminals offers a variety of mounting flexibility.
- Military and other high-reliability applications.



**TO-205AF (TO-39)  
Package**

Also available in:

**U-18 LCC package**  
(surface mount)  
 [2N6849U](#)

### MAXIMUM RATINGS @ $T_A = +25^\circ\text{C}$ unless otherwise stated

Parameters / Test Conditions	Symbol	Value	Unit
Operating & Storage Junction Temperature Range	$T_J$ & $T_{stg}$	-55 to +150	°C
Thermal Resistance Junction-to-Case	$R_{eJC}$	5.0	°C/W
Total Power Dissipation @ $T_A = +25^\circ\text{C}$ @ $T_C = +25^\circ\text{C}$ <sup>(1)</sup>	$P_T$	0.8 25	W
Drain-Source Voltage, dc	$V_{DS}$	-100	V
Gate-Source Voltage, dc	$V_{GS}$	± 20	V
Drain Current, dc @ $T_C = +25^\circ\text{C}$ <sup>(2)</sup>	$I_{D1}$	-6.5	A
Drain Current, dc @ $T_C = +100^\circ\text{C}$ <sup>(2)</sup>	$I_{D2}$	-4.1	A
Off-State Current (Peak Total Value) <sup>(3)</sup>	$I_{DM}$	-25	A (pk)
Source Current	$I_S$	-6.5	A

**Notes:** 1. Derate linearly 0.2 W/°C for  $T_C > +25^\circ\text{C}$ .

2. The following formula derives the maximum theoretical  $I_D$  limit.  $I_D$  is also limited by package and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_J(\text{max}) - T_C}{R_{eJC} \times R_{DS(on)} @ T_J(\text{max})}}$$

3.  $I_{DM} = 4 \times I_{D1}$  as calculated in note 2.

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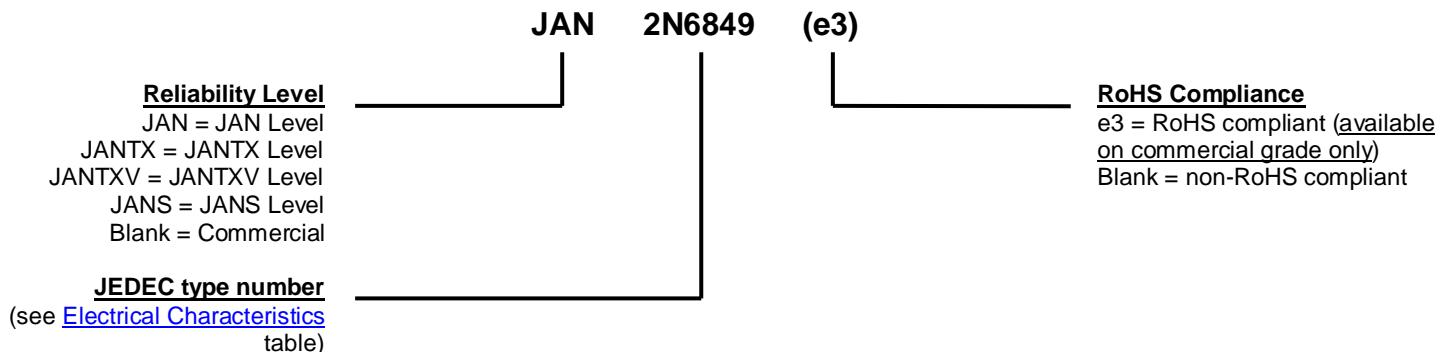
#### Website:

[www.microsemi.com](http://www.microsemi.com)

### MECHANICAL and PACKAGING

- CASE: Hermetically sealed, kovar base, nickel cap.
- TERMINALS: Tin/lead solder dip nickel plate or RoHS compliant pure tin plate (commercial grade only).
- MARKING: Part number, date code, manufacturer's ID.
- WEIGHT: Approximately 1.064 grams.
- See [Package Dimensions](#) on last page.

### PART NOMENCLATURE



### SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I <sub>F</sub>	Forward current
R <sub>G</sub>	Gate drive impedance
V <sub>DD</sub>	Drain supply voltage
V <sub>DS</sub>	Drain source voltage, dc
V <sub>GS</sub>	Gate source voltage, dc

**ELECTRICAL CHARACTERISTICS @  $T_A = +25^\circ\text{C}$ , unless otherwise noted**

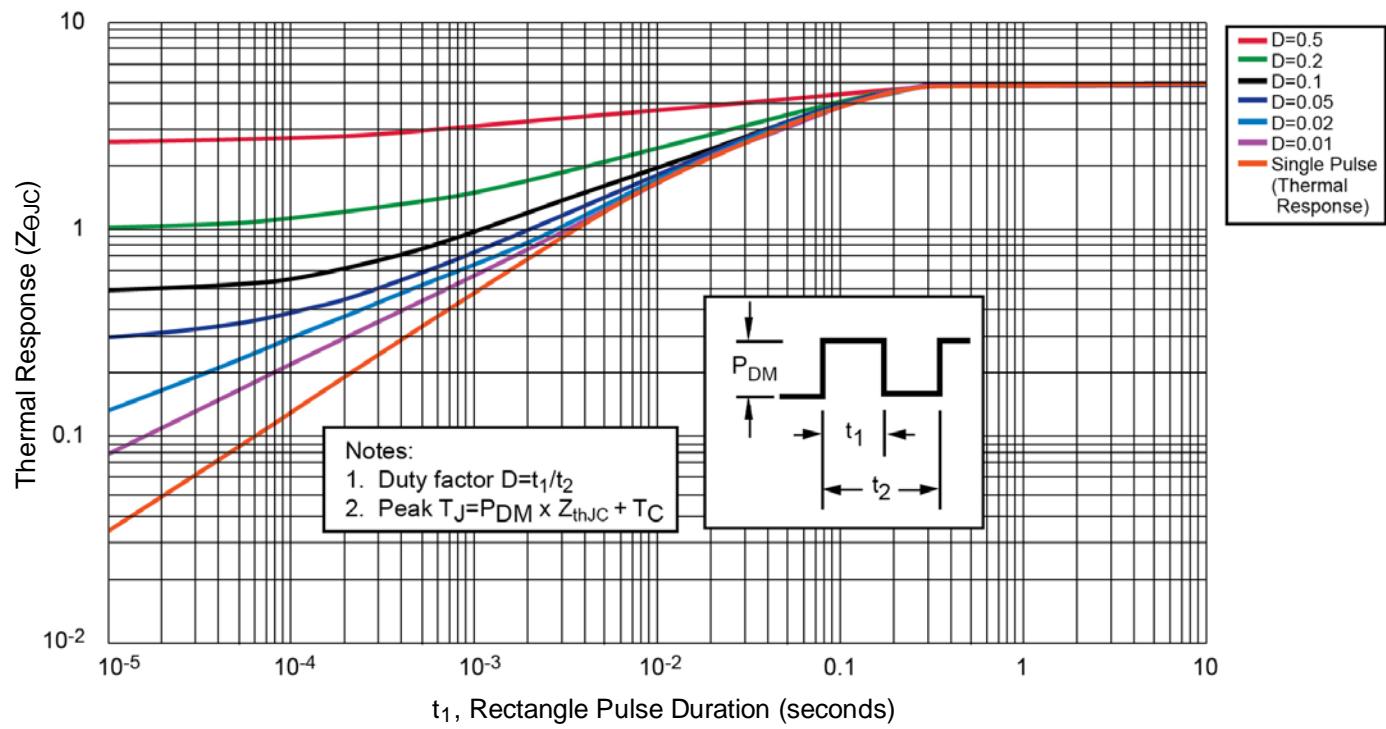
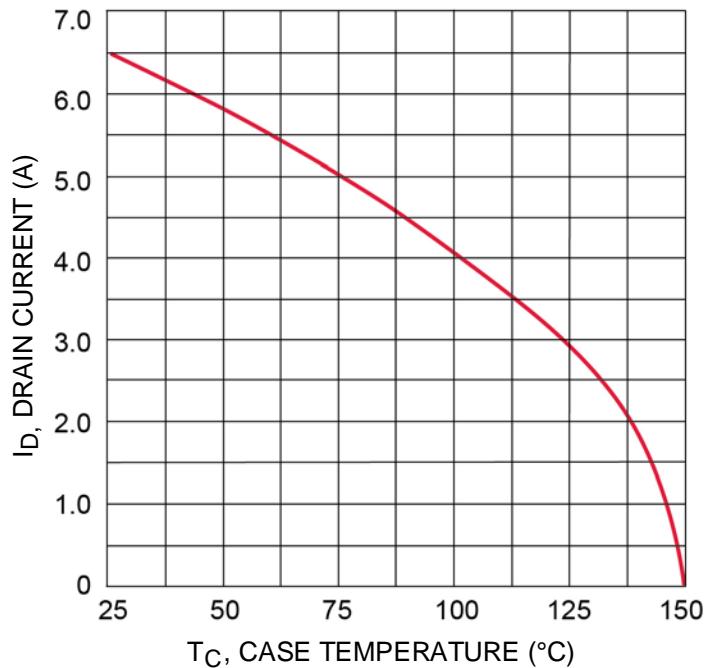
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>OFF CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}$ , $I_D = -1.0\text{ mA}$	$V_{(BR)DSS}$	-100		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}$ , $I_D = -0.25\text{ mA}$ $V_{DS} \geq V_{GS}$ , $I_D = -0.25\text{ mA}$ , $T_J = +125^\circ\text{C}$ $V_{DS} \geq V_{GS}$ , $I_D = -0.25\text{ mA}$ , $T_J = -55^\circ\text{C}$	$V_{GS(\text{th})1}$ $V_{GS(\text{th})2}$ $V_{GS(\text{th})3}$	-2.0 -1.0 -5.0	-4.0	V
Gate Current $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ , $T_J = +125^\circ\text{C}$	$I_{GSS1}$ $I_{GSS2}$		$\pm 100$ $\pm 200$	nA
Drain Current $V_{GS} = 0\text{ V}$ , $V_{DS} = -80\text{ V}$	$I_{DSS1}$		-25	$\mu\text{A}$
Drain Current $V_{GS} = 0\text{ V}$ , $V_{DS} = -80\text{ V}$ , $T_J = +125^\circ\text{C}$	$I_{DSS2}$		-0.25	mA
Static Drain-Source On-State Resistance $V_{GS} = -10\text{ V}$ , $I_D = -4.1\text{ A}$ pulsed	$r_{DS(\text{on})1}$		0.30	$\Omega$
Static Drain-Source On-State Resistance $V_{GS} = -10\text{ V}$ , $I_D = -6.5\text{ A}$ pulsed	$r_{DS(\text{on})2}$		0.32	$\Omega$
Static Drain-Source On-State Resistance $T_J = +125^\circ\text{C}$ $V_{GS} = -10\text{ V}$ , $I_D = -4.1\text{ A}$ pulsed	$r_{DS(\text{on})3}$		0.54	$\Omega$
Diode Forward Voltage $V_{GS} = 0\text{ V}$ , $I_D = -6.5\text{ A}$ pulsed	$V_{SD}$		-4.3	V

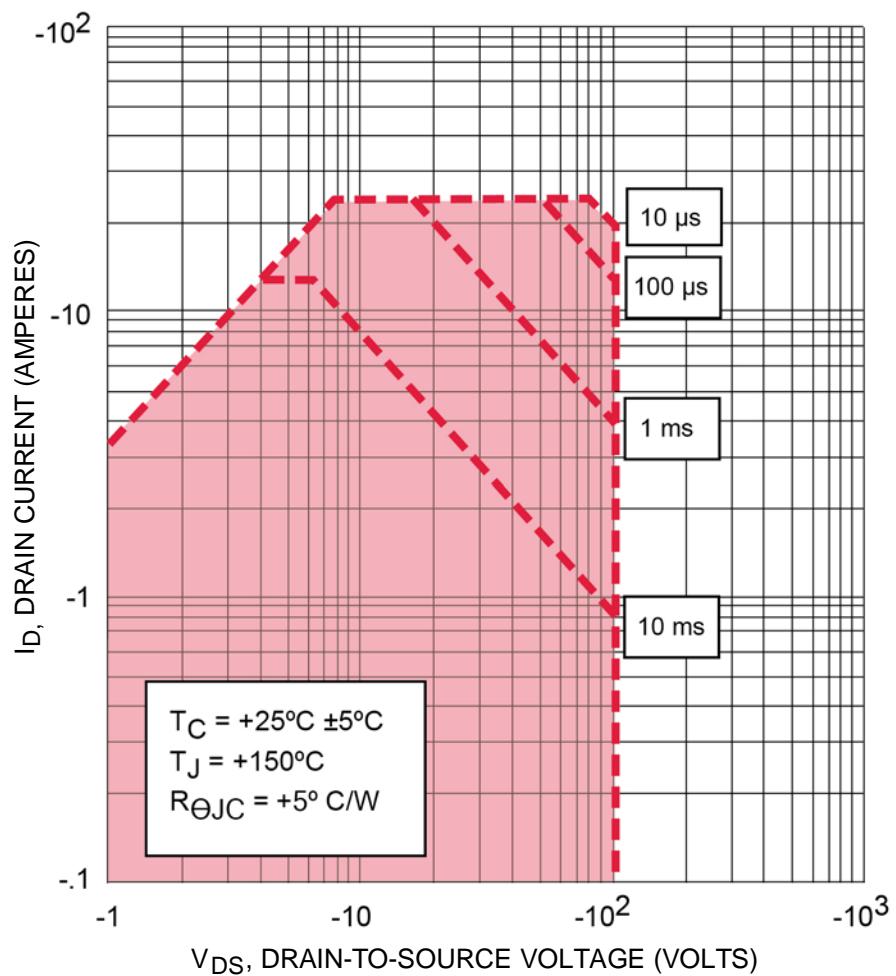
**DYNAMIC CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Gate Charge:	$Q_{g(\text{on})}$			
On-State Gate Charge $V_{GS} = -10\text{ V}$ , $I_D = -6.5\text{ A}$ , $V_{DS} = -50\text{ V}$			34.8	nC
Gate to Source Charge $V_{GS} = -10\text{ V}$ , $I_D = -6.5\text{ A}$ , $V_{DS} = -50\text{ V}$	$Q_{gs}$		6.8	nC
Gate to Drain Charge $V_{GS} = -10\text{ V}$ , $I_D = -6.5\text{ A}$ , $V_{DS} = -50\text{ V}$	$Q_{gd}$		23.1	nC

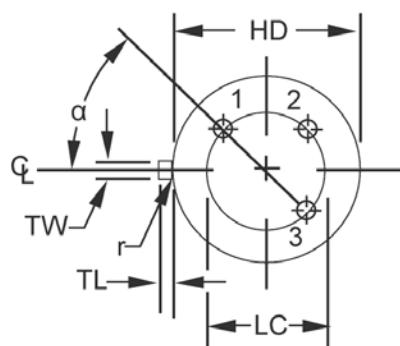
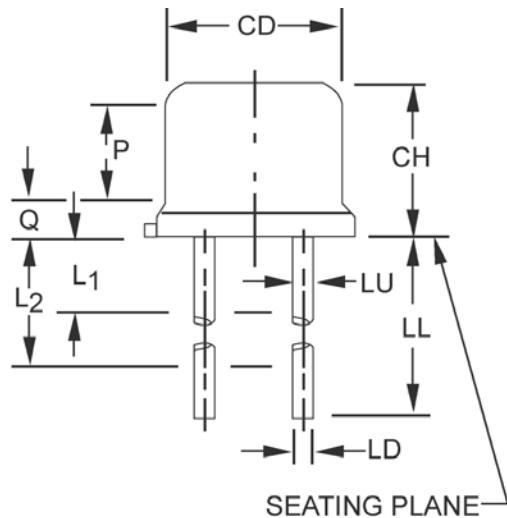
**ELECTRICAL CHARACTERISTICS @  $T_A = +25^\circ\text{C}$ , unless otherwise noted (continued)**
**SWITCHING CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-on delay time $I_D = -6.5 \text{ A}$ , $V_{GS} = -10 \text{ V}$ , $R_G = 7.5 \Omega$ , $V_{DD} = -40 \text{ V}$	$t_{d(on)}$		60	ns
Rinse time $I_D = -6.5 \text{ A}$ , $V_{GS} = -10 \text{ V}$ , $R_G = 7.5 \Omega$ , $V_{DD} = -40 \text{ V}$	$t_r$		140	ns
Turn-off delay time $I_D = -6.5 \text{ A}$ , $V_{GS} = -10 \text{ V}$ , $R_G = 7.5 \Omega$ , $V_{DD} = -40 \text{ V}$	$t_{d(off)}$		140	ns
Fall time $I_D = -6.5 \text{ A}$ , $V_{GS} = -10 \text{ V}$ , $R_G = 7.5 \Omega$ , $V_{DD} = -40 \text{ V}$	$t_f$		140	ns
Diode Reverse Recovery Time $di/dt \leq -100 \text{ A}/\mu\text{s}$ , $V_{DD} \leq -50 \text{ V}$ , $I_F = -6.5 \text{ A}$	$t_{rr}$		250	ns

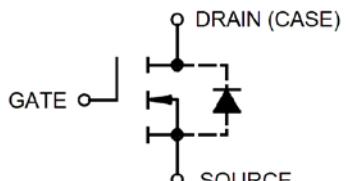
**GRAPHS**

**FIGURE 1 – Normalized Transient Thermal Impedance**

**FIGURE 2 – Maximum Drain Current vs Case Temperature**

**GRAPHS (continued)**


**FIGURE 3 – Maximum Safe Operating Area**

**PACKAGE DIMENSIONS**


Symbol	Dimensions				Note	
	Inch		Millimeters			
	Min	Max	Min	Max		
CD	0.305	0.335	7.75	8.51		
CH	0.160	0.180	4.07	4.57		
HD	0.335	0.370	8.51	9.39		
LC	0.200 TP		5.08 TP		6	
LD	0.016	0.021	0.41	0.53	7, 8	
LL	0.500	0.750	12.70	19.05	7, 8	
LU	0.016	0.019	0.41	0.48	7, 8	
L1	-	0.050	-	1.27	7, 8	
L2	0.250	-	6.35	-	7, 8	
P	0.100	-	2.54	-	5	
Q	-	0.050	-	1.27	4	
TL	0.029	0.045	0.74	1.14	3	
TW	0.028	0.034	0.72	0.86	2	
r	-	0.010	-	0.25	9	
$\alpha$	45° TP		45° TP		6	


**Schematic**
**NOTES:**

1. Dimensions are in inches. Millimeters are given for general information only.
2. Beyond radius (r) maximum, TW shall be held for a minimum length of 0.011 (0.028 mm).
3. Dimension TL measured from maximum HD.
4. Outline in this zone is not controlled.
5. Dimension CD shall not vary more than 0.010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane 0.054 +0.001, -0.000 (1.37 +0.03, -0.00 mm) below seating plane shall be within 0.007 (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. LU applies between L1 and L2. LD applies between L2 and LL minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. All three leads.
9. Radius (r) applies to both inside corners of tab.
10. Drain is electrically connected to the case.
11. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.
12. Lead 1 = source, lead 2 = gate, lead 3 = drain.