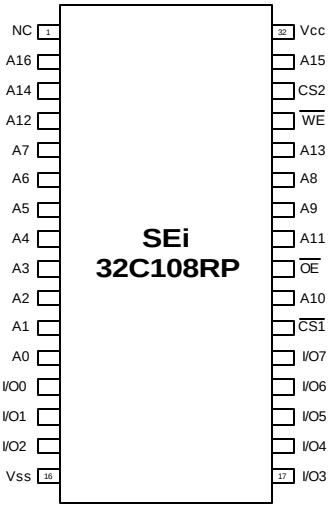
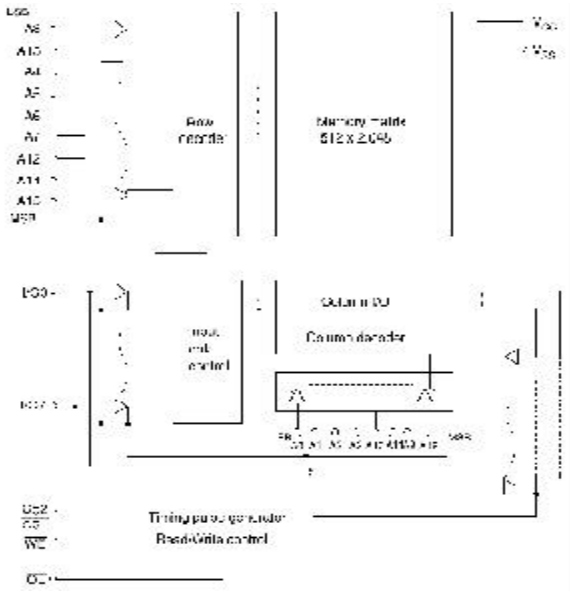
32C108RP

RADIATION HARDENED 1 MEGABIT CMOS SRAM





FEATURES:

- Total dose hardness typical 100 krad (Si); dependent upon orbit
- Package:
  - 32-pin RAD-PAK® DIP
  - 32-pin RAD-PAK® flat pack
- Fast propagation time:
  - 55 ns maximum access time standard
- Completely static memory
  - No clock or timing strobe required
- High-speed 0.8 micron CMOS technology
  - Single 5-volt power supply
  - Equal access and cycle times
  - All inputs and outputs are directly TTL compatible
  - Low-power:
    - standby: 10 uW typical
    - operation: 75 mW/MHz typical
  - Capable of battery backup operation

DESCRIPTION:

Space Electronics' 32C108RP (RP for RAD-PAK®) high-density 1 megabit SRAM microcircuit features a typical 100 kilorad (Si) total dose tolerance; dependent upon orbit. Using SEi's radiation-hardened RAD-PAK® packaging technology, the 32C108RP realizes higher density, higher performance and lower power consumption by employing 0.8 micron Bi-CMOS process technology. The 32C108RP is fully suitable for battery back-up systems since it offers low-power standby power dissipation. Capable of surviving space environments, the 32C108RP is ideal for satellite, spacecraft, and space probe missions. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. The 32C108RP features the same advanced 128k x 8 SRAM, high-speed, and low-power demand as the commercial counterpart. This product is available with packaging and screening up to Class S.

32C108RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	-0.5	7.0	V
Voltage on Any Pin, Relative to V_{SS}	V_T	-0.5	V_{CC} +0.3	V
Power Dissipation	P_D		1.0	W
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-55	+125	°C

32C108RP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage, Positive	V_{CC}	4.5	5.5	V
Supply Voltage, Negative	V_{SS}	0	0	V
Input High Voltage	V_{IH}	2.2	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V

32C108RP AC ELECTRICAL CHARACTERISTICS - WRITE

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Cycle Time	t_{WC}	55		ns
Chip Selection to End of Write	t_{CW}	50		ns
Address Setup Time	t_{AS}	0		ns
Address Valid to End of Write	t_{AW}	50		ns
Write Pulse Width	t_{WP}	40		ns
Write Recovery Time[1]	t_{WR}	5 10		ns ns[1]
Write to Output in High-Z[2]	t_{WHZ}	0	15	ns
Data to Write Time Overlap	t_{DW}	25		ns
Write Hold from Write Time	t_{DH}	0		ns
Output Active from End of Write[2]	t_{OW}	5		ns

Notes:
1. This value is measured from CS2 going low to the end of write cycle.
2. Guaranteed by design.

32C108RP DC ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	$V_{IN}=V_{SS}$ to V_{CC}	I_{LI}	-2	2	uA
Output Leakage Current	CS1\ = V_{IH} or CS2=V_{IL}, OE\ = V_{IH} or WE=V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	I_{LO}	-2	2	uA
Operating Power Supply Current: DC	CS1\=V_{IL}, CS2=V_{IH}, ers=V_{IH}/V_{IL}, $I_{I/O}$=0mA	I_{CC}		35	mA
Operating Power Supply Current	$I_{I/O}$=0mA	I_{CC1}		70	mA
Min. cycle, duty=100%, CS1\=V_{IL}, CS2=V_{IH}, others = V_{IH}/V_{IL}	Cycle time=1us, duty=100%, $I_{I/O}$=0mA, CS1\≤0.2V, CS2≥V_{CC}-0.2V, V_{IL}≤0.2V	I_{CC2}		30	mA
Standby Power Supply Current: DC	CS1\=V_{IH}, CS2=V_{IH} or CS2=V_{IL}	I_{SB}		3	mA
Standby Power Supply Current(1): DC	V_{IN}≥0V	I_{SB1}		2	mA
Output Low Voltage	I_{OL} =2.1mA	V_{OL}		0.4	V
Output High Voltage	I_{OH}=-1.0mA	V_{OH}	2.4		V
Input Capacitance	V_{IN}=0V	C_{in}		8	pF
Input/Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$		10	pF

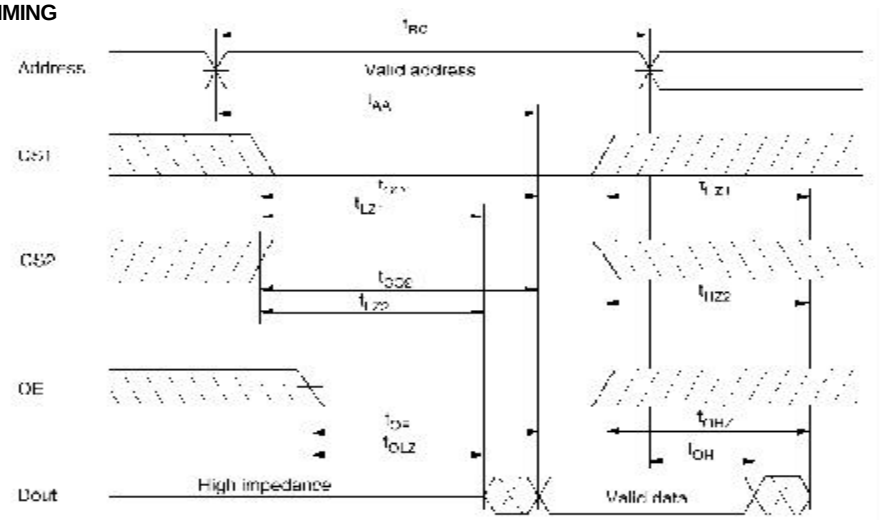
32C108RP AC ELECTRICAL CHARACTERISTICS - READ CYCLE

PARAMETER	SYMBOL	MIN	MAX	UNIT
Read Cycle Time	t_{RC}	55		ns
Address Access Time	t_{AA}		55	ns
Chip Selection (CS1\) to Output Valid	t_{CO1}		55	ns
Chip Selection (CS2) to Output Valid	t_{CO2}		55	ns
Output Enable (OE\) Output Valid	t_{OE}		25	ns
Chip Selection (CS1\) to Output in Low-Z[1,2,3]	t_{LZ1}	10		ns
Chip Selection (CS2) to Output in Low-Z[1,2,3]	t_{LZ2}	10		ns
Output Enable (OE\) to Output in Low-Z[1,2,3]	t_{OLZ}	5		ns
Chip Deselection (CS1\) to Output in High-Z[1,2,3]	t_{HZ1}	0	20	ns
Chip Deselection (CS2) to Output in High-Z[1,2,3]	t_{HZ2}	0	20	ns
Output Disable (OE\) to Output in High-Z[1,2,3]	t_{OHZ}	0	20	ns
Output Hold From Address Change	t_{OH}	10		ns

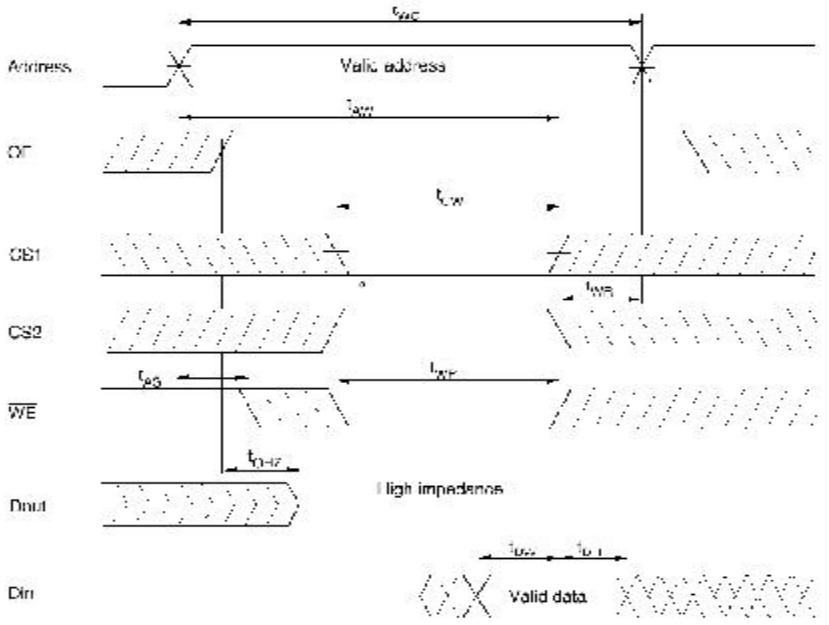
Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. Guaranteed by design.

32C108RP TIMING WAVEFORM

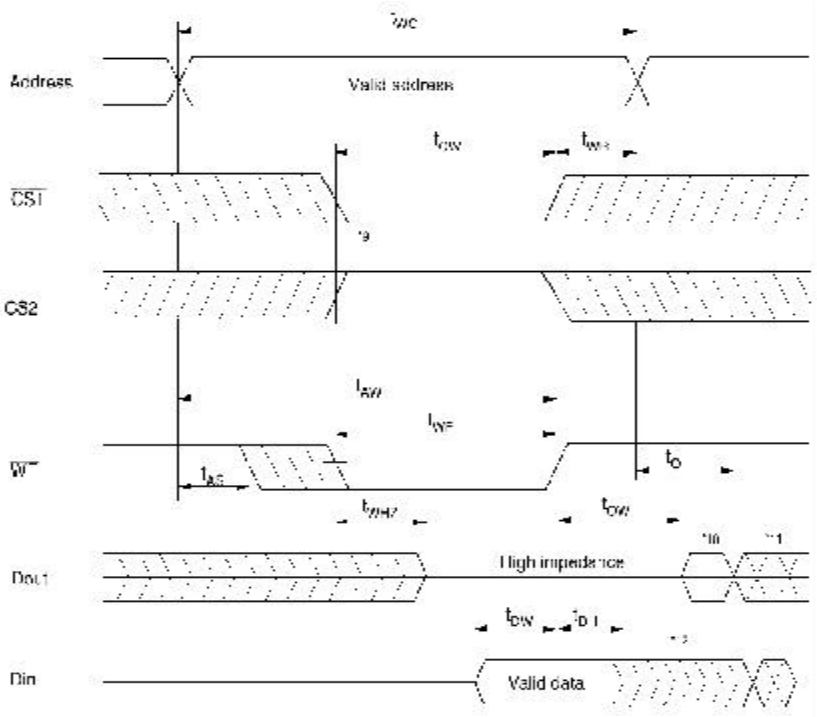
READ CYCLE TIMING

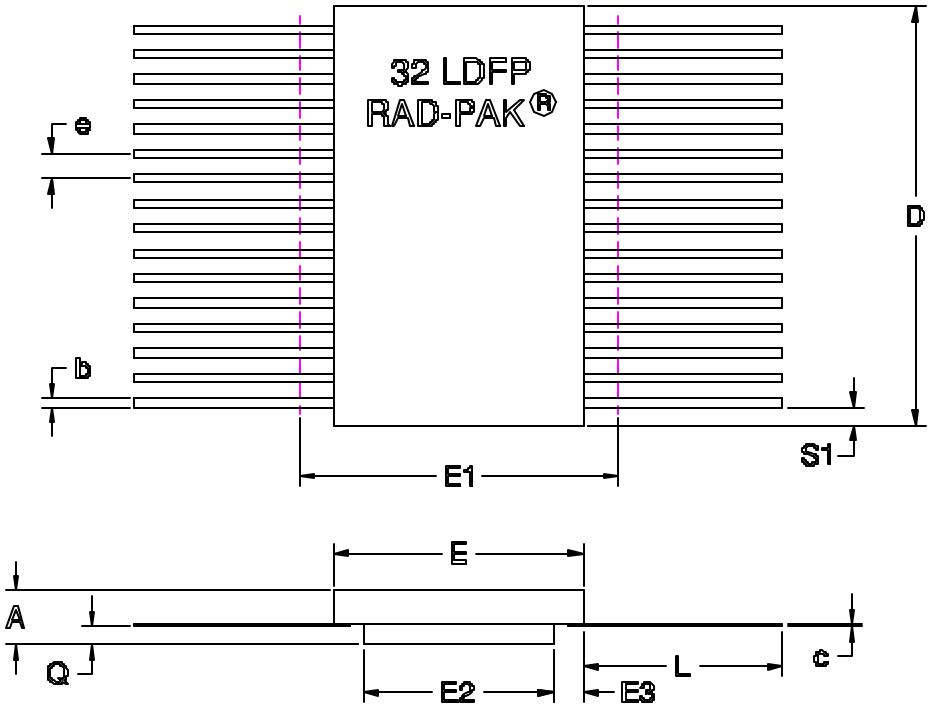


WRITE CYCLE TIMING (1) ($\overline{OE}$ Clocked)



WRITE CYCLE TIMING (2) ($\overline{OE}$ Low Fixed)





32 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.117	0.130	0.143
b	0.015	0.017	0.019
c	0.004	0.005	0.009
D	--	0.820	0.830
E	0.404	0.410	0.416
E1	--	--	0.426
E2	0.234	0.240	--
E3	0.030	0.085	--
e		0.050 BSC	
L	0.390	0.400	0.410
Q	0.021	0.033	0.036
S1	0.005	0.027	--
N		32	

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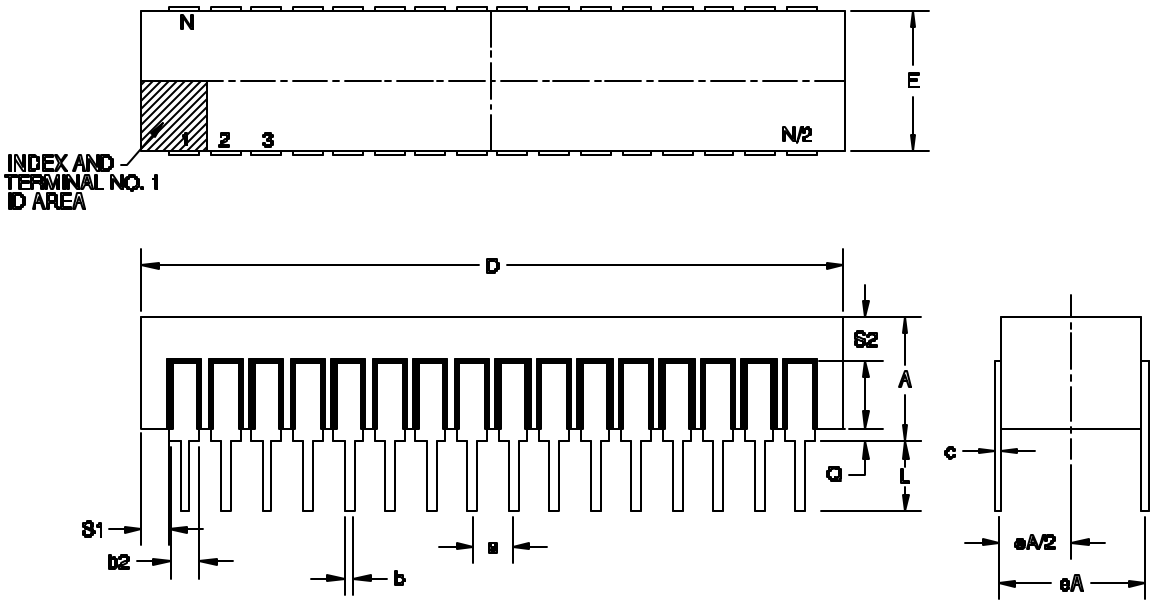
(All Dimensions are in Inches)



32 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.152	0.225
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.018
D	--	1.600	1.680
E	0.510	0.590	0.620
eA		0.600 BSC	
eA/2		0.300 BSC	
e		0.100 BSC	
L	0.135	0.145	0.155
Q	0.015	0.050	0.070
S1	0.005	0.025	--
S2	0.005	--	--
N		32	

D32-01

(All Dimensions are in Inches)