74LVC377

Octal D-type flip-flop with data enable; positive-edge trigger

Product data sheet

1. General description

The 74LVC377 is a low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74LVC377 has eight edge-triggered D-type flip-flops with individual inputs (D) and outputs (Q). A common clock input (CP) loads all flip-flops simultaneously when data enable input ($\overline{E}$) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. Input $\overline{E}$ must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

2. Features

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	-	4.6	-	ns
C_I	input capacitance		-	5.0	-	pF
f_{max}	maximum clock frequency	V_{CC} = 3.3 V	-	330	-	MHz

PHILIPS

Table 1: Quick reference data *…continued*

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{PD}	power dissipation capacitance per flip-flop		[1] [2]	-	22	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC377D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC377DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC377PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

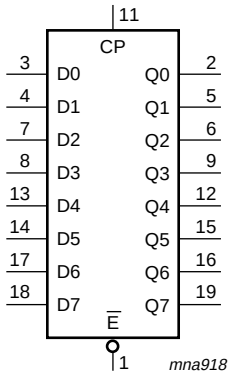


Fig 1. Logic symbol

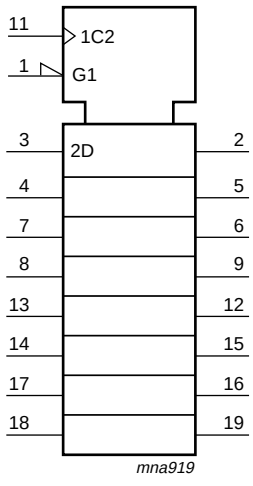


Fig 2. IEC logic symbol

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Control		Input	Output
	CP	$\overline{E}$	Dn	Qn
Load 1	↑	l	h	H
Load 0	↑	l	l	L
Hold	↑	h	X	no change
Do nothing	X	H	X	no change

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH CP transition;
X = don t care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+5.5	V
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_{IK}	input diode current	V_I < 0 V		-	–50	mA
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance	2.7	-	3.6	V
		low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.2	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.5	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.6	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.2	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	µA
C_I	input capacitance		-	5.0	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.3	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.65	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.75	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 1	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	-	±20	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	40	µA
ΔI_{CC}	additional quiescent supply current	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0 A	-	-	5	mA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 4					
		V_{CC}= 1.2 V		-	15.0	-	ns
		V_{CC} = 2.7 V		1.5	4.9	7.9	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	4.6	7.6	ns
t_W	clock pulse width HIGH or LOW	see Figure 4					
		V_{CC}= 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		5.0	1.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	4	1.0	-	ns
t_{su}	set-up time						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-		-	ns
		V_{CC} = 2.7 V		5.0	0.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	3	0.2	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.0	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.0	0.7	-	ns

Table 8: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time $\overline{E}$ to CP						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	–1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	0	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	–1.1	-	ns
		V_{CC} = 3.0 V to 3.6 V		0	–1.0	-	ns
f_{max}	maximum clock frequency	see Figure 4					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	150	330	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per flip-flop		[4] [5]	-	22	-	pF
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 4					
		V_{CC}= 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	10	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	9.5	ns
t_W	clock pulse width HIGH or LOW	see Figure 4					
		V_{CC}= 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		5.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		4.0	-	-	ns
t_{su}	set-up time						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-		-	ns
		V_{CC} = 2.7 V		5.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.0	-	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	ns

Table 8: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time $\overline{E}$ to CP						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		0	-	-	ns
f_{max}	maximum clock frequency	see Figure 4					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	-	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.5	ns

[1] Typical values are measured at T_{amb} = 25 °C.

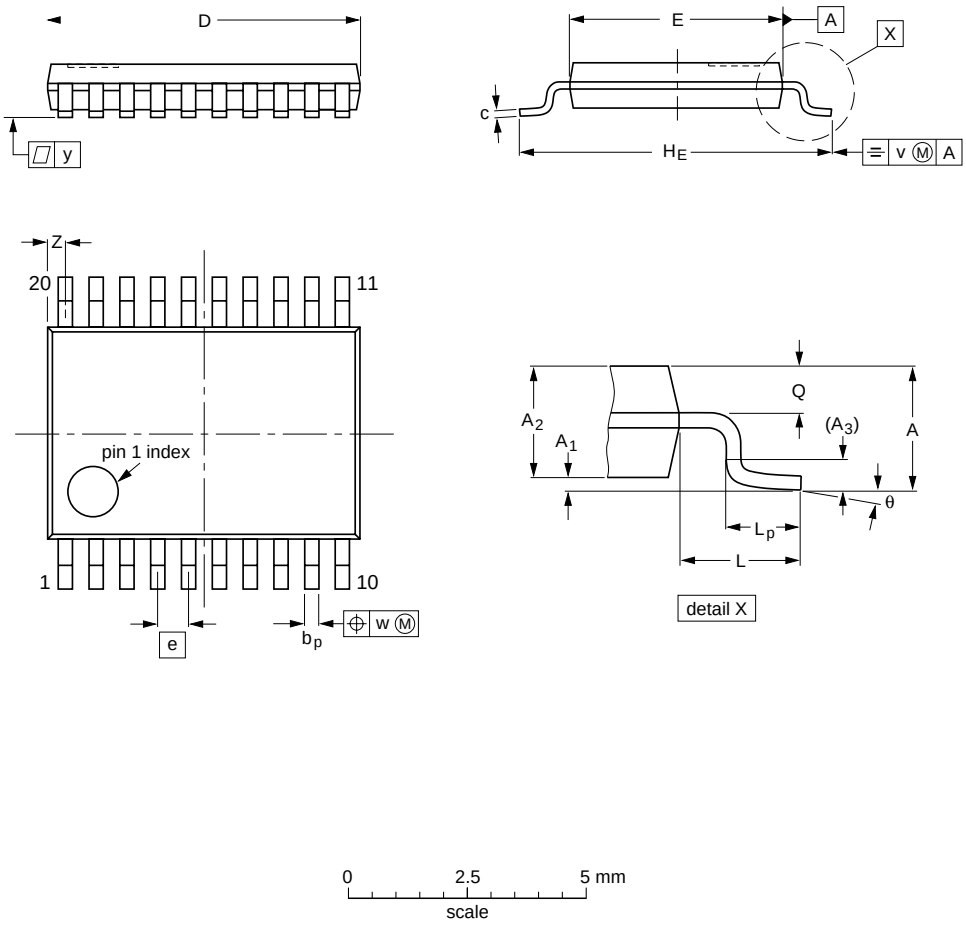
[2] Typical value is measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				

Fig 9. Package outline SOT360-1 (TSSOP20)