IRFP350, IRFP351, IRFP352, IRFP353

File Number **2319**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

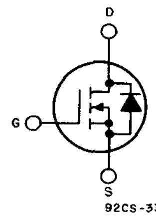
14 A and 16 A, 350 V - 400 V
$r_{DS(on)}$ = 0.3 Ω and 0.4 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRFP350, IRFP351, IRFP352, and IRFP353 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

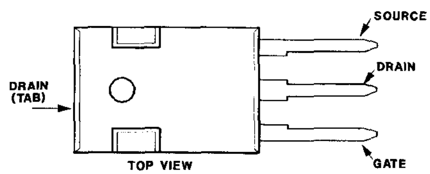
The IRFP-types are supplied in the JEDEC TO-247 plastic package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-247

Absolute Maximum Ratings

Parameter		IRFP350	IRFP351	IRFP352	IRFP353	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	16		14		A
I_D @ T_C = 100°C	Continuous Drain Current	10		8.9		A
I_{DM}	Pulsed Drain Current ②	64		56		A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	180				W
	Linear Derating Factor	1.4				W/°C ⑤
I_{LM}	Inductive Current, Clamped	(See Fig. 14) L = 100μH 64		56		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

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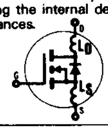
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRFP350 IRFP352	400	–	–	V	V_{GS} = 0V
	IRFP351 IRFP353	350	–	–	V	I_D = 250 μA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
I_{GSS} Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS} Gate-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		–	–	1000	μA	V_{DS} = Max. Rating × 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$ On-State Drain Current ④	IRFP350 IRFP351	16	–	–	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max.}$, V_{GS} = 10V
	IRFP352 IRFP353	14	–	–	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ④	IRFP350 IRFP351	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 8.9A
	IRFP352 IRFP353	–	0.30	0.40	Ω	
g_{fs} Forward Transconductance ④	ALL	8.0	12	–	S(℧)	V_{DS} = 2 × V_{GS}, I_{DS} = 8.0
C_{iss} Input Capacitance	ALL	–	2400	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss} Output Capacitance	ALL	–	460	–	pF	
C_{rss} Reverse Transfer Capacitance	ALL	–	99	–	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	–	12	18	ns	V_{DD} = 200V, I_D ≈ 15A, R_G = 6.2Ω, R_D = 13Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	–	51	77	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	–	75	110	ns	
t_f Fall Time	ALL	–	47	71	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	87	130	nC	V_{GS} = 10V, I_D = 15A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	–	10	15	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	–	33	50	nC	
L_D Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC} Junction-to-Case	ALL	–	–	0.70	°C/W ⑤	
R_{thCS} Case-to-Sink	ALL	–	0.10	–	°C/W ⑤	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	–	–	80	°C/W ⑤	Typical socket mount
Mounting Torque	ALL	–	–	10	in. • lbs.	Standard 6-32 screw

Source-Drain Diode Ratings and Characteristics

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	IRFP350 IRFP351	–	–	16	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRFP352 IRFP353	–	–	14	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRFP350 IRFP351	–	–	64	A	
	IRFP352 IRFP353	–	–	56	A	
V_{SD} Diode Forward Voltage ②	ALL	–	–	1.6	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr} Reverse Recovery Time	ALL	270	600	1300	ns	T_J = 25°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR} Reverse Recovered Charge	ALL	1.7	3.8	8.1	μC	T_J = 25°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C.
⑤ K/W = °C/W
W/K = W/°C

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ @ V_{dd} = 50V, T_j = 25°C, L = 100 μH, RG = 25Ω

④ Pulse Test: Pulse width ⩽ 300μs, Duty Cycle ⩽ 2%.

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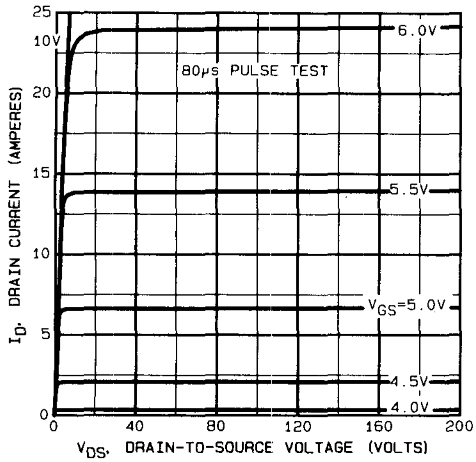

Fig. 1 — Typical Output Characteristics

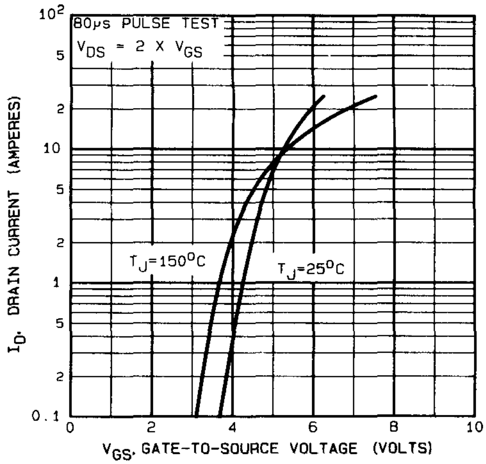

Fig. 2 — Typical Transfer Characteristics

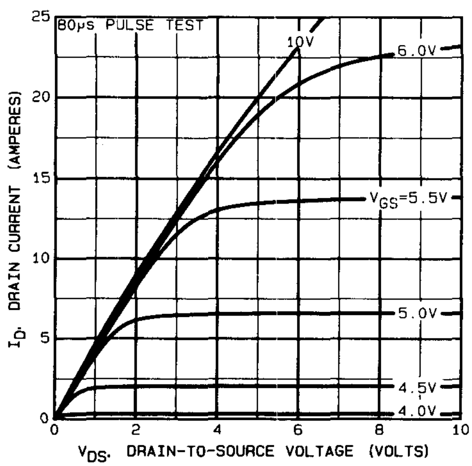

Fig. 3 — Typical Saturation Characteristics

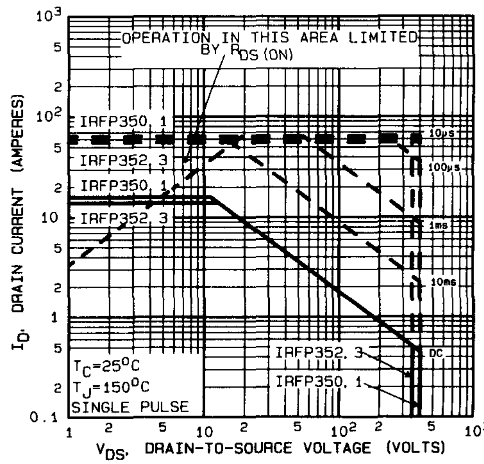

Fig. 4 — Maximum Safe Operating Area

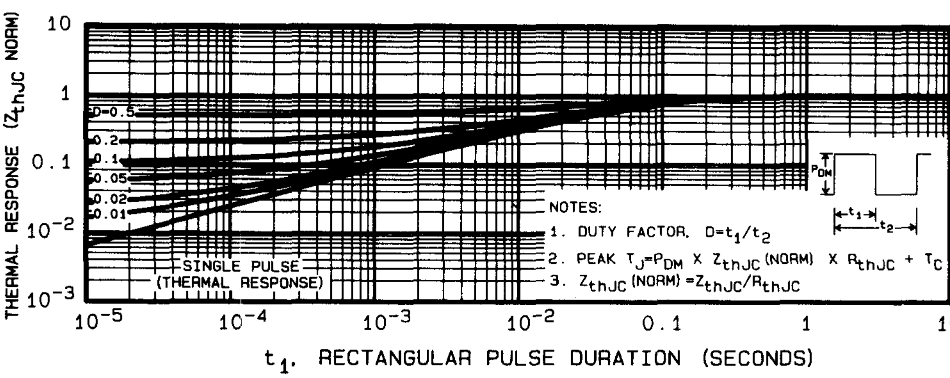

Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

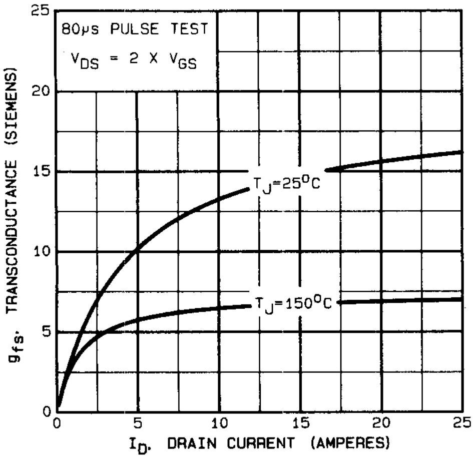

Fig. 6 — Typical Transconductance Vs. Drain Current

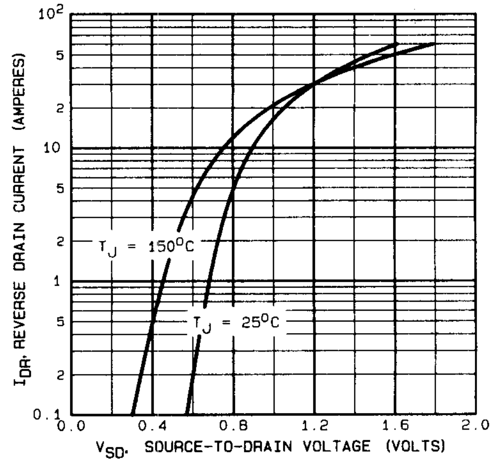

Fig. 7 — Typical Source-Drain Diode Forward Voltage

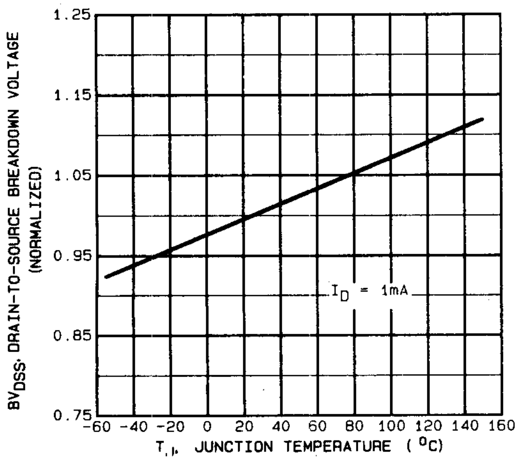

Fig. 8 — Breakdown Voltage Vs. Temperature

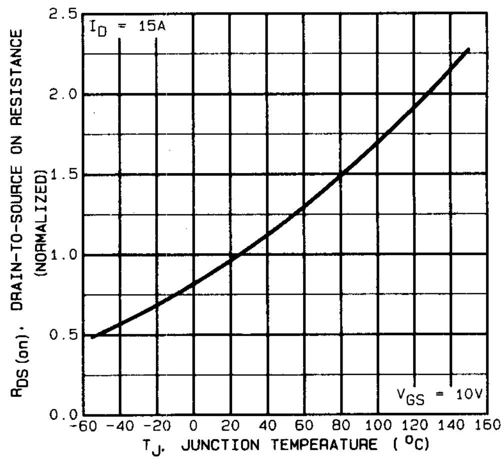

Fig. 9 — Normalized On-Resistance Vs. Temperature

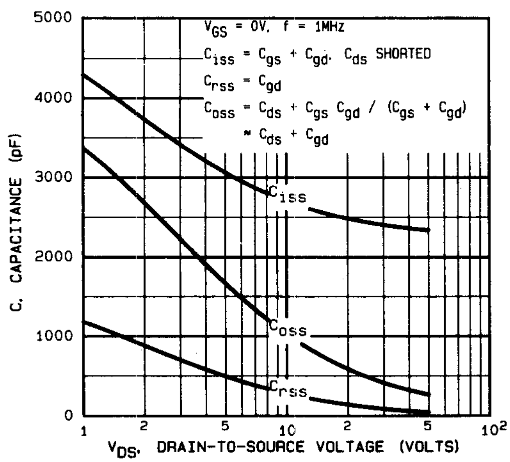

Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

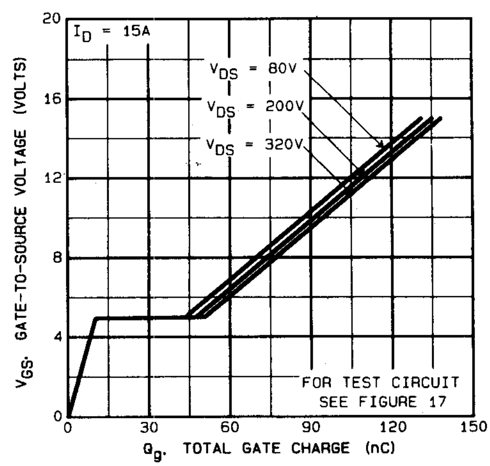

Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

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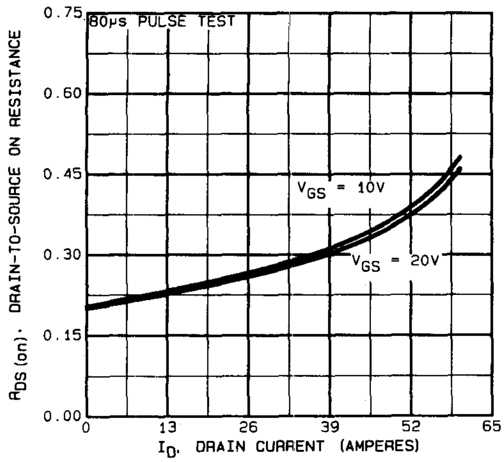

Fig. 12 – Typical On-Resistance Vs. Drain Current

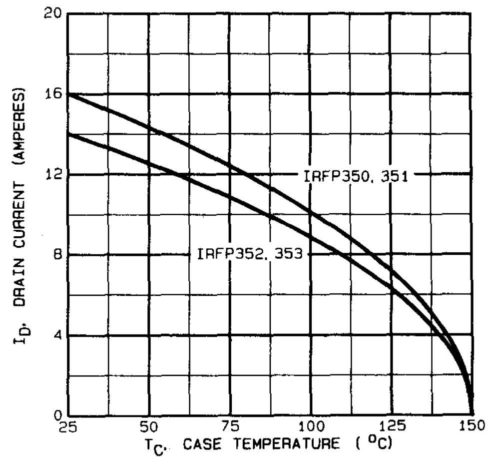

Fig. 13 – Maximum Drain Current Vs. Case Temperature

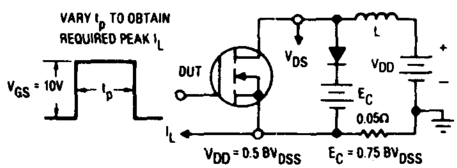

Fig. 14 – Clamped Inductive Test Circuit

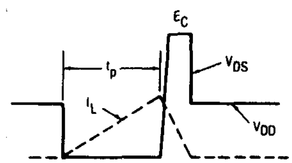

Fig. 15 – Clamped Inductive Waveforms

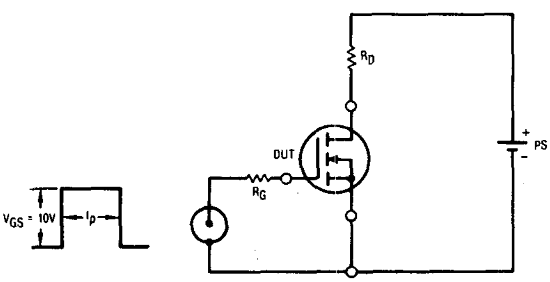

Fig. 16 – Switching Time Test Circuit

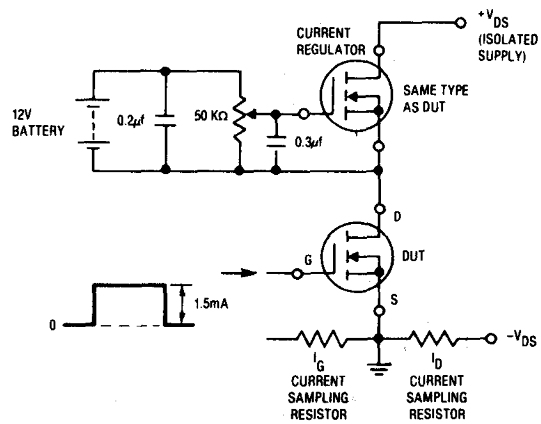

Fig. 17 – Gate Charge Test Circuit