

SN74AHCT367 Hex Buffer and Line Driver with 3-State Output

1 Features

- Inputs are TTL-voltage compatible
- True outputs
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
 - 2000V human-body model
 - 2000V charged-device model

2 Applications

- Telecom Infrastructure
- TVs
- Set Top Boxes
- Network Switches
- Wireless Infrastructure
- Electronic Points of Sale

3 Description

The SN74AHCT367 device is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

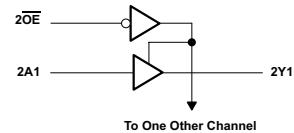
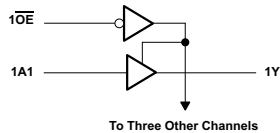
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AHCT367	D (SOIC, 16)	9.9mm x 6mm	9.9mm x 3.90mm
	DB (SSOP, 16)	6.2mm x 7.8mm	6.2mm x 5.30mm
	DGV (TSSOP, 16)	3.6mm x 6.4mm	3.6mm x 4.4mm
	PW (TSSOP, 16)	5mm x 6.4mm	5.00mm x 4.40mm

(1) For more information, see [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length x width) is a nominal value and includes pins, where applicable.

(3) The body size (length x width) is a nominal value and does not include pins.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features	1	7.3 Feature Description.....	8
2 Applications	1	7.4 Device Functional Modes.....	8
3 Description	1	8 Application and Implementation	9
4 Pin Configuration and Functions	3	8.1 Application Information.....	9
5 Specifications	4	8.2 Typical Application.....	9
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	10
5.2 ESD Ratings.....	4	8.4 Layout.....	10
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	12
5.4 Thermal Information.....	5	9.1 Documentation Support.....	12
5.5 Electrical Characteristics.....	5	9.2 Receiving Notification of Documentation Updates.....	12
5.6 Switching Characteristics.....	5	9.3 Support Resources.....	12
5.7 Noise Characteristics.....	6	9.4 Trademarks.....	12
5.8 Operating Characteristics.....	6	9.5 Electrostatic Discharge Caution.....	12
5.9 Typical Characteristics.....	6	9.6 Glossary.....	12
6 Parameter Measurement Information	7	10 Revision History	12
7 Detailed Description	8	11 Mechanical, Packaging, and Orderable Information	13
7.1 Overview.....	8		
7.2 Functional Block Diagram.....	8		

4 Pin Configuration and Functions

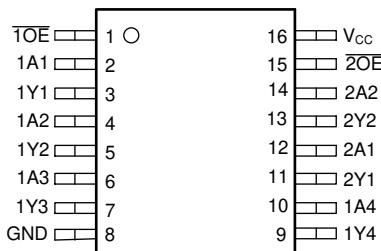


Figure 4-1. D, DB, DGV, or PW Package; 16-Pin SOIC, SSOP, TVSOP, or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1 OE	I	Output Enable 1
2	1A1	I	1A1 Input
3	1Y1	O	1Y1 Output
4	1A2	I	1A2 Input
5	1Y2	O	1Y2 Output
6	1A3	I	1A3 Input
7	1Y3	O	1Y3 Output
8	GND	—	Ground Pin
9	1Y4	O	1Y4 Output
10	1A4	I	1A4 Input
11	2Y1	O	2Y1 Output
12	2A1	I	2A1 Input
13	2Y2	O	2Y2 Output
14	2A2	I	2A2 Input
15	2 OE	I	Output Enable 2
16	V _{cc}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range ⁽²⁾		-0.5	7	V
V_O	Output voltage range ⁽²⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND			± 75	mA
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74AHCT367		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		-8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHCT367				UNIT °C/W
		D	DB	DGV	PW	
		16 PINS				
R _{θJA}	Junction-to-ambient thermal resistance	93.8	103.9	124.5	135.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.7	54.3	49.8	70.3	
R _{θJB}	Junction-to-board thermal resistance	50.9	54.6	56.2	81.3	
Ψ _{JT}	Junction-to-top characterization parameter	20.8	14.3	5.8	22.5	
Ψ _{JB}	Junction-to-board characterization parameter	50.7	54.0	55.7	80.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = −50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = −8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1		V
	I _{OH} = 8 mA			0.36		0.44		0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±0.1 ⁽¹⁾		±1 ⁽¹⁾		±1		μA
I _{OZ}	V _O = V _{CC} or GND V _I (OE) = V _{IL} or V _{IH}	5.5 V		±0.25		±2.5		±2.5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		4		40		40		μA
ΔI _{CC} ⁽²⁾	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V		1.35		1.5		1.5		mA
C _i	V _I = V _{CC} or GND	5 V	2.5	10		10		10		pF
C _O	V _O = V _{CC} or GND	5 V	5							pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C		−40°C to 85°C		−40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF	2.5 ⁽¹⁾	4.8 ⁽¹⁾	1	6.5	1	8.5	ns
t _{PHL}				2.5 ⁽¹⁾	4.8 ⁽¹⁾	1	6.5	1	8.5	
t _{PZH}	OE	Y	C _L = 15 pF	3.5 ⁽¹⁾	8 ⁽¹⁾	1	9.5	1	9	ns
t _{PZL}				2.8 ⁽¹⁾	7 ⁽¹⁾	1	8.5 ⁽¹⁾	1	8	
t _{PHZ}	OE	Y	C _L = 15 pF	3.1 ⁽¹⁾	8 ⁽¹⁾	1	9.5	1	9	ns
t _{PLZ}				2.8 ⁽¹⁾	7 ⁽¹⁾	1	8.5	1	8	
t _{PLH}	A	Y	C _L = 50 pF	3.5	5.8	1	7.5	1	9.5	ns
t _{PHL}				3.3	5.8	1	7.5	1	9.5	
t _{PZH}	OE	Y	C _L = 50 pF	4.5	9	1	10.5	1	10	ns
t _{PZL}				3.7	8	1	9.5	1	9	
t _{PHZ}	OE	Y	C _L = 50 pF	4.1	9	1	10.5	1	10	ns
t _{PLZ}				3.6	8	1	9.5	1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.7 Noise Characteristics

$V_{CC} = 5$ V, $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	SN74AHCT367			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.4		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.4		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$ High-level dynamic input voltage		2		V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

5.8 Operating Characteristics

$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1$ MHz	22	pF

5.9 Typical Characteristics

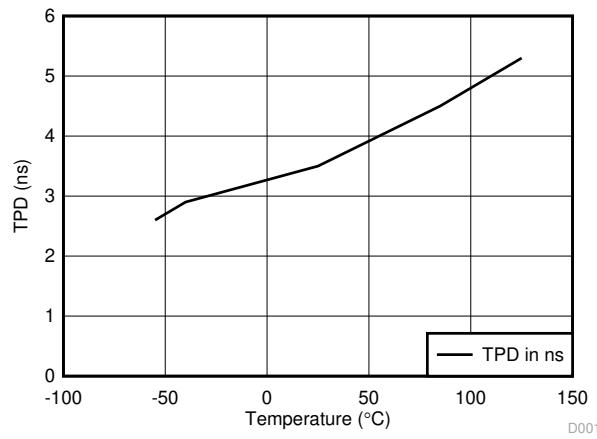
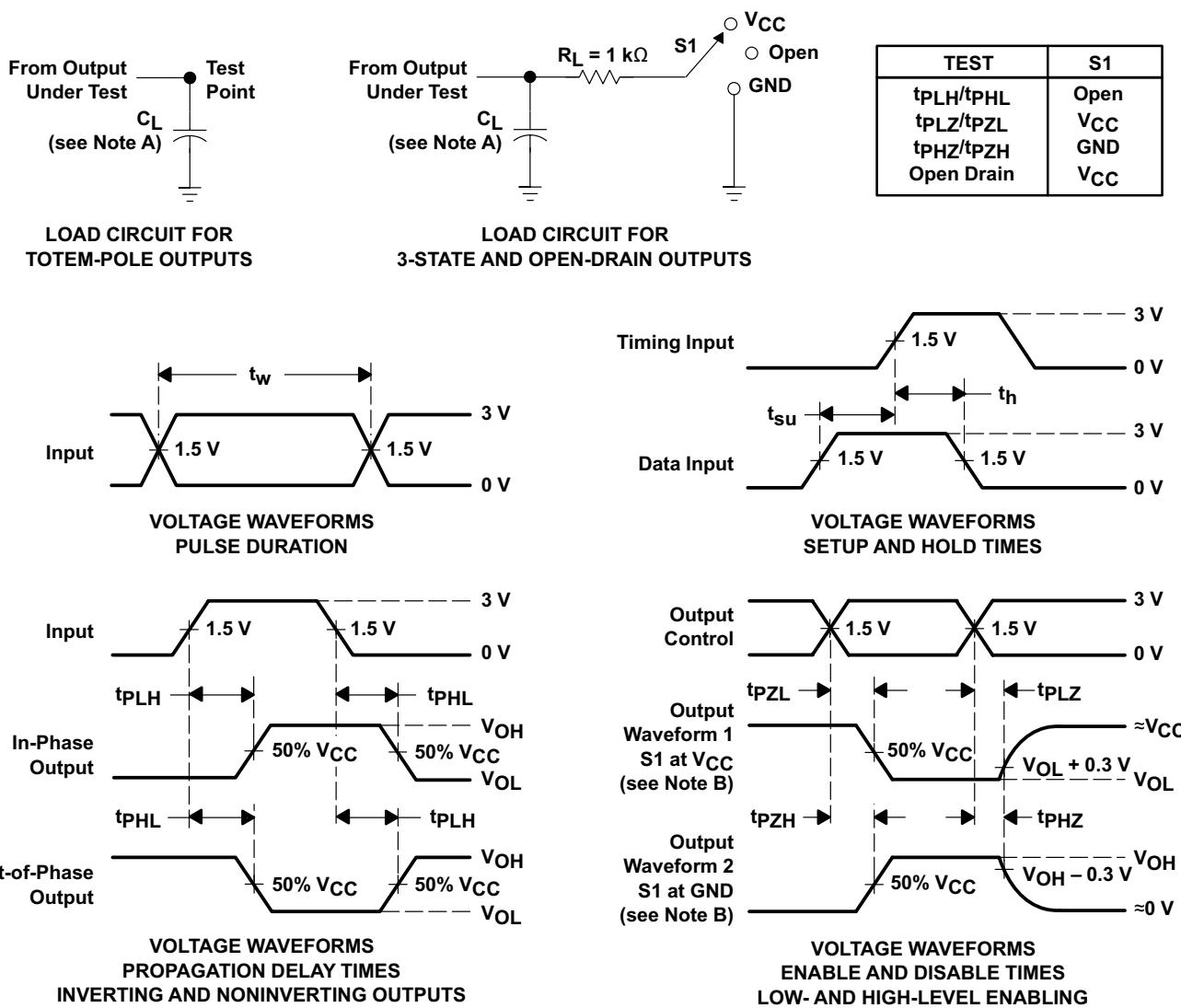


Figure 5-1. TPD vs Temperature, 50 pF Load

6 Parameter Measurement Information



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHCT367 device is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. This device is organized as a dual 4-line and 2-line buffer/driver with active-low output-enable (1 \overline{OE} and 2 \overline{OE}) inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

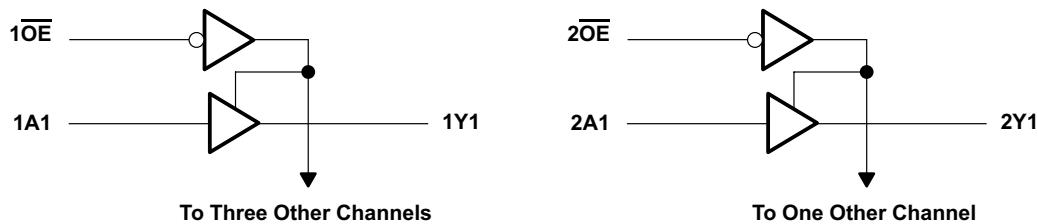


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
 - Inputs Accept V_{IH} levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

7.4 Device Functional Modes

Table 7-1. Function Table
(Each Buffer/Driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
H	X	Z
L	H	H
L	L	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74AHCT367 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH} . This feature makes it ideal for translating up from 3.3 V to 5 V. [Figure 8-2](#) shows this type of translation.

8.2 Typical Application

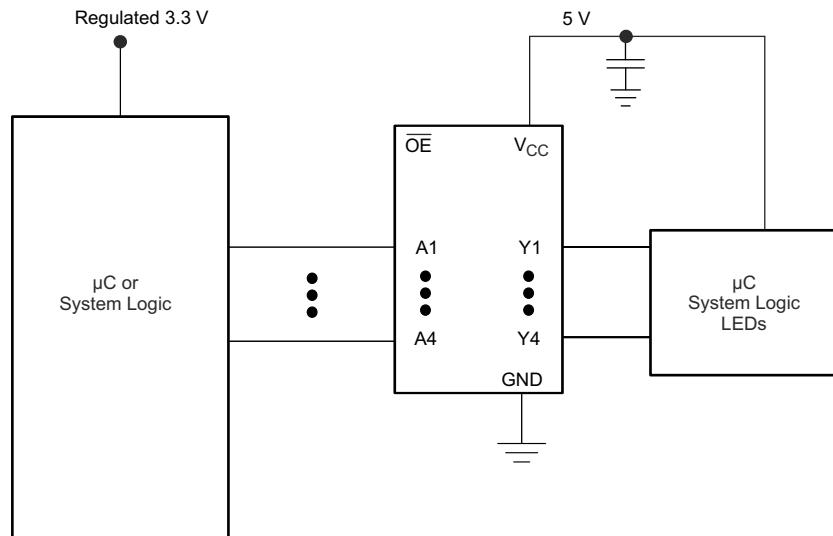


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Section 5.3](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Section 5.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curves

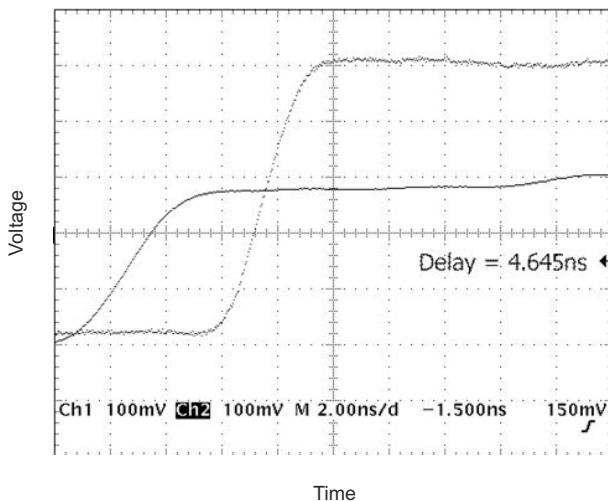


Figure 8-2. Typical Application Curve

8.3 Power Supply Recommendations

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

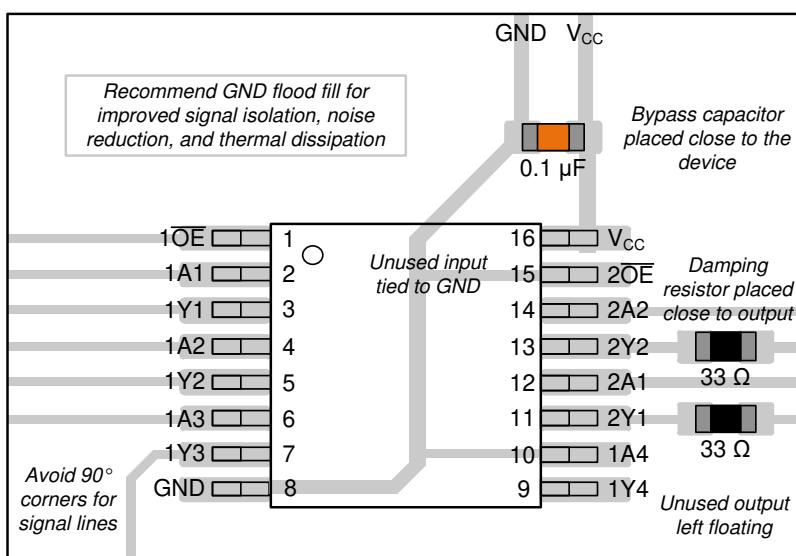


Figure 8-3. Example Layout for the SN74AHCT367 in the PW Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT367	Click here				

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision H (December 2014) to Revision I (July 2024)	Page
• Deleted machine model from <i>Features</i> section.....	1
• Updated packages and added package sizes to <i>Package Information</i> table.....	1
• Updated structural layout of data sheet to current standards.....	1
• Updated R _{θJA} values: D = 85.1 to 93.8, PW = 111.5 to 135.9; Updated D and PW packages for R _{θJC} (top), R _{θJB} , Ψ _{JT} , Ψ _{JB} , and R _{θJC} (bot), all values in °C/W	5
• Updated <i>Layout Example</i> figure.....	11

Changes from Revision G (July 2003) to Revision H (December 2014)	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and</i>	

<i>Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table.....	1
• MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table.....	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHCT367D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	AHCT367
SN74AHCT367DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367DGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367DGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT367
SN74AHCT367DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT367
SN74AHCT367PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 125	HB367
SN74AHCT367PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367
SN74AHCT367PWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

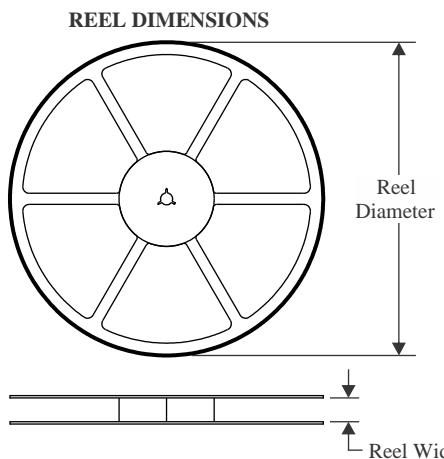
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

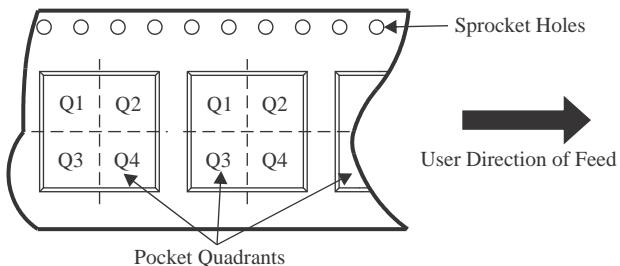
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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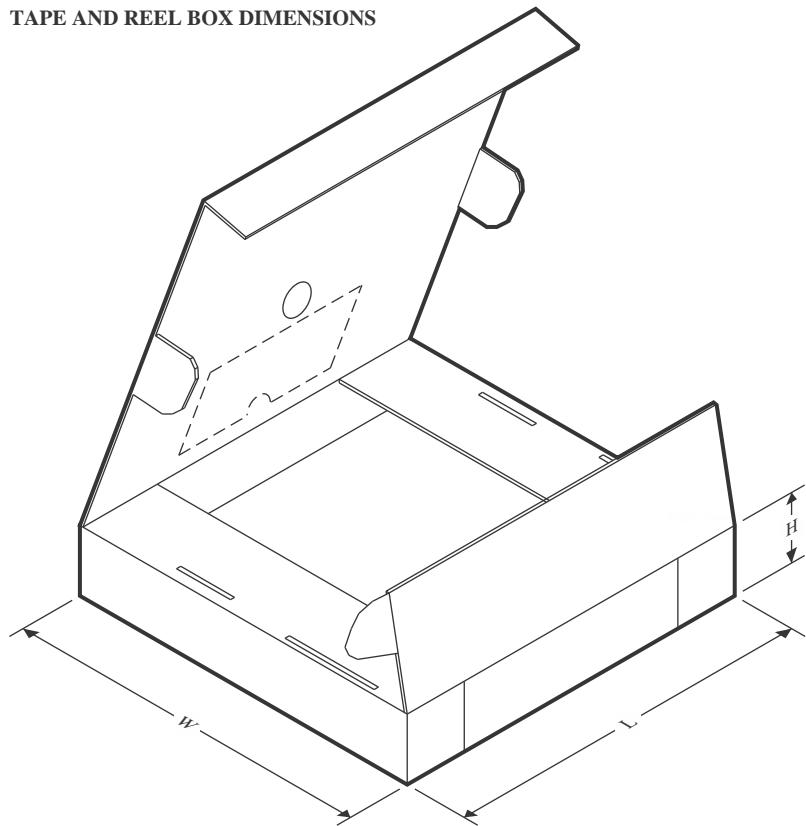
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT367DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT367DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT367DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT367PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT367PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

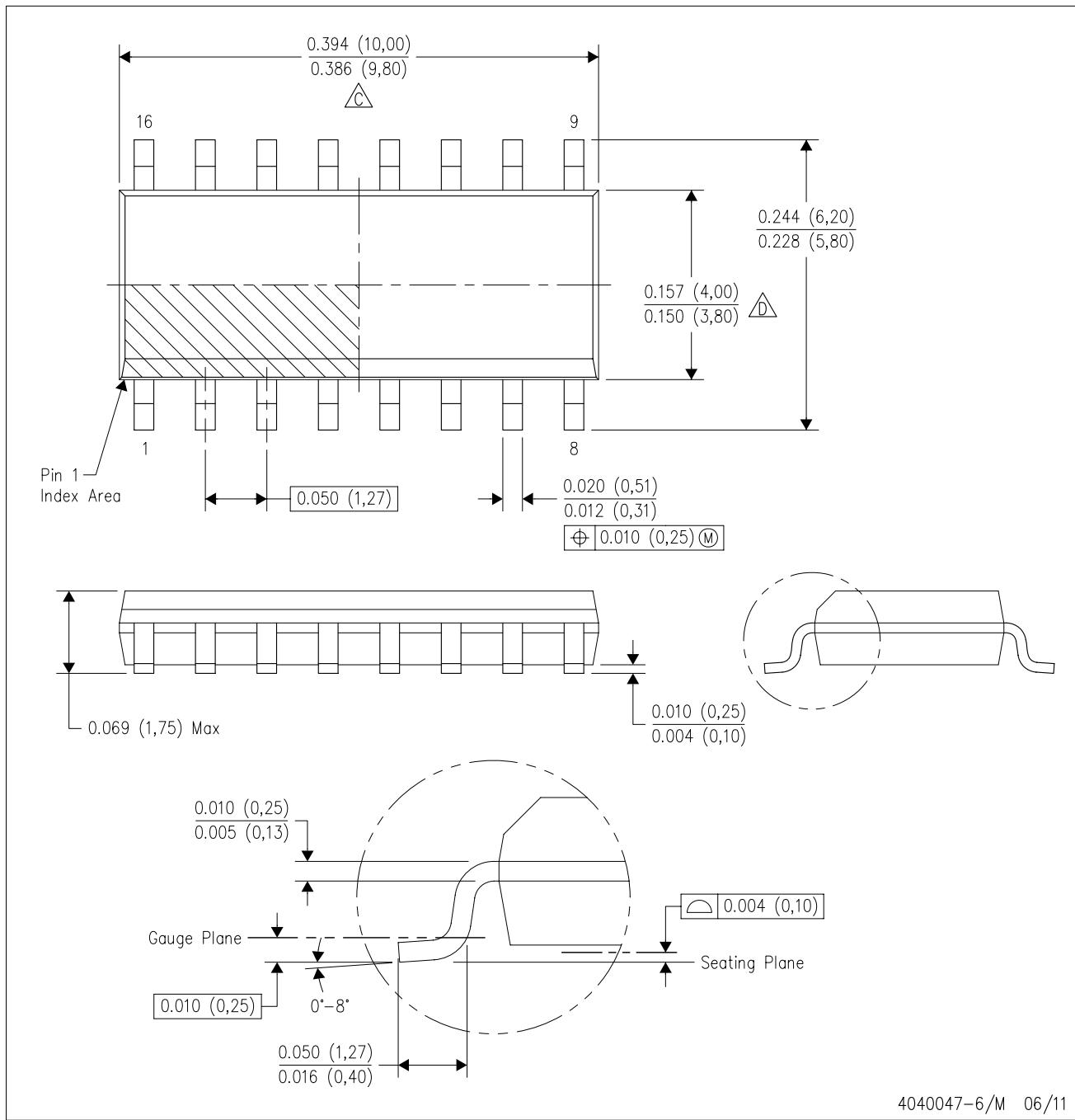
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT367DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHCT367DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74AHCT367DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT367PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHCT367PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

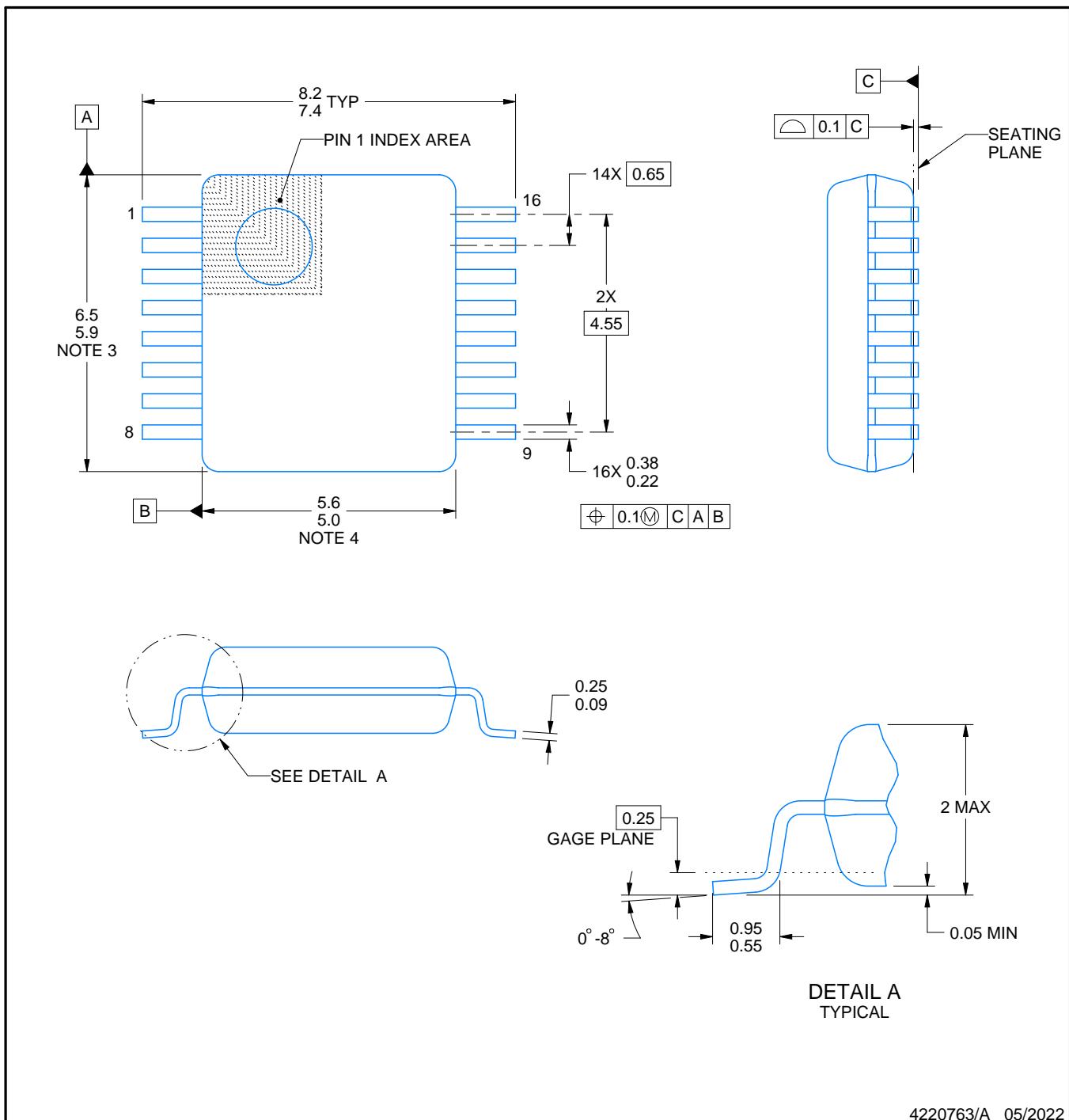
PACKAGE OUTLINE

DB0016A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

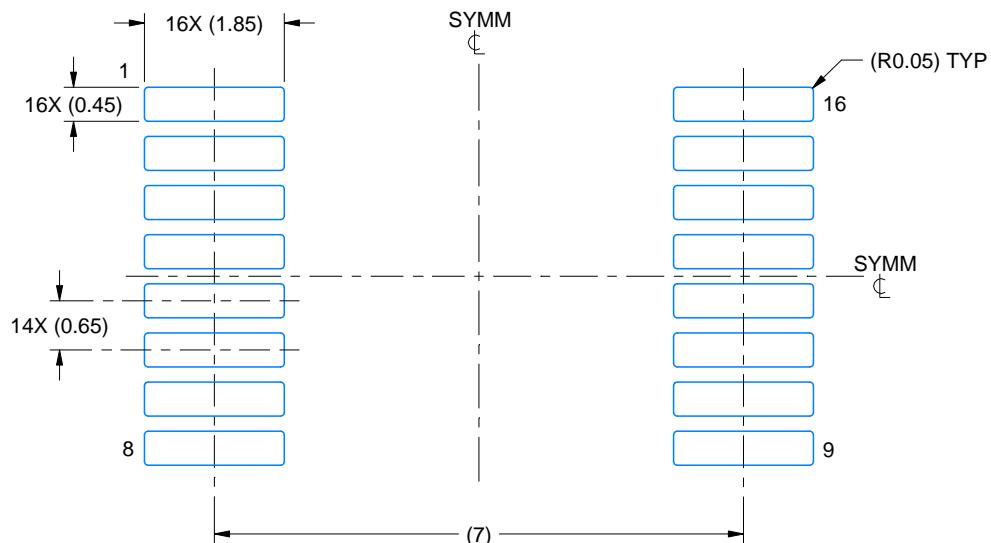
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

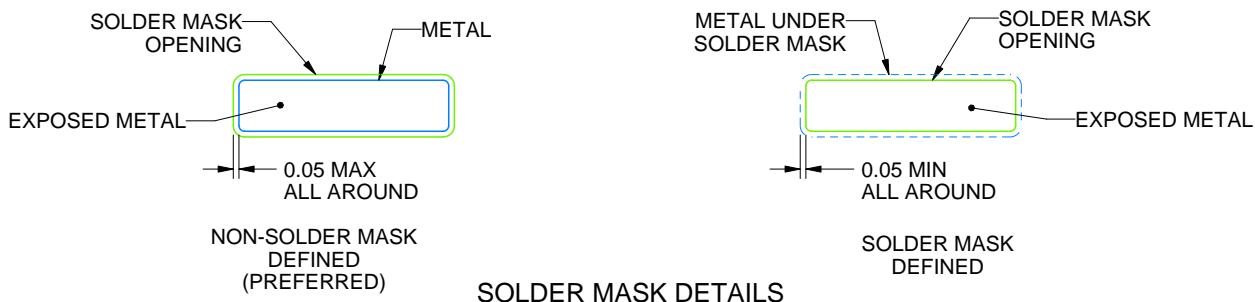
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

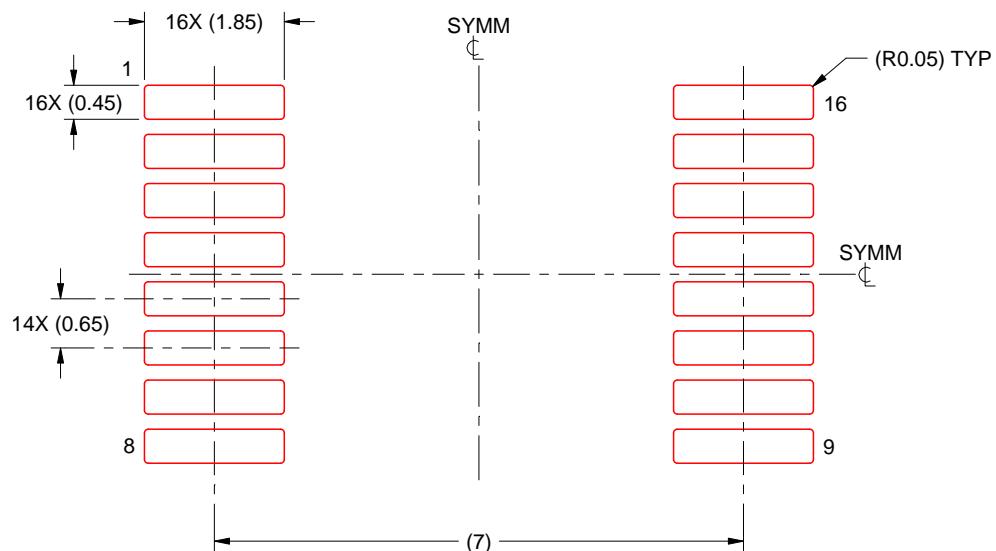
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X**

4220763/A 05/2022

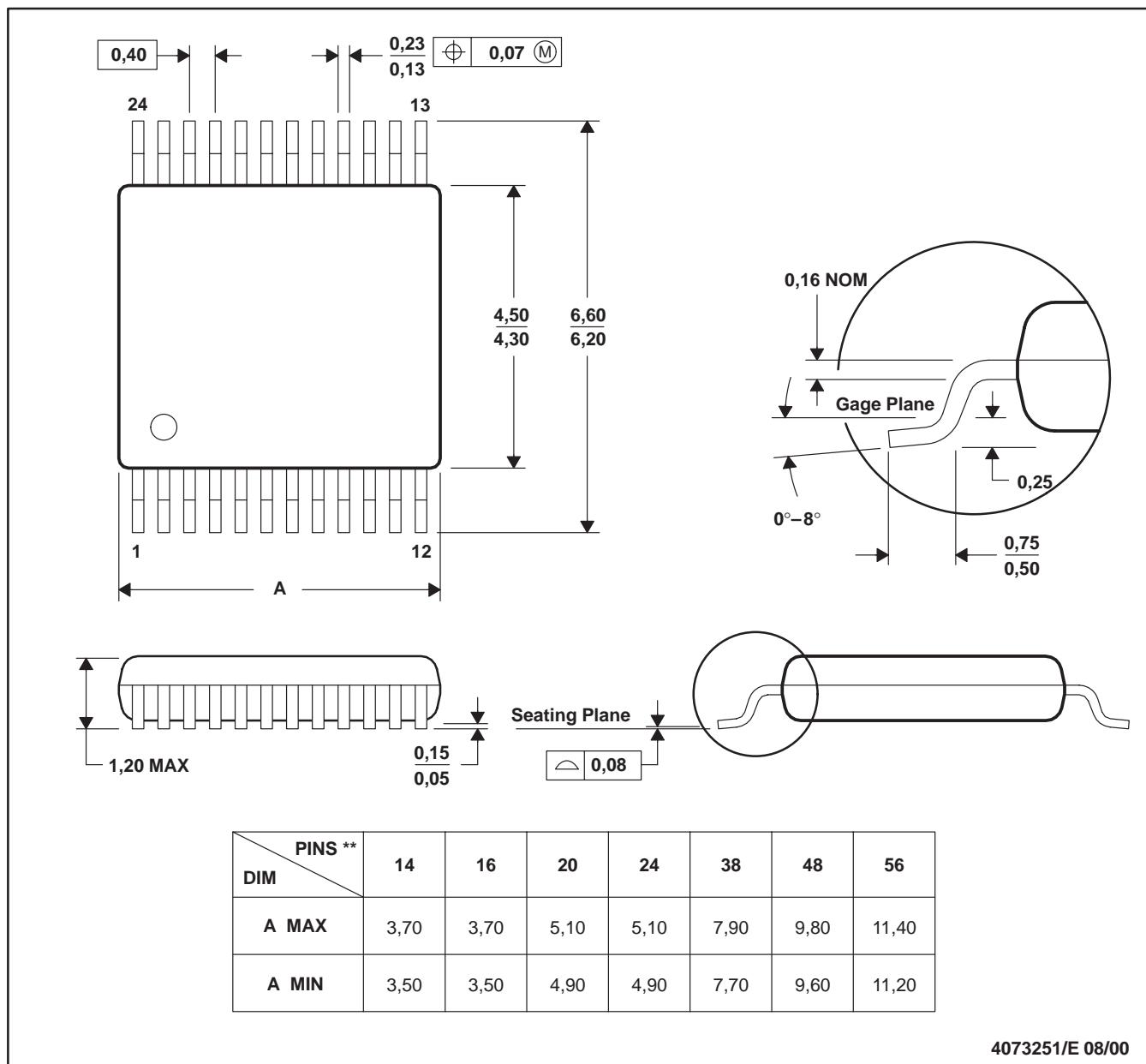
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

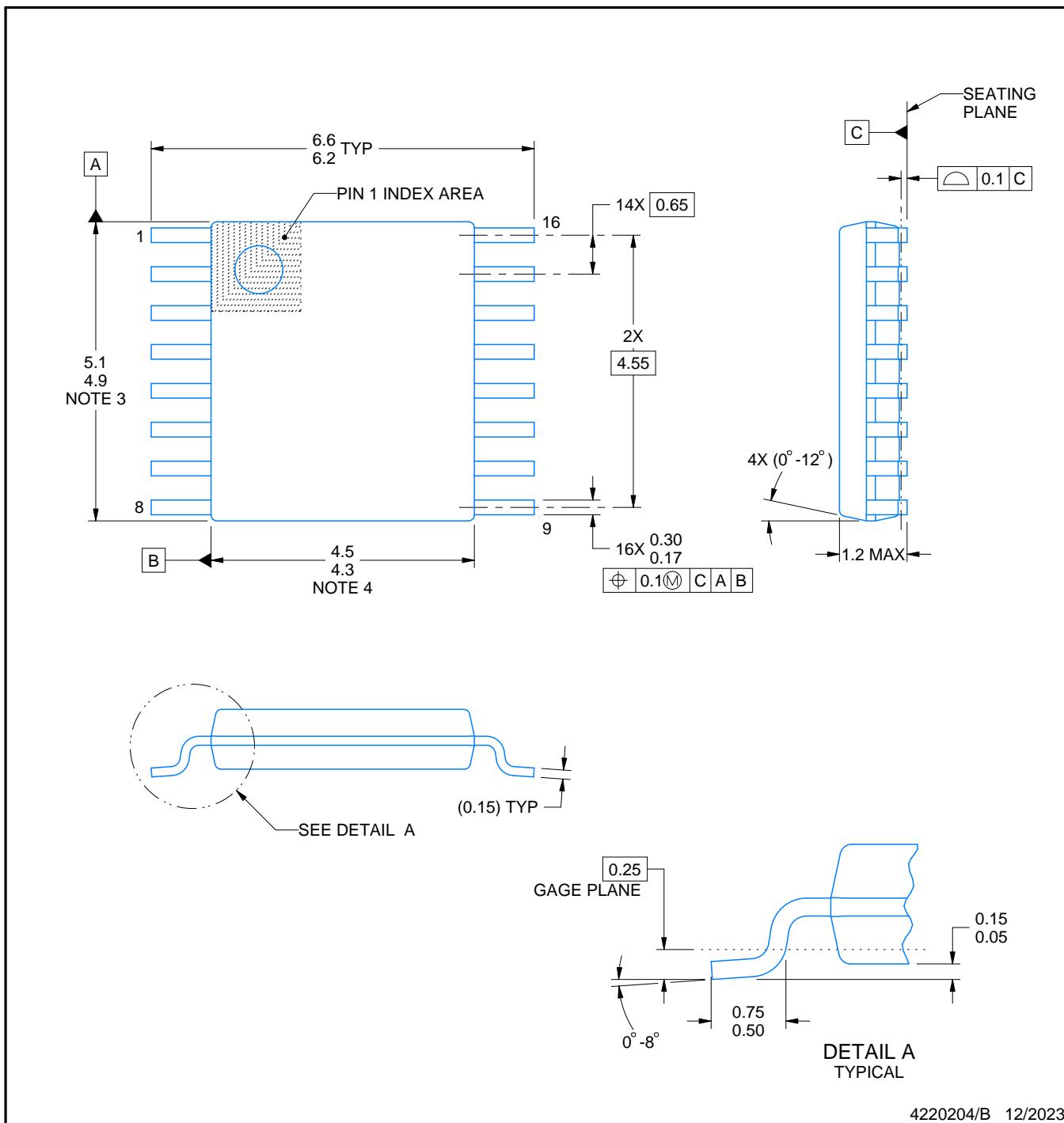
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

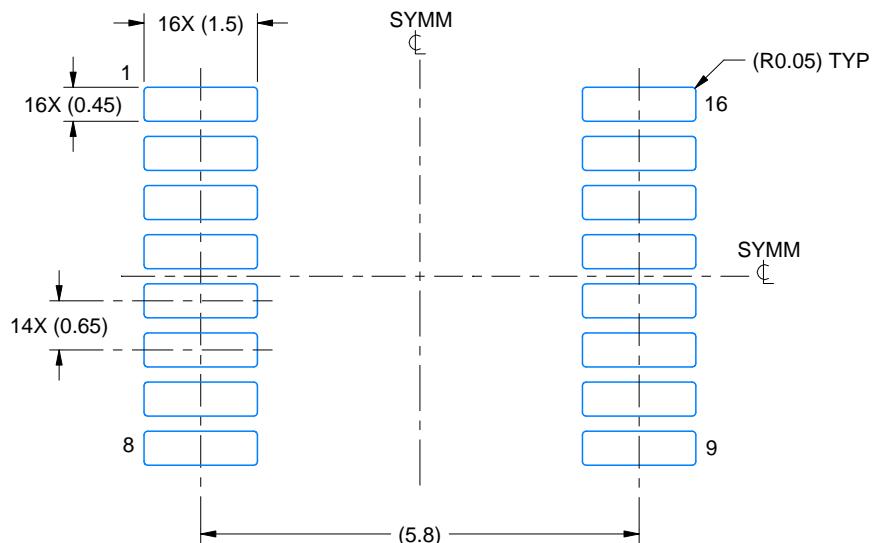
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

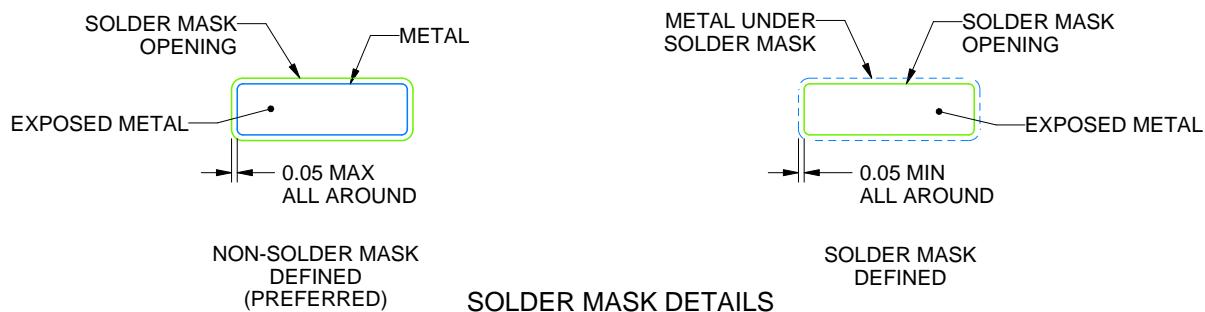
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

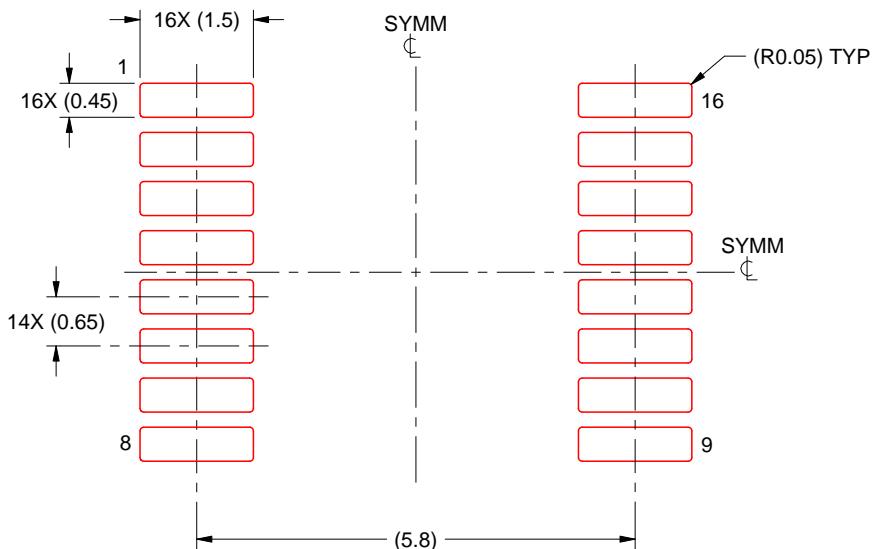
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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