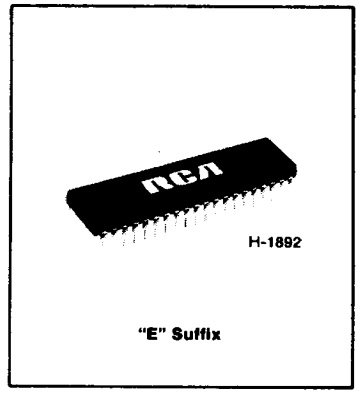
CMOS Four-Digit LCD Decoder-Drivers

6-V Rating

Features
- *6-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Direct microprocessor interface*
- *Decodes binary into hexadecimal (CD22105) and decimal (CD22105A) outputs*

Applications
- *Microprocessor-controlled digital meters and calculators*
- *General-purpose displays*
- *Microprocessor-controlled automotive dashboard displays*
- *Microprocessor appliance control panels*



The RCA-CD22105 types are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

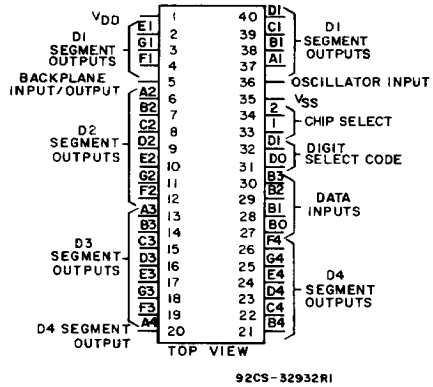
The CD22105 types contain all the circuitry necessary to drive conventional liquid-crystal displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four-digit displays.

The backplane and segment drives are designed so that p and n channels have the same ON resistances and thus equal rise and fall times. This equality eliminates any DC component, thereby maximizing display life. In addition to feeding the internal display drivers, the backplane signal can also be used as a master to drive a number of slave devices. The number of slaved devices should be limited to the load that keeps the backplane rise and fall times from exceeding 5 μs. If this limit is to be exceeded, the master backplane drivers should be disabled (by connecting pin 36, the oscillator input, to V_{SS}) and pin 5 should be fed from an external oscillator and all devices slaved to it. The maximum frequency of the external signal should be 125 Hz at room temperatures.

The on-board oscillator, which operates at 16 kHz when free-running (pin 36 floating), provides a backplane signal whose frequency is approximately 125 Hz. This frequency can be reduced by connecting an external capacitor to pin 36. Plots of backplane frequency vs. supply voltage at various values of external capacitance are shown in Fig. 3. The oscillator may be overdriven by an external signal but care must be taken to keep the lower voltage level above V_{SS} by at least 20 per cent of V_{DD} (for V_{DD}=5 V the signal should oscillate between +1 and +5 volts). This precaution prevents the backplane driver from being disabled, a condition that would present a DC component to the LCD display. A signal swinging from rail-to-rail can also be used to overdrive the oscillator but in this case the duty cycle should be such that the lower portion of the signal must be less than one-microsecond duration (the backplane disable sensing circuit will not respond to signals of this duration).

A four-bit data-input latch and a two-bit select-code latch under the control of two chip-select inputs permit interfacing with a microprocessor. This device simplifies designing a seven-segment display into a microprocessor system, without requiring extensive ROM or CPU time for decoding and display updating. The four-bit binary input is decoded by means of a PROM into a seven-segment hexadecimal output for the CD22105 type and into a decimal display for the CD22105A type. These types are pin-compatible with the Intersil ICM7211MIPL and ICM7211AMIPL, respectively.

The CD22105 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.



CD22105, CD22105A
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.3 to +6.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to V_{DD} +0.3 V
DC INPUT CURRENT, ANY ONE INPUT* ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-20 to +60° C ..... 500 mW
For T_A=+60 to +70° C ..... Derate Linearly at 12 mW/° C to 380 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -20 to +70° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +125° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

*Pin 36 limited to ±5 mA.

STATIC ELECTRICAL CHARACTERISTICS
T_A=25° C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Operating Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3	5	6	V
Operating Current	I_{op}	Display Operating	—	10	50	μA
Oscillator Input Current	I_{OL}, I_{OH}	Pin 36	—	±2	±10	μA
Segment Rise and Fall Time	t_{rs}, t_{fs}	C_L = 200 pF	—	0.5	—	μs
Backplane Rise and Fall Time	t_{rB}, t_{fB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz
Input High Voltage	V_{IH}		3.5	—	—	V
Input Low Voltage	V_{IL}		—	—	1.5	V
Input Leakage Current	I_{IL}	Pins 27-34	—	±0.01	±1	μA
Input Capacitance	C_I	Pins 27-34	—	5	—	pF
Backplane Input Leakage	$I_{IL(BP)}$	Pin 5 with Pin 36 @ V_{SS}	—	±0.01	±1	μA
Backplane Input Capacitance	$C_{I(BP)}$		—	200	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS
T_A=25° C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	TYP. VALUES	UNITS
Chip-Select Active Pulse Width	t_{csa}	See Timing Diagram	100	ns
Data Setup Time	t_{dsm}	See Timing Diagram	50	ns
Data Hold Time	t_{dhm}	See Timing Diagram	25	ns
Inter-Chip Select Time	t_{ics}	See Timing Diagram	1	μs

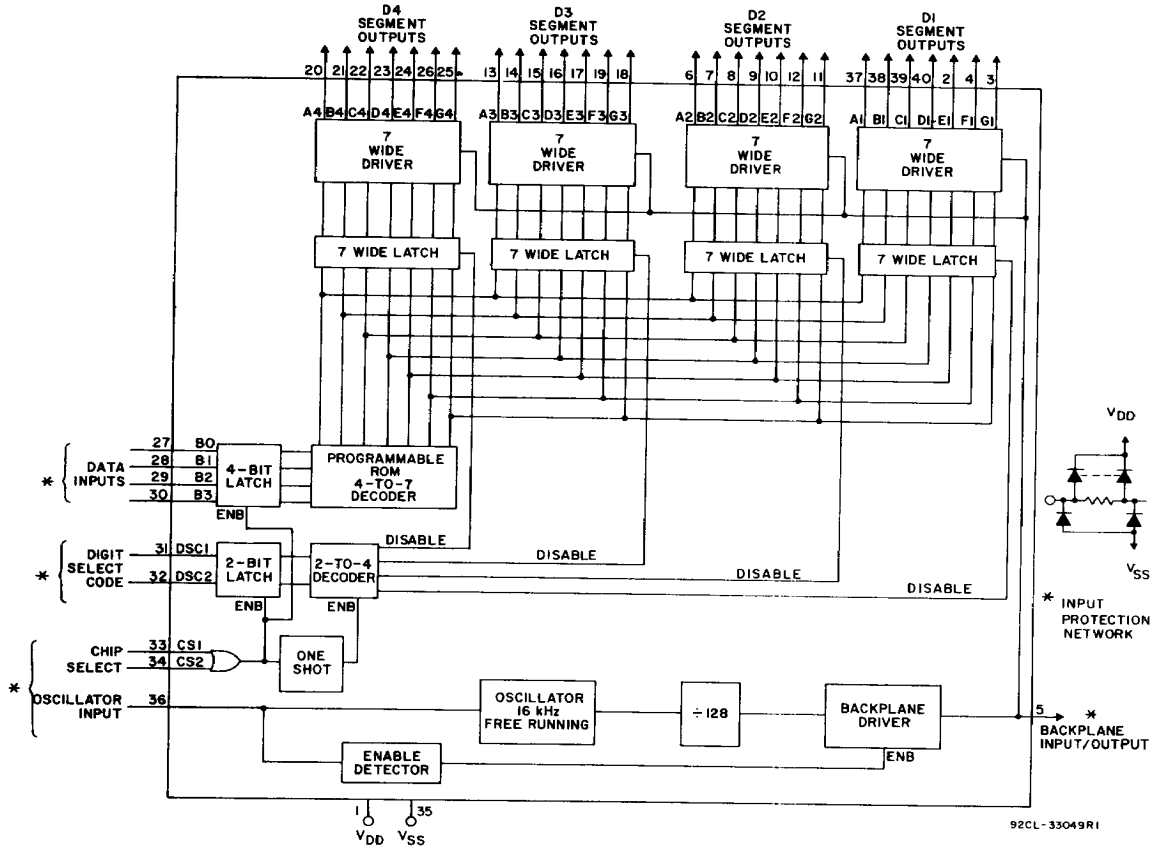


Fig. 1 - Block diagram of CD22105 and CD22105A.

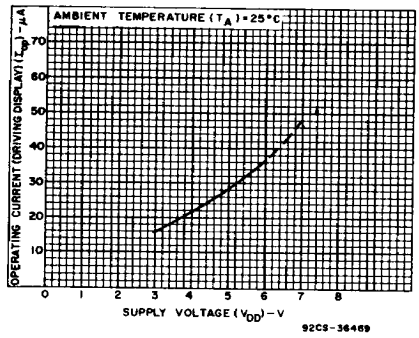


Fig. 2 - Typical operating current as a function of supply voltage.

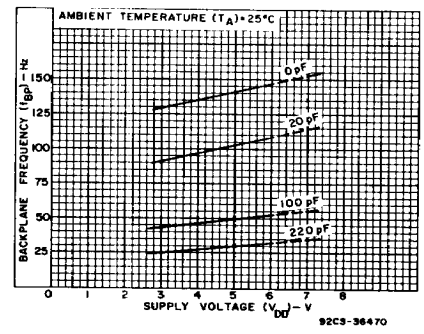


Fig. 3 - Typical backplane frequency as a function of supply voltage and external capacitance on pin 36.

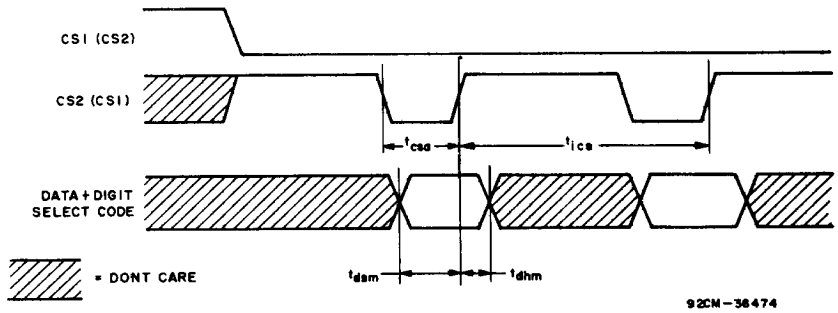


Fig. 4 - CD22105, CD22105A timing diagram.

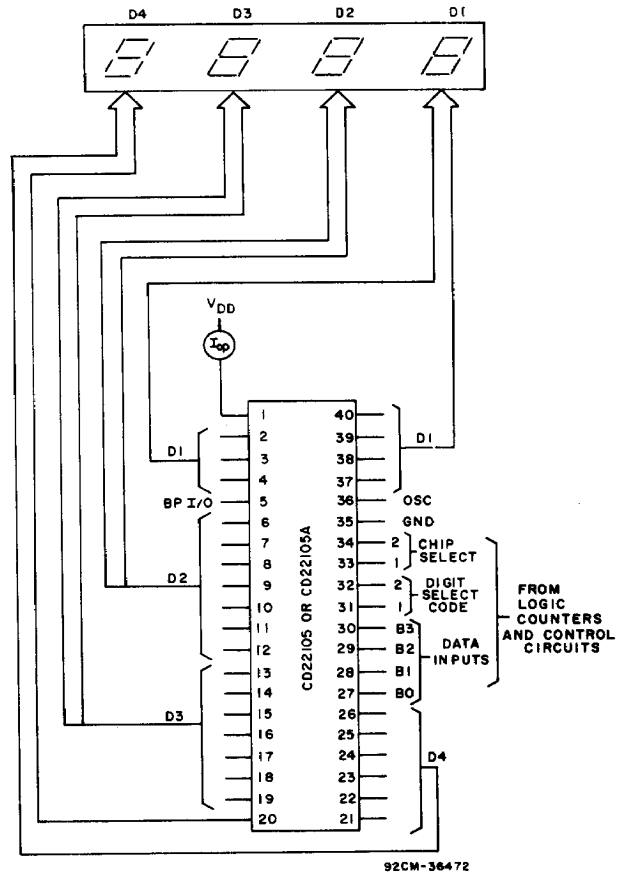


Fig. 5 - Test circuit.

Table I — Output Codes

Binary Input B3 B2 B1 B0	Display Hexadecimal CD22105	Display Decimal CD22105A
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	A	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

92CS-33150

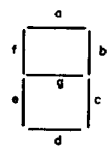
CHIP-SELECT TRUTH TABLE

Pins 33	Pins 34	Function
0	0	New inputs from μP are written into input latches
0	1	Inputs from μP are latched in input latches, decoded, and passed through selected (1 of 4) output latch to update selected digit
1	0	
1	1	

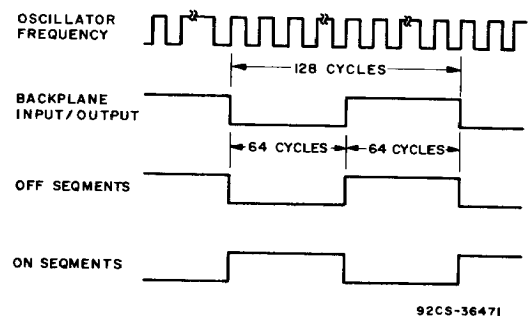
DIGIT SELECTION TRUTH TABLE

Pins 31	Pins 32	Digit Selected
1	1	D1 (LSD)
0	1	D2
1	0	D3
0	0	D4 (MSD)

DISPLAY SEGMENTS



92CS-31376



92CS-36471

Fig. 6 - Display waveforms.