

IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors



BT137X-600G

4Q Triac

1 May 2015

Product data sheet

1. General description

Planar passivated four quadrant triac in a SOT186A "full pack" plastic package intended for use in general purpose bidirectional switching and phase control applications.

2. Features and benefits

- High blocking voltage capability
- Isolated package
- Least sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants

3. Applications

- General purpose motor control
- General purpose switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20 \text{ ms}$; Fig. 4 ; Fig. 5	-	-	65	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_h \leq 73^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	8	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G+; $T_j = 25^\circ\text{C}$; Fig. 7	-	5	50	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G-; $T_j = 25^\circ\text{C}$; Fig. 7	-	8	50	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G-; $T_j = 25^\circ\text{C}$; Fig. 7	-	11	50	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G+; $T_j = 25^\circ\text{C}$; Fig. 7	-	30	100	mA



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 TO-220F (SOT186A)	
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

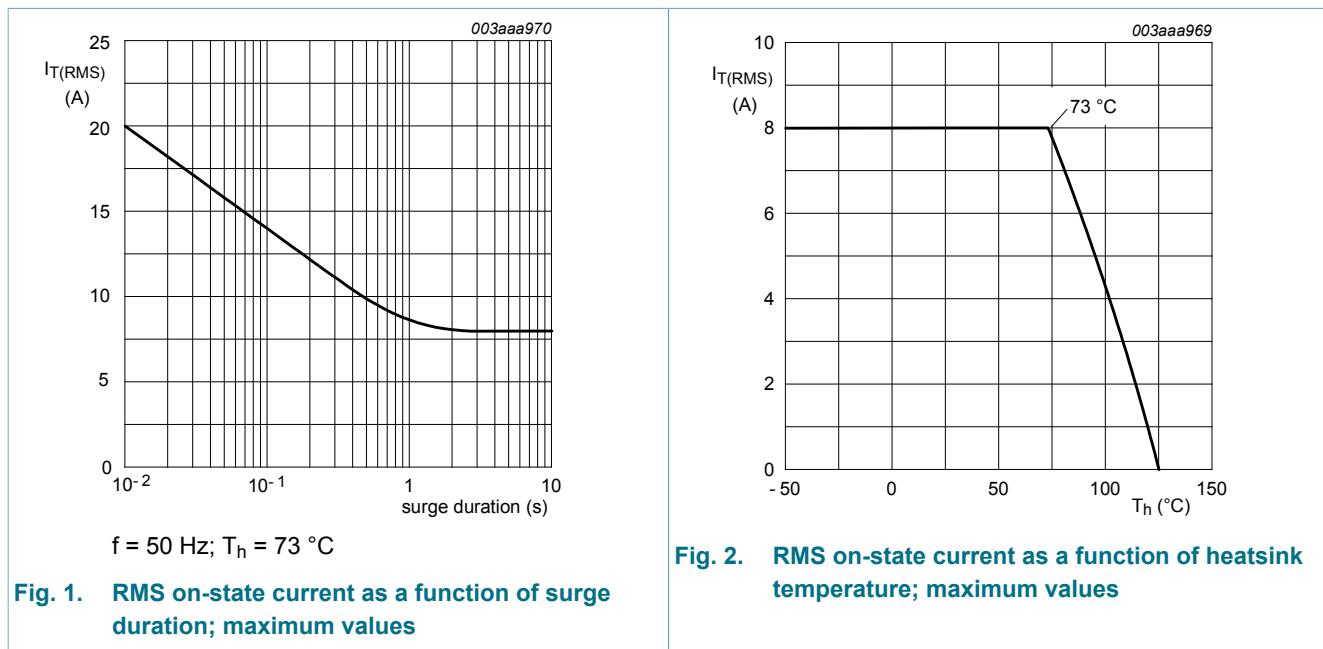
Type number	Package		
	Name	Description	Version
BT137X-600G	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 73^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3		-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5		-	65	A
		full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 16.7\text{ ms}$		-	71	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN		-	21	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 100\text{ mA}$; T2+ G+		-	50	$\text{A}/\mu\text{s}$
		$I_G = 100\text{ mA}$; T2+ G-		-	50	$\text{A}/\mu\text{s}$
		$I_G = 200\text{ mA}$; T2- G+		-	10	$\text{A}/\mu\text{s}$
		$I_G = 100\text{ mA}$; T2- G-		-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	$^\circ\text{C}$
T_j	junction temperature			-	125	$^\circ\text{C}$



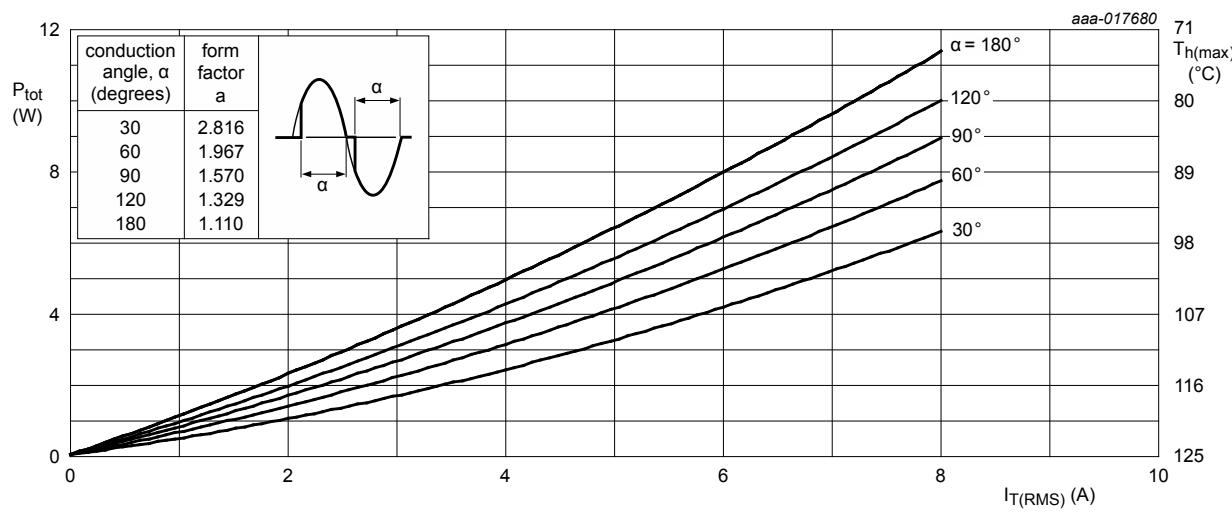


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

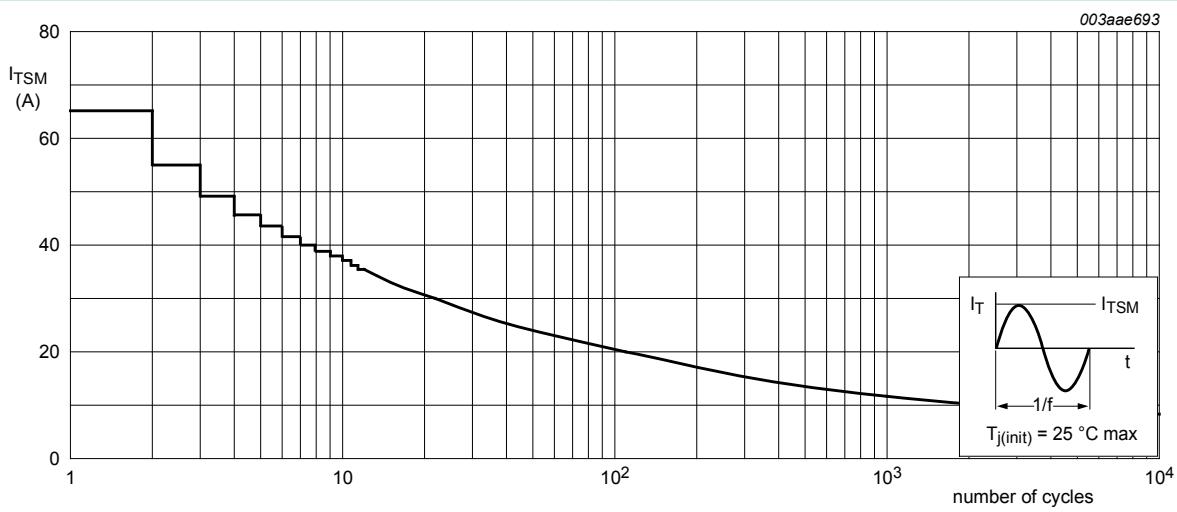


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

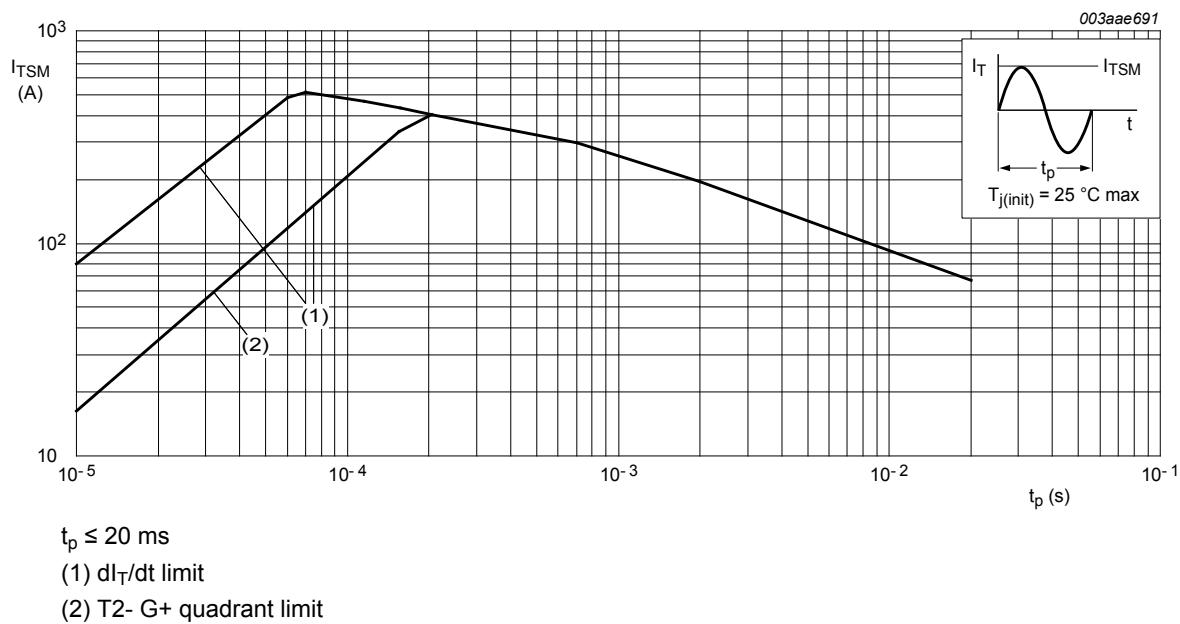
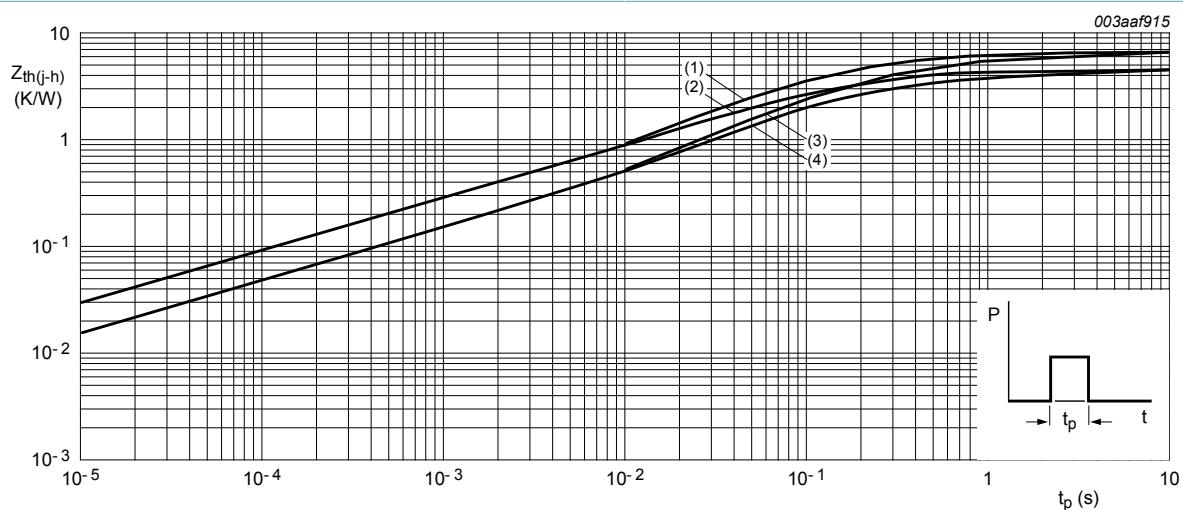


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; without heatsink compound; Fig. 6	-	-	6.5	K/W
		full or half cycle; with heatsink compound; Fig. 6	-	-	4.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



- (1) Unidirectional (half cycle) without heatsink compound
- (2) Unidirectional (half cycle) with heatsink compound
- (3) Bidirectional (full cycle) without heatsink compound
- (4) Bidirectional (full cycle) with heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50 \text{ Hz} \leq f \leq 60 \text{ Hz}$; $\text{RH} \leq 65 \%$; $T_h = 25^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1 \text{ MHz}$; $T_h = 25^\circ\text{C}$	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7		-	5	50	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7		-	8	50	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7		-	11	50	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 7		-	30	100	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8		-	7	45	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8		-	16	60	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8		-	5	45	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 8		-	7	60	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9		-	5	40	mA
V _T	on-state voltage	I _T = 10 A; T _j = 25 °C; Fig. 10		-	1.3	1.65	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11		-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11		0.25	0.4	-	V
I _D	off-state current	V _D = 600 V; T _j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit		200	250	-	V/μs
dV _{com} /dt	rate of change of commutating voltage	V _D = 400 V; T _j = 95 °C; dI _{com} /dt = 3.6 A/ms; I _T = 8 A		10	20	-	V/μs
t _{gt}	gate-controlled turn-on time	I _{TM} = 12 A; V _D = 600 V; I _G = 0.1 A; dI _G /dt = 5 A/μs		-	2	-	μs

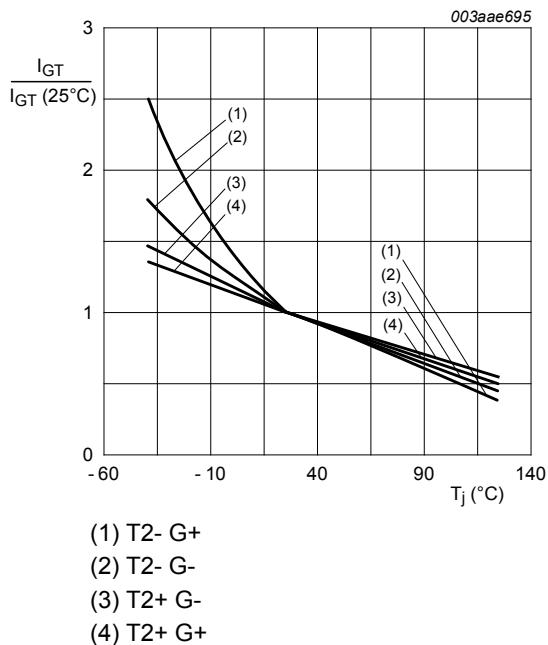


Fig. 7. Normalized gate trigger current as a function of junction temperature

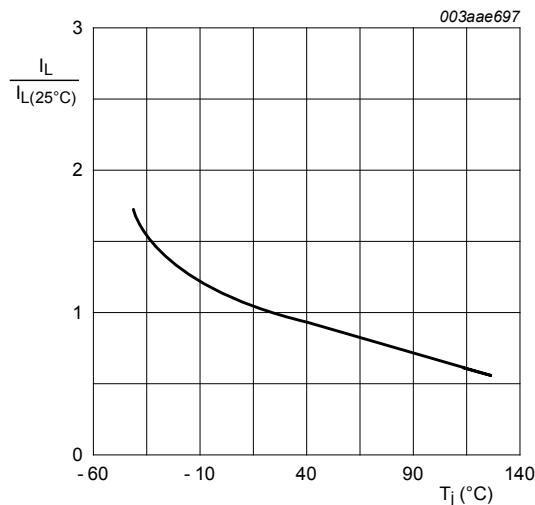


Fig. 8. Normalized latching current as a function of junction temperature

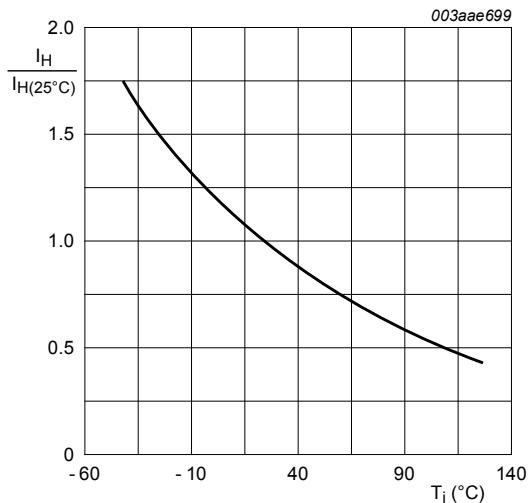


Fig. 9. Normalized holding current as a function of junction temperature

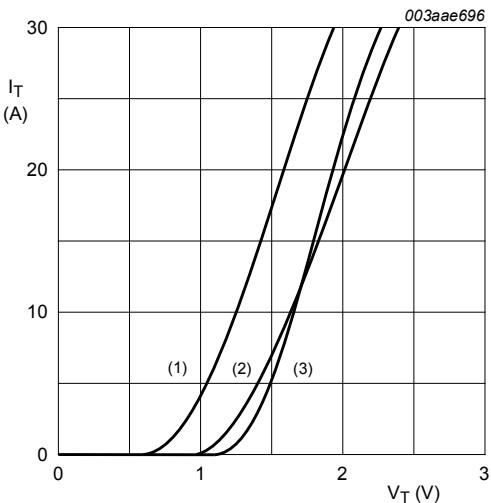


Fig. 10. On-state current as a function of on-state voltage

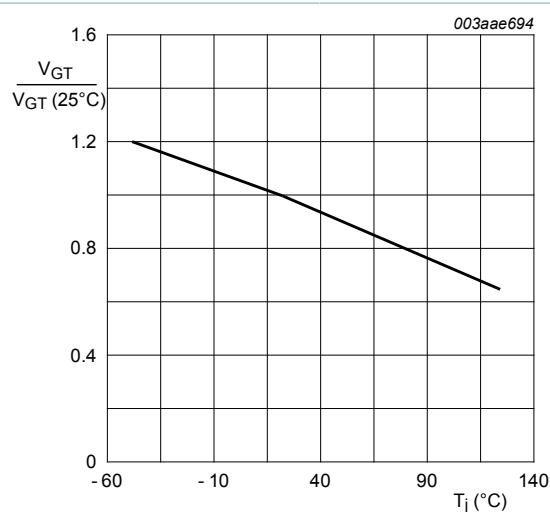
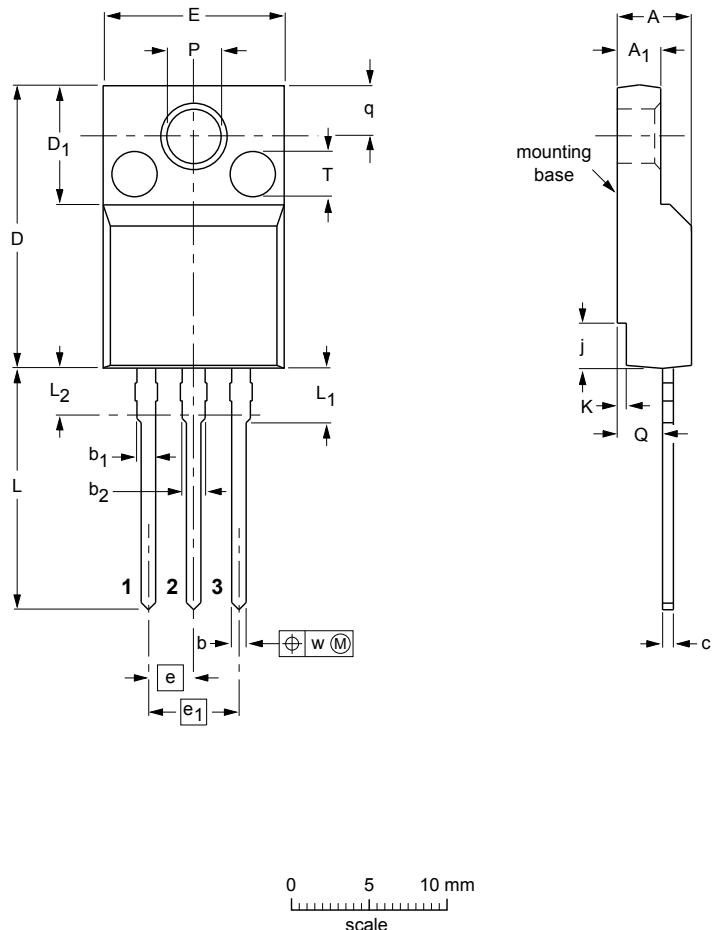


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	2.5	0.4
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7	2.54	5.08	1.7	0.4	13.5	2.79	3.0	3.0	2.3	2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are # 2.5 x 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				-02-04-09- 06-02-14

Fig. 12. Package outline TO-220F (SOT186A)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Limiting values	3
8	Thermal characteristics	6
9	Isolation characteristics	6
10	Characteristics	7
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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Date of release: 1 May 2015