

# 80C51 8-bit microcontroller family

## 8K/16K/32K Flash with 256 RAM

# 89C52/89C54/89C58

### DESCRIPTION

The 89C52/89C54/89C58 contain a non-volatile FLASH program memory that is parallel programmable. For devices that are serial programmable (In System Programmable (ISP) with a boot loader), see the 89C51RC+/89C51RD+ datasheet.

Both families are Single-Chip 8-bit Microcontrollers manufactured in advanced CMOS process and are derivatives of the 80C51 microcontroller family. All the devices have the same instruction set as the 80C51.

### SELECTION TABLE FOR FLASH DEVICES

ROM/EPROM Memory Size (X by 8)	RAM Size (X by 8)	Programmable Timer Counter (PCA)
<b>Multi-Time Programmable (MTP) devices:</b>		
<b>89C51</b>		
4K	128	No
<b>89C52/54/58</b>		
8K/16K/32K	256	No
<b>Serial In-System Programmable devices:</b>		
<b>89C51RC+</b>		
32K	512	Yes
<b>89C51RD+</b>		
64K	1024	Yes

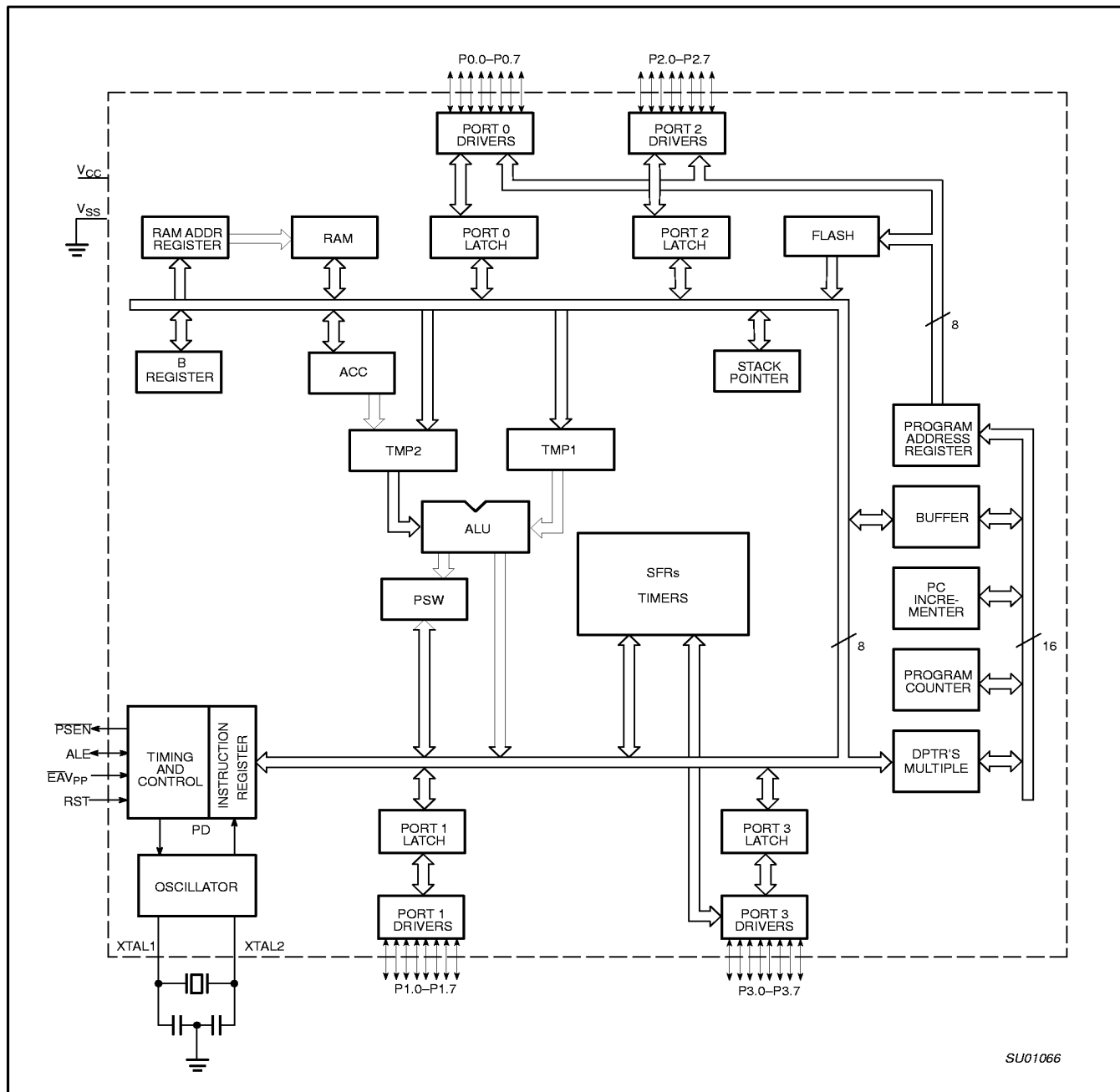
### FEATURES

- 80C51 Central Processing Unit
- On-chip FLASH Program Memory
- Speed up to 33MHz
- Full static operation
- RAM expandable externally to 64K bytes
- 4 level priority interrupt
- 6 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Clock can be stopped and resumed
  - Idle mode
  - Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)

### ORDERING INFORMATION

	MEMORY SIZE 8K × 8	MEMORY SIZE 16K × 8	MEMORY SIZE 32K × 8	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
FLASH	P89C52UBAA	P89C54UBAA	P89C58UBAA	0 to +70, Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
FLASH	P89C52UBPN	P89C54UBPN	P89C58UBPN	0 to +70, Plastic Dual In-line Package	5V	0 to 33	SOT129-1
FLASH	P89C52UBBB	P89C54UBBB	P89C58UBBB	0 to +70, Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
FLASH	P89C52UFAA	P89C54UFAA	P89C58UFAA	–40 to +85, Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
FLASH	P89C52UFPN	P89C54UFPN	P89C58UFPN	–40 to +85, Plastic Dual In-line Package	5V	0 to 33	SOT129-1
FLASH	P89C52UFBB	P89C54UFBB	P89C58UFBB	–40 to +85, Plastic Quad Flat Pack	5V	0 to 33	SOT307-2

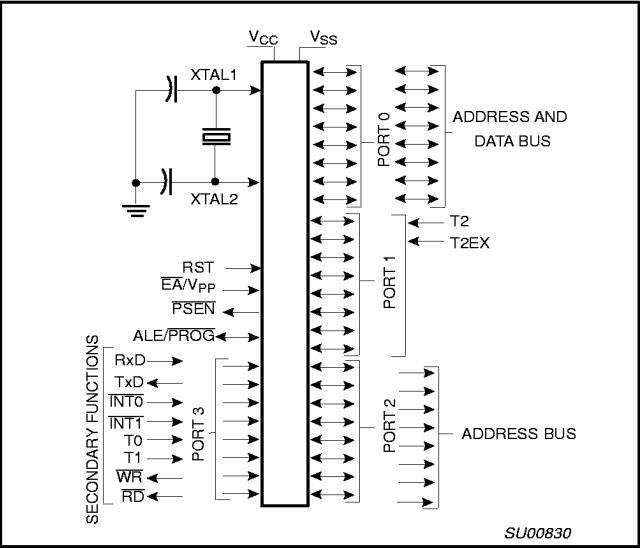
## 89C52/89C54/89C58



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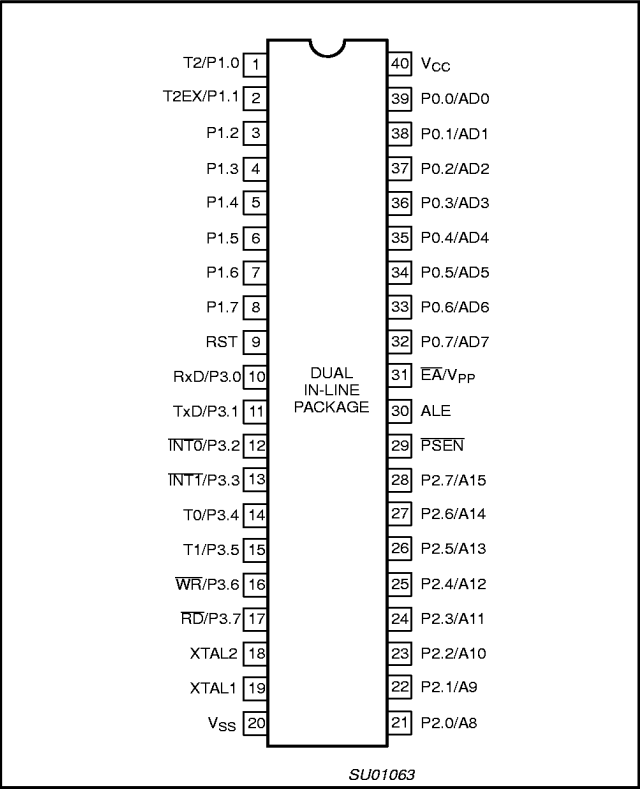
89C52/89C54/89C58

LOGIC SYMBOL

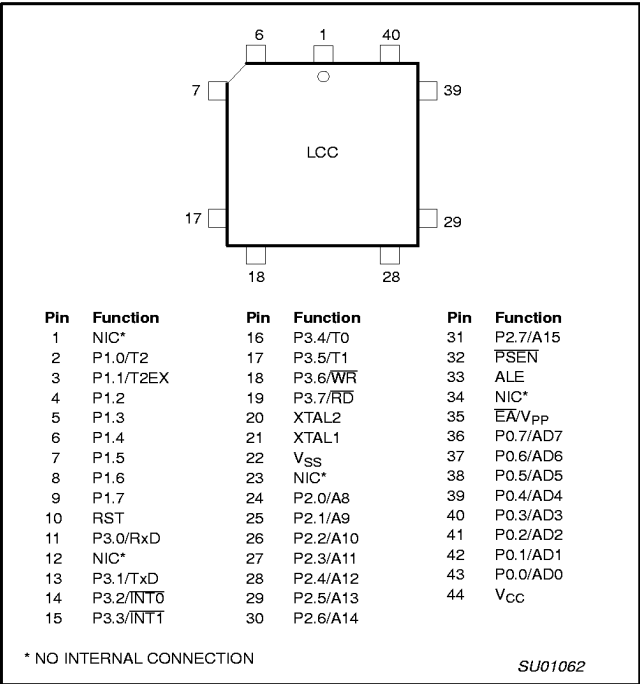


PIN CONFIGURATIONS

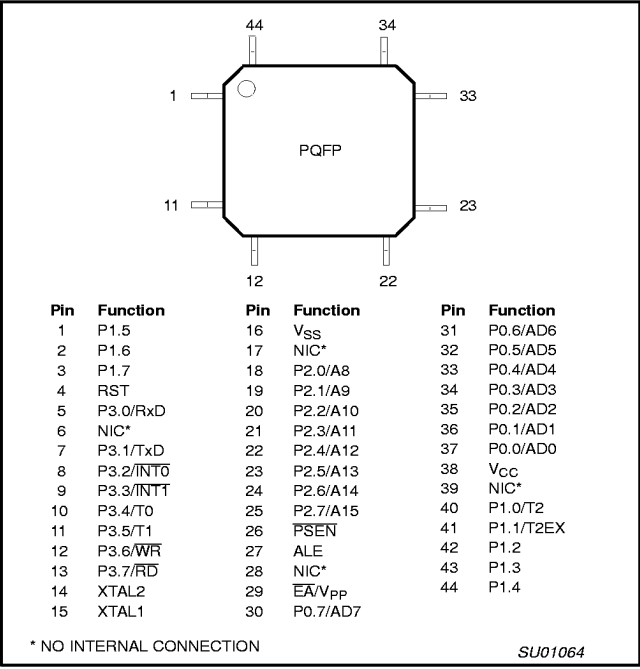
Dual In-Line Package Pin Functions



Ceramic and Plastic Leaded Chip Carrier  
Pin Functions



Plastic Quad Flat Pack Pin Functions



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### PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference.
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–36	37–30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Alternate function for Port 1: <b>T2 (P1.0):</b> Timer/Counter2 external count input/clockout (see Programmable Clock-Out). <b>T2EX (P1.1):</b> Timer/Counter2 reload/capture/direction control.
P2.0–P2.7	21–28	24–31	18–25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 3 also serves the special features of the 89C52/89C54/89C58, as listed below: <b>RxD (P3.0):</b> Serial input port <b>TxD (P3.1):</b> Serial output port <b>INT0 (P3.2):</b> External interrupt <b>INT1 (P3.3):</b> External interrupt <b>T0 (P3.4):</b> Timer 0 external input <b>T1 (P3.5):</b> Timer 1 external input <b>WR (P3.6):</b> External data memory write strobe <b>RD (P3.7):</b> External data memory read strobe
RST	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .
ALE	30	33	27	O	<b>Address Latch Enable:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V <sub>pp</sub>	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 7FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH for 8k devices, 3FFFH for 16k devices, and 7FFFH for 32k devices. The value on the EA pin is latched when RST is released and any subsequent changes have no effect. This pin also receives the 12.00V programming supply voltage (V <sub>pp</sub> ) during FLASH programming.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier.

#### NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin (other than V<sub>pp</sub>) at any time must not be higher than V<sub>CC</sub> + 0.5V or V<sub>SS</sub> – 0.5V, respectively.

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**Table 1. 89C52/89C54/89C58 Special Function Registers**

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	—	—	—	—	—	—	—	AO	xxxxxxx0B
AUXR1#	Auxiliary 1	A2H	—	—	—	—	GF2	0	—	DPS	xxxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	—	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	—	—	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	—	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xxx00000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	—	—	—	—	—	—	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
PCON#1	Power Control	87H	SMOD1	EXTRAM	—	—	GF1	GF0	PD	IDL	00xxx000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	—	P	000000x0B
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxx0B
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	—	—	—	—	—	—	T2OE	DCEN	xxxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

— Reserved bits.

1. Reset value depends on reset source.

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### FLASH EPROM MEMORY

#### General Description

The 89C52/89C54/89C58 FLASH reliably stores memory contents even after 100 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The 89C52/89C54/89C58 uses a  $12.0V \pm 0.5V$   $V_{PP}$  supply to perform the Program/Erase algorithms.

#### Features

- FLASH EPROM internal program memory with Chip Erase
- Up to 64k byte external program memory if the internal program memory is disabled ( $\overline{EA} = 0$ )
- Programming and erase voltage  $12V \pm 0.5V$
- Read/Programming/Erase:
  - Byte-wise read (100ns access time)
  - Byte Programming (20 $\mu$ S)
  - Typical erase times (including preprogramming time) of 3 sec.
- Programmable security bits
- 100 minimum erase/program cycles for each byte
- 10 year minimum data retention
- Programming support available from many popular vendors

### OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

### RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on  $V_{CC}$  and RST must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above  $V_{IH1}$  (min.) is applied to RESET.

The value on the  $\overline{EA}$  pin is latched when RST is deasserted and has no further effect.

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### LOW POWER MODES

#### Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

#### Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

#### Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0V and care must be taken to return  $V_{CC}$  to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

### Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

#### ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

- Pull ALE low while the device is in reset and  $\overline{PSEN}$  is high;
- Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and  $\overline{PSEN}$  are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

#### Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

- to input the external clock for Timer/Counter 2, or
- to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

**Table 2. External Pin Status During Idle and Power-Down Mode**

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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### TIMER 2 OPERATION

#### Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by  $C/T2^*$  in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

#### Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by  $C/T2^*$  in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2=1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.).

#### Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter [ $C/T2^*$  in T2CON]) then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see

Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

		(MSB)							(LSB)
		TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/T2^*$	CP/RL2
Symbol	Position	Name and Significance							
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.							
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).							
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.							
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.							
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.							
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.							
$C/T2^*$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).							
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.							

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Figure 1. Timer/Counter 2 (T2CON) Control Register

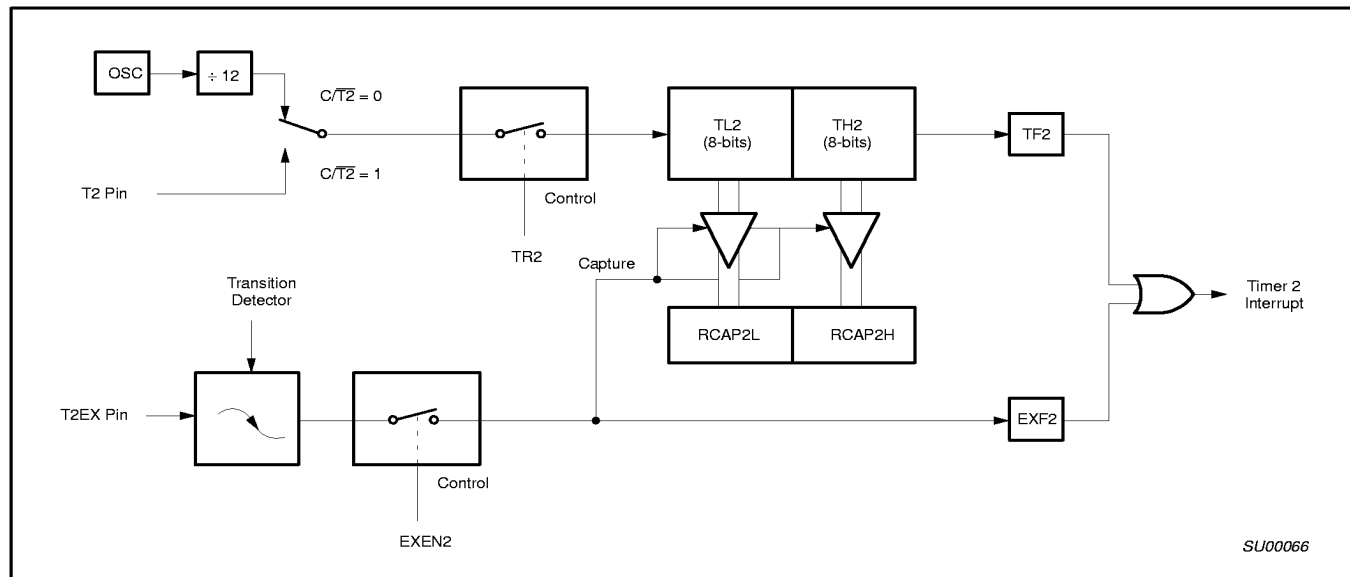


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### Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)



### Figure 2. Timer 2 in Capture Mode

**T2MOD** Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit	7	6	5	4	3	2	1 0

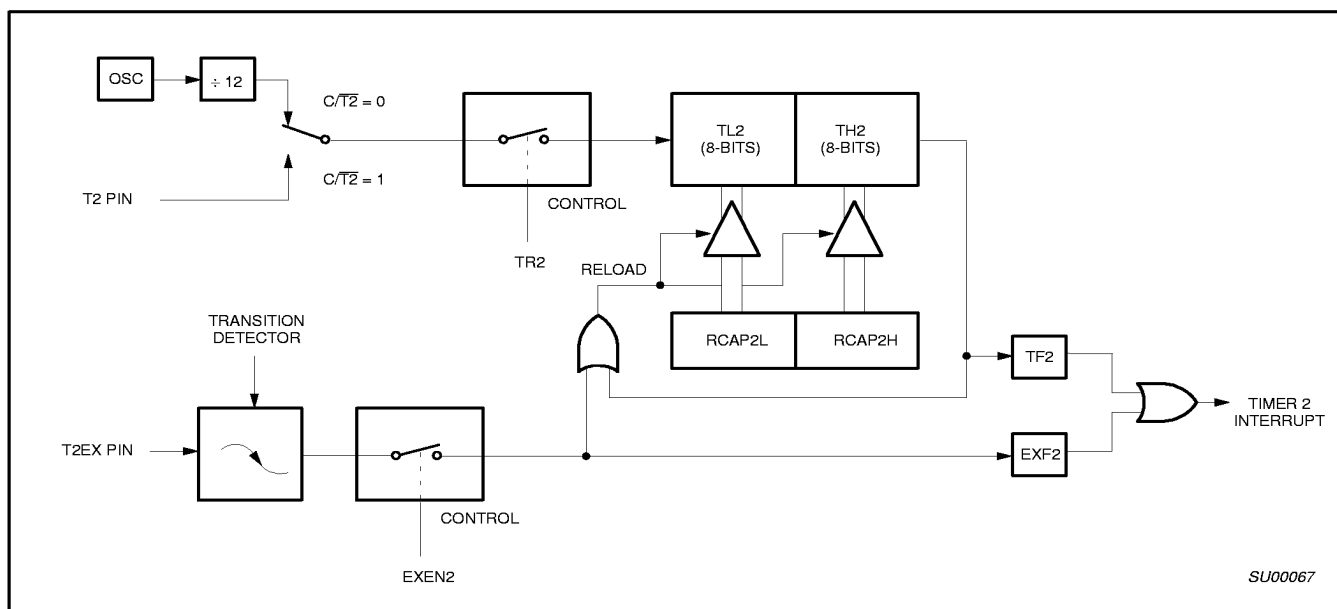
Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

\* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

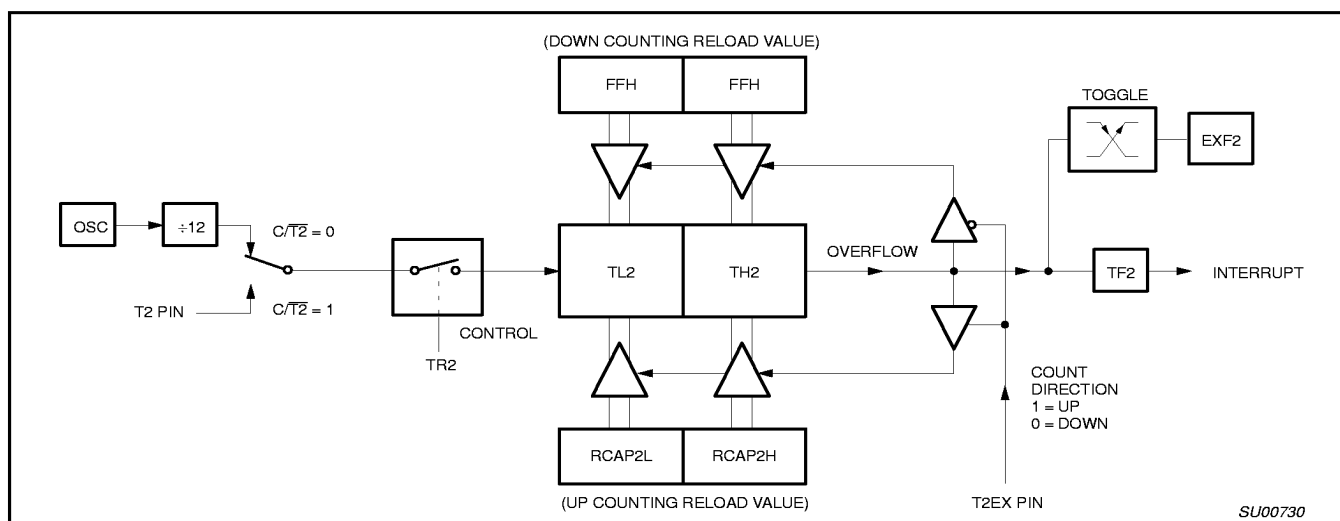
### Figure 3. Timer 2 Mode (T2MOD) Control Register

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**Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)**



**Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)**

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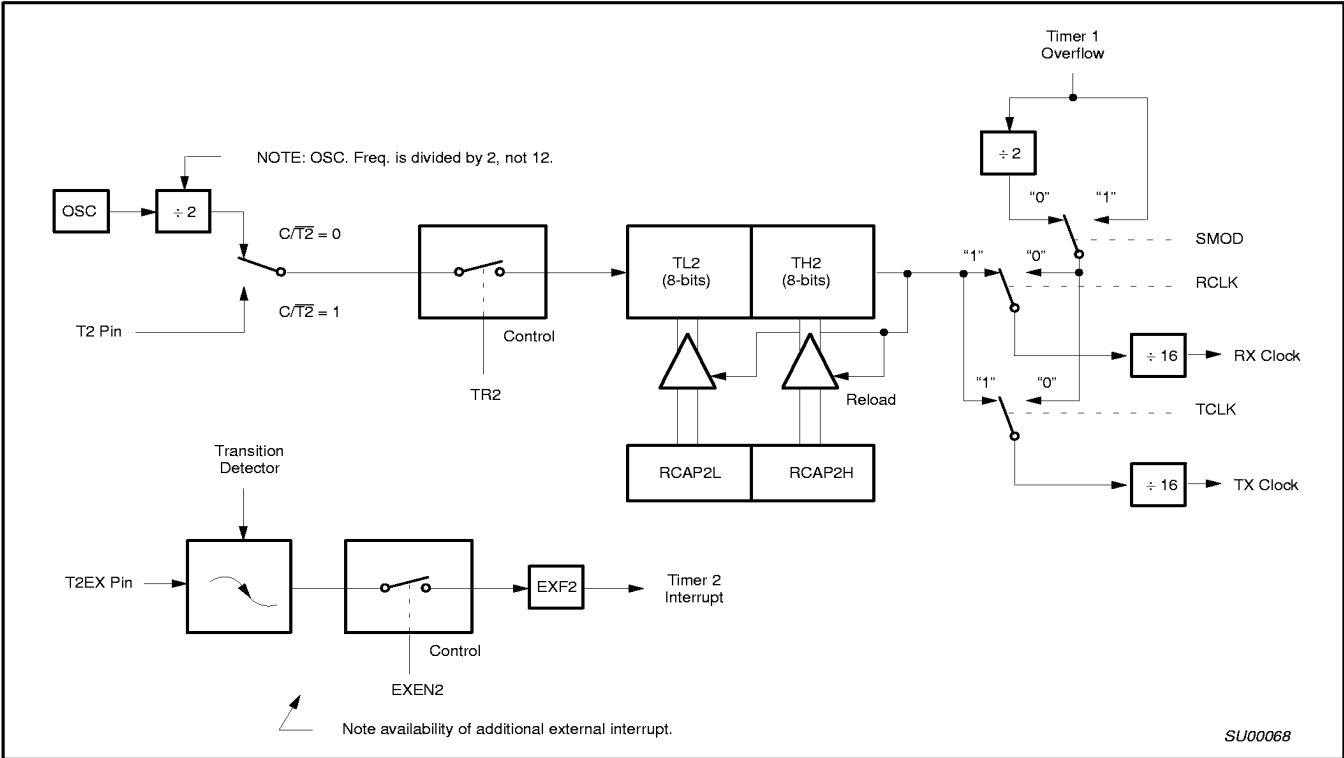


Figure 6. Timer 2 in Baud Rate Generator Mode

Table 4. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375K	12MHz	FF	FF
9.6K	12MHz	FF	D9
2.8K	12MHz	FF	B2
2.4K	12MHz	FF	64
1.2K	12MHz	FE	C8
300	12MHz	FB	1E
110	12MHz	F2	AF
300	6MHz	FD	8F
110	6MHz	F9	57

Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 4) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

Modes 1 and 3 Baud Rates =  $\frac{\text{Timer 2 Overflow Rate}}{16}$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/T2=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

Modes 1 and 3 Baud Rates =  $\frac{\text{Oscillator Frequency}}{[32 \times [65536 - (RCAP2H, RCAP2L)]]}$

Where: (RCAP2H, RCAP2L) = The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

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When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time ( $f_{osc}/2$ ) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

### Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{osc}}{[32 \times [65536 - (RCAP2H, RCAP2L)]]}$$

Where  $f_{osc}$  = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$RCAP2H, RCAP2L = 65536 - \frac{f_{osc}}{32 \times \text{Baud Rate}}$$

### Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

**Table 5. Timer 2 as a Timer**

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

**Table 6. Timer 2 as a Counter**

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

#### NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

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### Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

### Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1101</u>
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	<u>1111 1110</u>
	Given =	1100 00X0

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1001</u>
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	<u>1111 1010</u>
	Given =	1110 0XX0
Slave 2	SADDR =	1110 0000
	SADEN =	<u>1111 1100</u>
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

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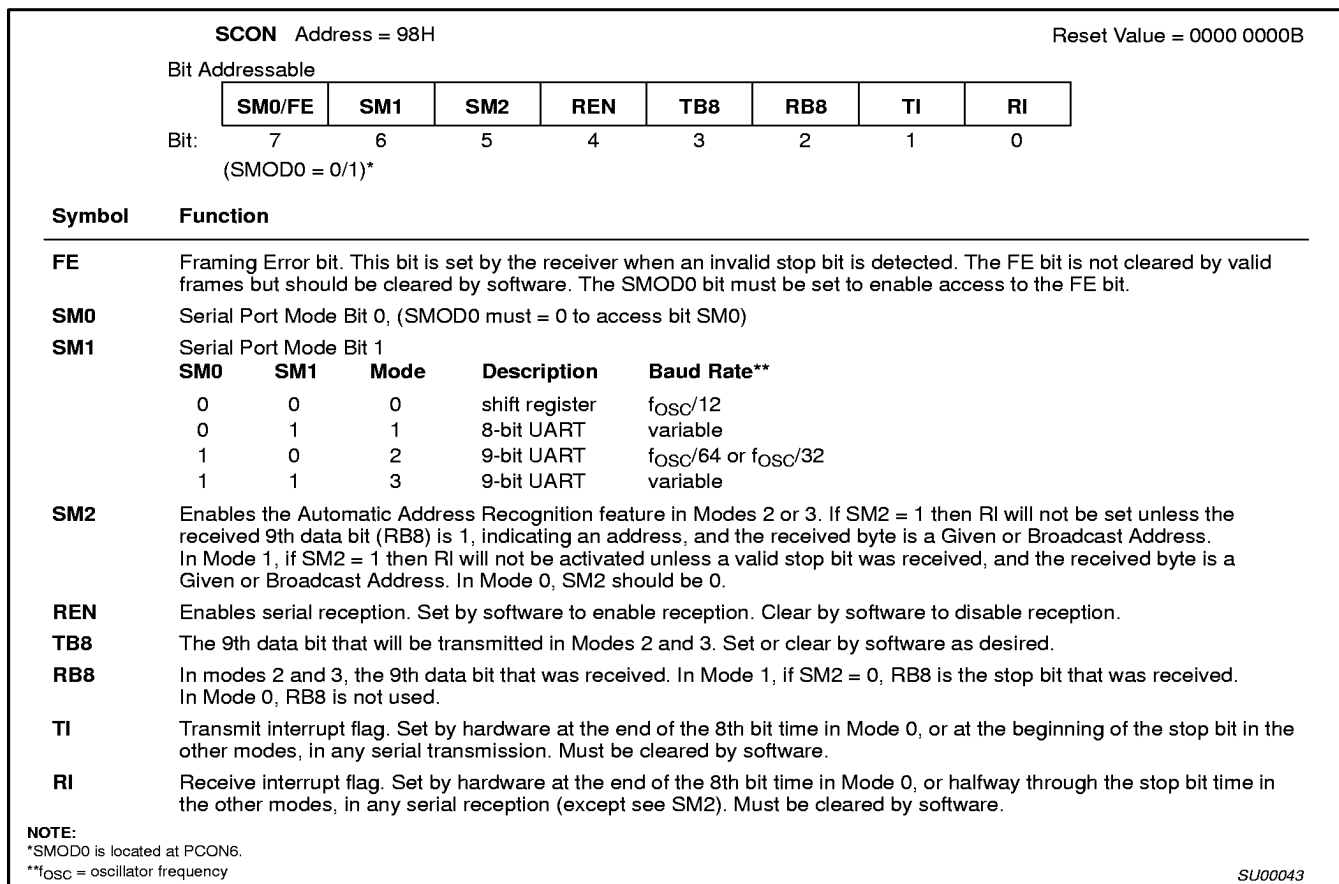
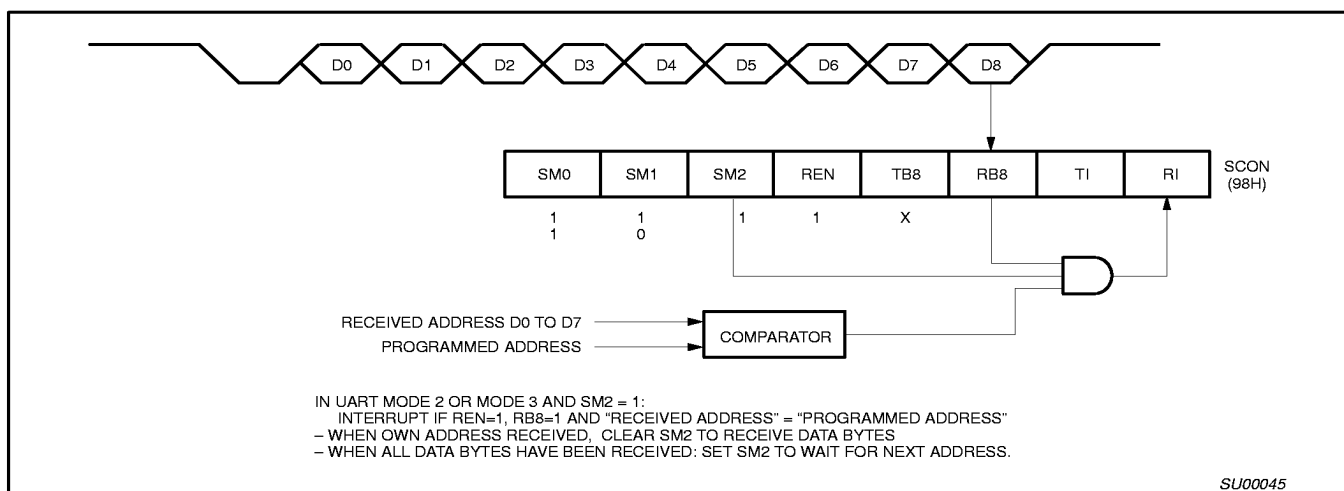
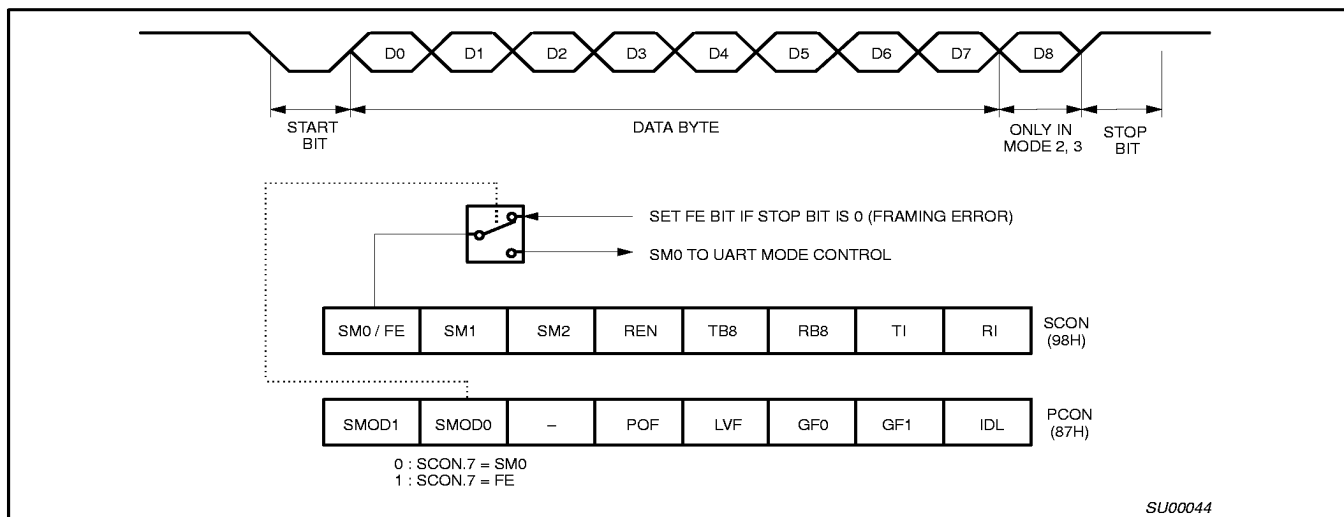


Figure 7. SCON: Serial Port Control Register

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### Interrupt Priority Structure

The 89C52/89C54/89C58 have a 6-source four-level interrupt structure.

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

The function of the IPH SFR is simple and when combined with the IE SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

**Table 7. Interrupt Table**

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L) <sup>1</sup> Y (T) <sup>2</sup>	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
SP	5	RI, TI	N	23H
T2	6	TF2, EXF2	N	2BH

**NOTES:**

1. L = Level activated
2. T = Transition activated

		7	6	5	4	3	2	1	0
<b>IE (0A8H)</b>		EA	—	ET2	ES	ET1	EX1	ET0	EX0
		Enable Bit = 1 enables the interrupt. Enable Bit = 0 disables it.							
<b>BIT</b>	<b>SYMBOL</b>	<b>FUNCTION</b>							
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.							
IE.6	—	Not implemented. Reserved for future use.							
IE.5	ET2	Timer 2 interrupt enable bit.							
IE.4	ES	Serial Port interrupt enable bit.							
IE.3	ET1	Timer 1 interrupt enable bit.							
IE.2	EX1	External interrupt 1 enable bit.							
IE.1	ET0	Timer 0 interrupt enable bit.							
IE.0	EX0	External interrupt 0 enable bit.							

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**Figure 10. IE Registers**



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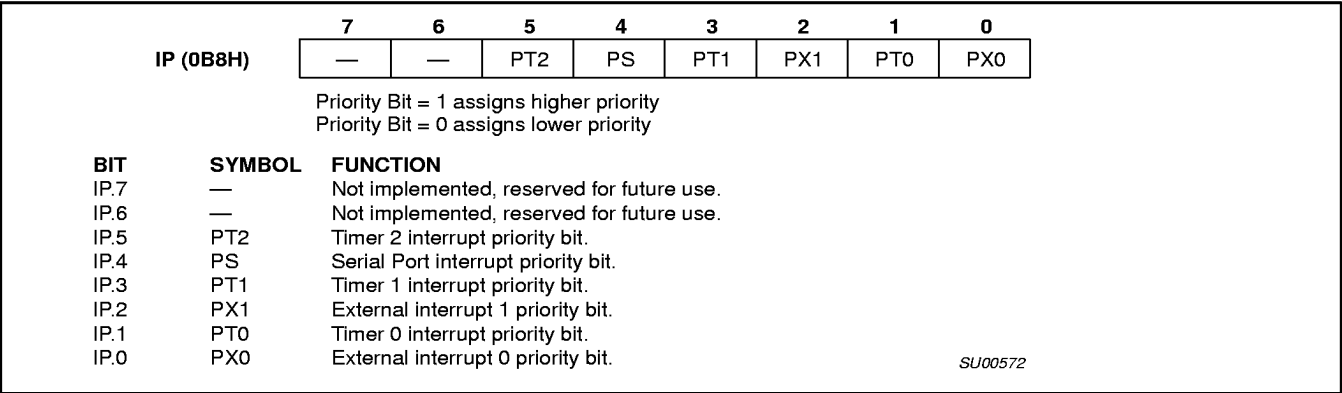


Figure 11. IP Registers

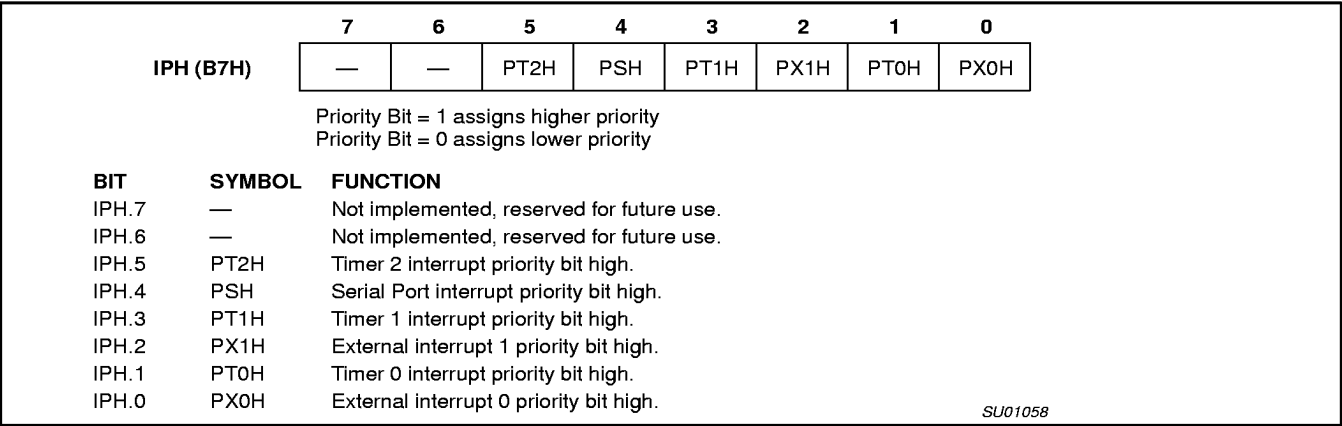


Figure 12. IPH Registers

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### Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

### Reduced EMI Mode

#### AUXR (8EH)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	AO

AUXR.0

AO

Turns off ALE output.

### Dual DPTR

The dual DPTR structure (see Figure 13) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxxxxx0B

#### AUXR1 (A2H)

7	6	5	4	3	2	1	0
—	—	—	—	GF2	0	—	DPS

Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF0 bit is a general purpose user-defined flag. Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF2 bit.

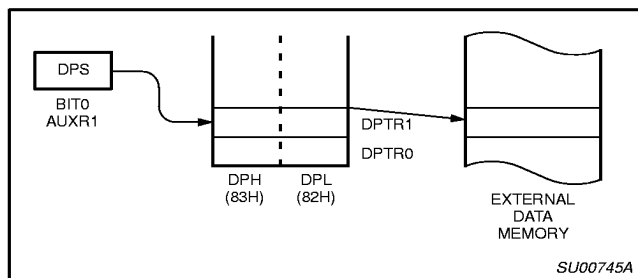


Figure 13.

### DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR, A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

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### ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on EA/V <sub>PP</sub> pin to V <sub>SS</sub>	0 to +13.0	V
Voltage on any other pin to V <sub>SS</sub>	-0.5 to +6.5	V
Maximum I <sub>OL</sub> per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

#### NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.

### AC ELECTRICAL CHARACTERISTICS

T<sub>amb</sub> = 0°C to +70°C or -40°C to +85°C

SYMBOL	PARAMETER	CLOCK FREQUENCY RANGE -f		UNIT
		MIN	MAX	
1/t <sub>CLCL</sub>	Oscillator frequency: U (33MHz)	0	33	MHz

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### DC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}; 5\text{V} \pm 10\%; V_{SS} = 0\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>1</sup>	MAX	
$V_{IL}$	Input low voltage	$4.5\text{V} < V_{CC} < 5.5\text{V}$	-0.5		$0.2V_{CC} - 0.1$	V
$V_{IH}$	Input high voltage (ports 0, 1, 2, 3, $\overline{\text{EA}}$ )		$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V
$V_{IH1}$	Input high voltage, XTAL1, RST		$0.7V_{CC}$		$V_{CC} + 0.5$	V
$V_{OL}$	Output low voltage, ports 1, 2, 3 <sup>8</sup>	$V_{CC} = 4.5\text{V}$ $I_{OL} = 1.6\text{mA}^2$			0.4	V
$V_{OL1}$	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$ <sup>7, 8</sup>	$V_{CC} = 4.5\text{V}$ $I_{OL} = 3.2\text{mA}^2$			0.4	V
$V_{OH}$	Output high voltage, ports 1, 2, 3 <sup>3</sup>	$V_{CC} = 4.5\text{V}$ $I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
$V_{OH1}$	Output high voltage (port 0 in external bus mode), ALE <sup>9</sup> , $\overline{\text{PSEN}}$ <sup>3</sup>	$V_{CC} = 4.5\text{V}$ $I_{OH} = -3.2\text{mA}$	$V_{CC} - 0.7$			V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{V}$	-1		-75	$\mu\text{A}$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3 <sup>6</sup>	$V_{IN} = 2.0\text{V}$ See note 4			-650	$\mu\text{A}$
$I_{LI}$	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			$\pm 10$	$\mu\text{A}$
$I_{CC}$	Power supply current (see Figure 21): Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 25 for conditions)	See note 5  $T_{amb} = 0^{\circ}\text{C to } 70^{\circ}\text{C}$ $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		3	100 125	$\mu\text{A}$ $\mu\text{A}$
$R_{RST}$	Internal reset pull-down resistor		40		225	k $\Omega$
$C_{IO}$	Pin capacitance <sup>10</sup> (except $\overline{\text{EA}}$ )				15	pF

#### NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the  $V_{OL}$ s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.  $I_{OL}$  can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and  $\overline{\text{PSEN}}$  to momentarily fall below the  $V_{CC} - 0.7$  specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when  $V_{IN}$  is approximately 2V.
- See Figures 22 through 25 for  $I_{CC}$  test conditions and Figure 21 for  $I_{CC}$  vs Freq.  
Active mode:  $I_{CC}(\text{MAX}) = (0.9 \times \text{FREQ.} + 20)\text{mA}$   
Idle mode:  $I_{CC}(\text{MAX}) = (0.37 \times \text{FREQ.} + 1.0)\text{mA}$
- This value applies to  $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ .
- Load capacitance for port 0, ALE, and  $\overline{\text{PSEN}} = 100\text{pF}$ , load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
Maximum  $I_{OL}$  per port pin: 15mA (\*NOTE: This is 85°C specification.)  
Maximum  $I_{OL}$  per 8-bit port: 26mA  
Maximum total  $I_{OL}$  for all outputs: 71mA  
If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to  $V_{OH1}$ , except when ALE is off then  $V_{OH}$  is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except  $\overline{\text{EA}}$  is 25pF).

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### AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}^{1, 2, 3}$

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK <sup>4</sup>		33MHz CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	14	Oscillator frequency Speed versions: I;J;U (33MHz)	3.5	33	3.5	33	MHz
$t_{LHLL}$	14	ALE pulse width	$2t_{CLCL}-40$		21		ns
$t_{AVLL}$	14	Address valid to ALE low	$t_{CLCL}-25$		5		ns
$t_{LLAX}$	14	Address hold after ALE low	$t_{CLCL}-25$		5		ns
$t_{LLIV}$	14	ALE low to valid instruction in		$4t_{CLCL}-65$		55	ns
$t_{LLPL}$	14	ALE low to PSEN low	$t_{CLCL}-25$		5		ns
$t_{PLPH}$	14	PSEN pulse width	$3t_{CLCL}-45$		45		ns
$t_{PLIV}$	14	PSEN low to valid instruction in		$3t_{CLCL}-60$		30	ns
$t_{PXIX}$	14	Input instruction hold after PSEN	0		0		ns
$t_{PXIZ}$	14	Input instruction float after PSEN		$t_{CLCL}-25$		5	ns
$t_{AVIV}$	14	Address to valid instruction in		$5t_{CLCL}-80$		70	ns
$t_{PLAZ}$	14	PSEN low to address float		10		10	ns
<b>Data Memory</b>							
$t_{RLRH}$	15, 16	RD pulse width	$6t_{CLCL}-100$		82		ns
$t_{WLWH}$	15, 16	WR pulse width	$6t_{CLCL}-100$		82		ns
$t_{RLDV}$	15, 16	RD low to valid data in		$5t_{CLCL}-90$		60	ns
$t_{RHDX}$	15, 16	Data hold after RD	0		0		ns
$t_{RHDZ}$	15, 16	Data float after RD		$2t_{CLCL}-28$		32	ns
$t_{LLDV}$	15, 16	ALE low to valid data in		$8t_{CLCL}-150$		90	ns
$t_{AVDV}$	15, 16	Address to valid data in		$9t_{CLCL}-165$		105	ns
$t_{LLWL}$	15, 16	ALE low to RD or WR low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	40	140	ns
$t_{AVWL}$	15, 16	Address valid to WR low or RD low	$4t_{CLCL}-75$		45		ns
$t_{QVWX}$	15, 16	Data valid to WR transition	$t_{CLCL}-30$		0		ns
$t_{WHQX}$	15, 16	Data hold after WR	$t_{CLCL}-25$		5		ns
$t_{QVWH}$	16	Data valid to WR high	$7t_{CLCL}-130$		80		ns
$t_{RLAZ}$	15, 16	RD low to address float		0		0	ns
$t_{WHLH}$	15, 16	RD or WR high to ALE high	$t_{CLCL}-25$	$t_{CLCL}+25$	5	55	ns
<b>External Clock</b>							
$t_{CHCX}$	18	High time	17	$t_{CLCL}-t_{CLCX}$			ns
$t_{CLCX}$	18	Low time	17	$t_{CLCL}-t_{CHCX}$			ns
$t_{CLCH}$	18	Rise time		5			ns
$t_{CHCL}$	18	Fall time		5			ns
<b>Shift Register</b>							
$t_{XLXL}$	17	Serial port clock cycle time	$12t_{CLCL}$		360		ns
$t_{QVXH}$	17	Output data setup to clock rising edge	$10t_{CLCL}-133$		167		ns
$t_{XHGX}$	17	Output data hold after clock rising edge	$2t_{CLCL}-80$		50		ns
$t_{XHDX}$	17	Input data hold after clock rising edge	0		0		ns
$t_{XHDV}$	17	Clock rising edge to input data valid		$10t_{CLCL}-133$		167	ns

#### NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the microcontroller to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- Parts are guaranteed to operate down to 0Hz.

80C51 8-bit microcontroller family  
8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

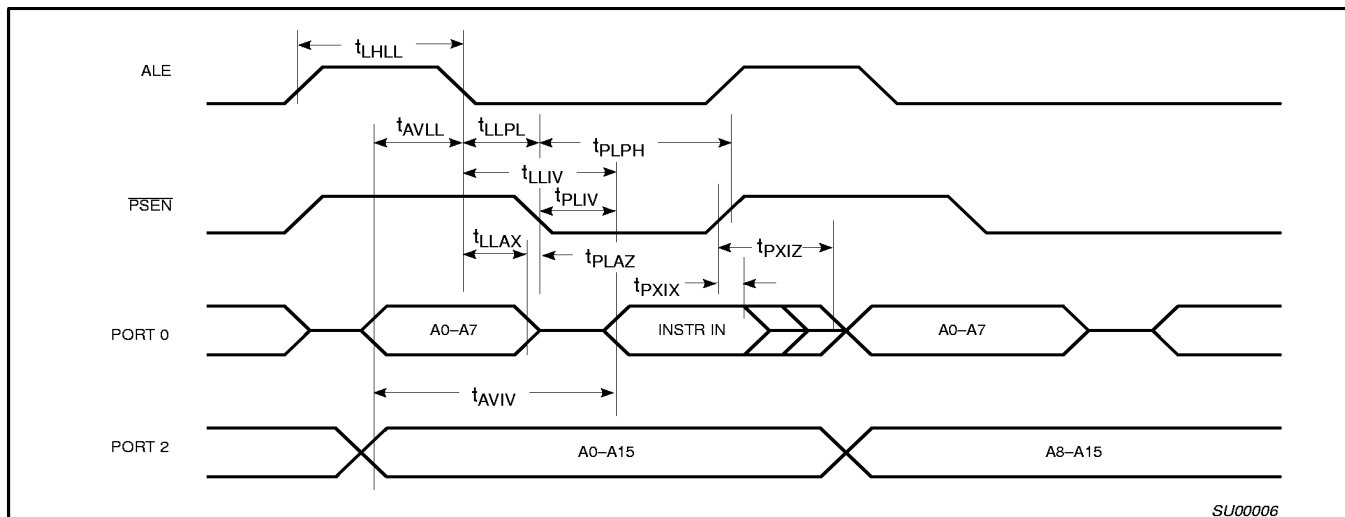
## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address  
C – Clock  
D – Input data  
H – Logic level high  
I – Instruction (program memory contents)  
L – Logic level low, or ALE

P – PSEN  
 Q – Output data  
 R – RD signal  
 t – Time  
 V – Valid  
 W – WR signal  
 X – No longer a valid logic level  
 Z – Float

**Examples:**  $t_{AVLL}$  = Time for address valid to ALE low.  
 $t_{LLPL}$  = Time for ALE low to  $\overline{PSEN}$  low.



### Figure 14. External Program Memory Read Cycle

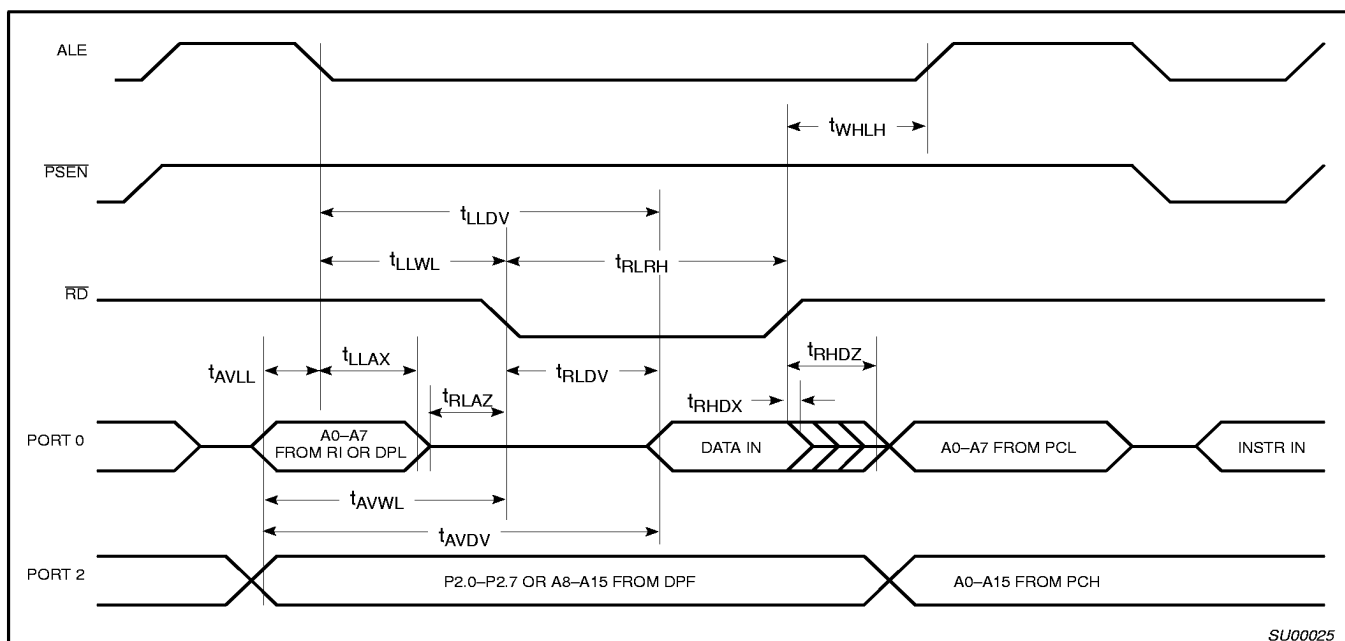


Figure 15. External Data Memory Read Cycle

80C51 8-bit microcontroller family  
8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

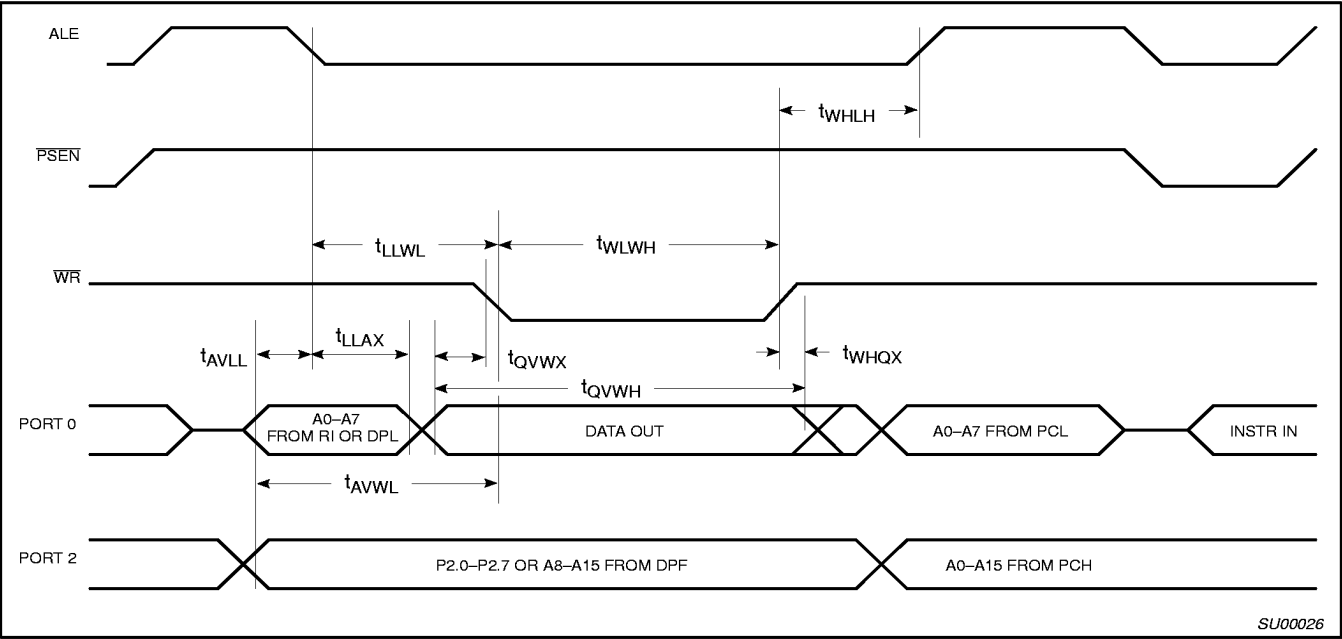


Figure 16. External Data Memory Write Cycle

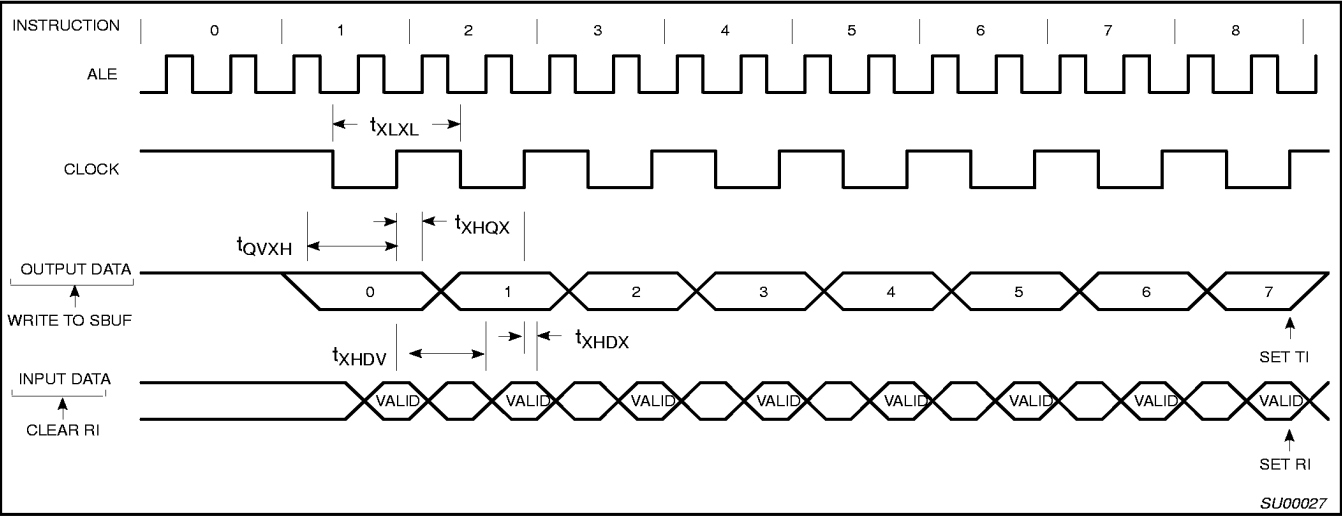


Figure 17. Shift Register Mode Timing

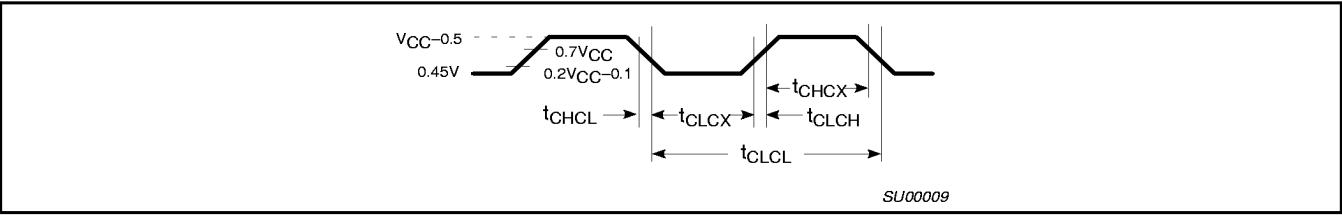


Figure 18. External Clock Drive

80C51 8-bit microcontroller family  
8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

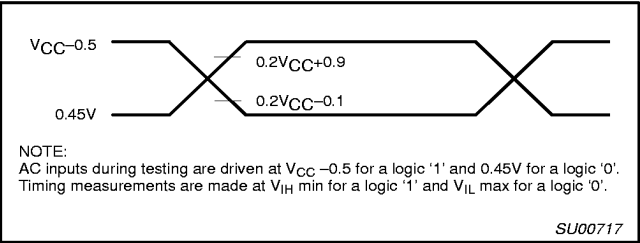


Figure 19. AC Testing Input/Output

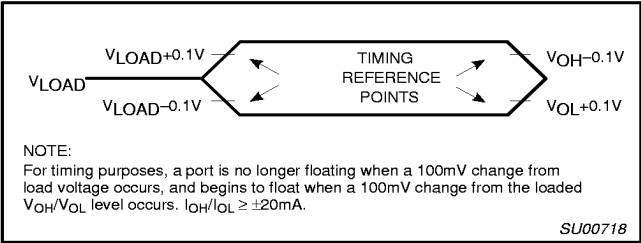


Figure 20. Float Waveform

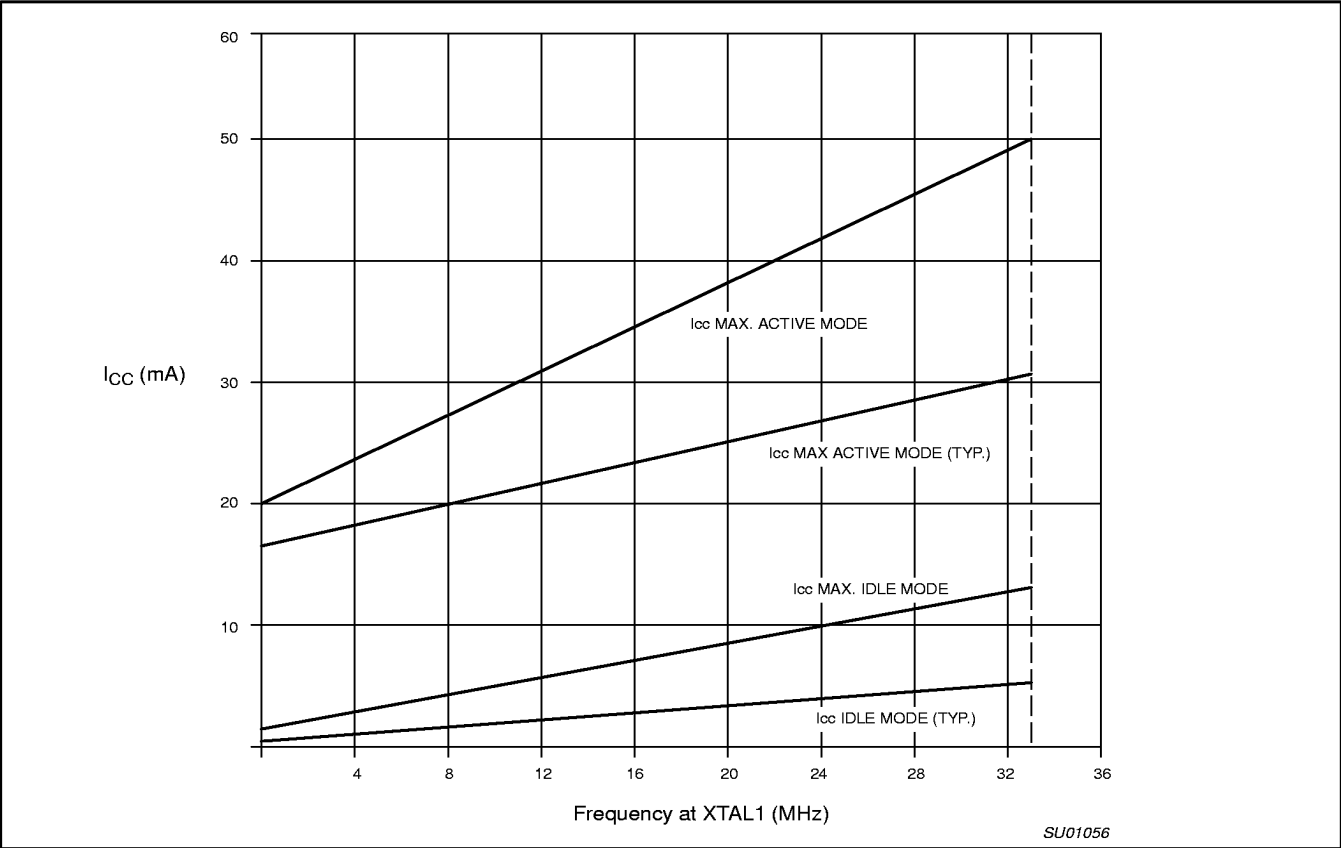


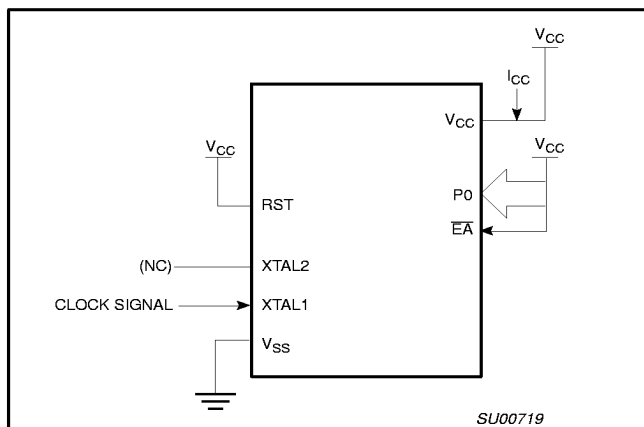
Figure 21.  $I_{CC}$  vs. FREQ  
Valid only within frequency specifications of the device under test



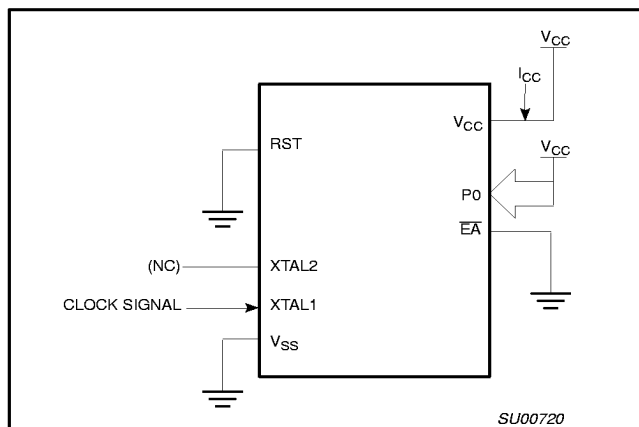
# 80C51 8-bit microcontroller family

## 8K/16K/32K Flash with 256 RAM

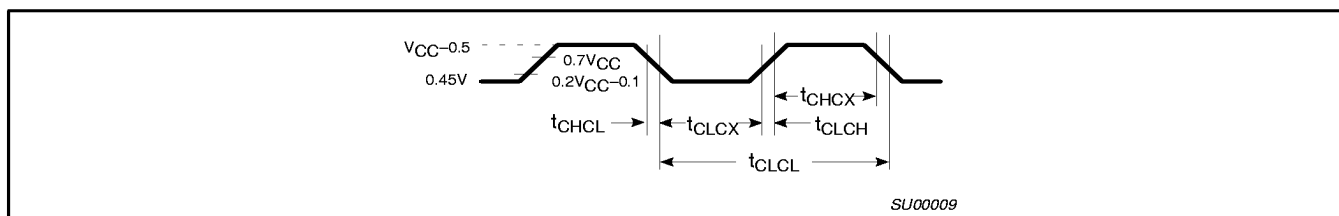
89C52/89C54/89C58



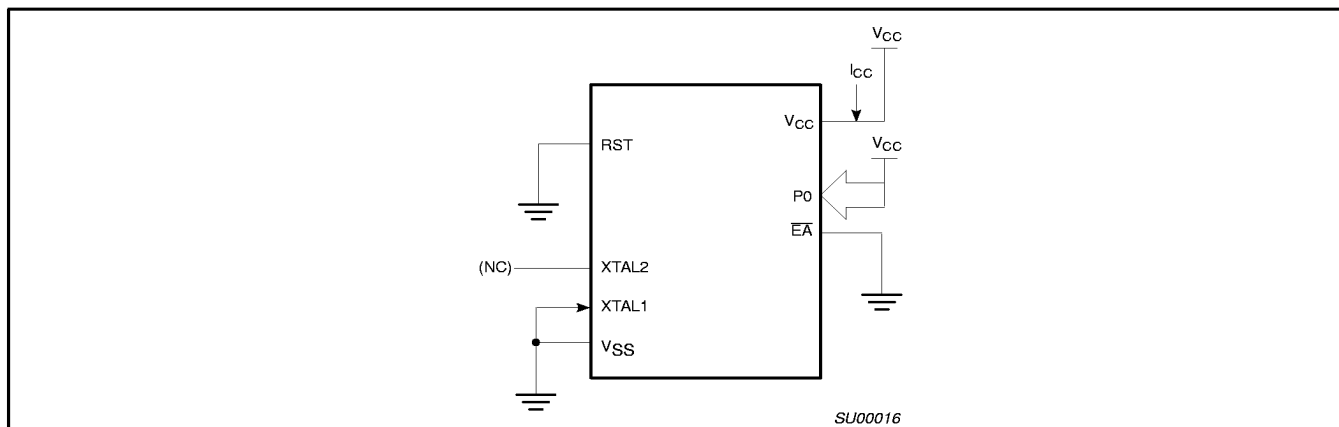
**Figure 22.  $I_{CC}$  Test Condition, Active Mode**  
All other pins are disconnected



**Figure 23.  $I_{CC}$  Test Condition, Idle Mode**  
All other pins are disconnected



**Figure 24. Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes**  
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$



**Figure 25.  $I_{CC}$  Test Condition, Power Down Mode**  
All other pins are disconnected.  $V_{CC} = 2\text{V to } 5.5\text{V}$

# 80C51 8-bit microcontroller family

## 8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

### Security

The security feature protects against software piracy and prevents the contents of the FLASH from being read. The Security Lock bits are located in FLASH. The 89C52/89C54/89C58 has 3 programmable security lock bits that will provide different levels of protection for the on-chip code and data (see Table 8).

**Table 8.**

SECURITY LOCK BITS <sup>1</sup>				PROTECTION DESCRIPTION
Level	LB1	LB2	LB3	
1	0	0	0	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory.
2	1	0	0	Same as level 1
3	1	1	0	Same as level 1, plus program verification is disabled
4	1	1	1	Same as level 3, plus external execution is disabled.

**NOTES:**

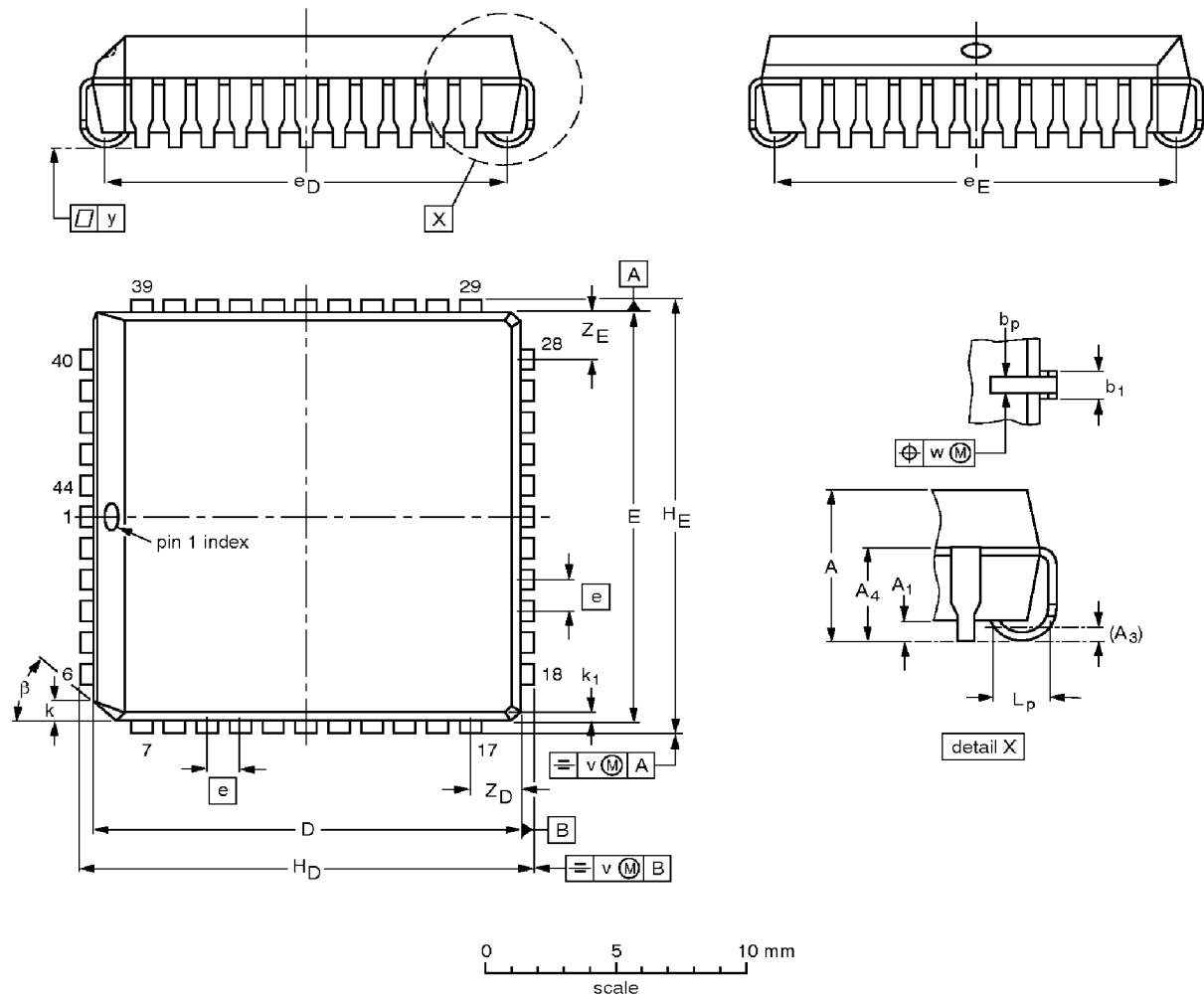
- Any other combination of the Lock bits is not defined.

80C51 8-bit microcontroller family  
8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	k <sub>1</sub> max.	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup> max.	Z <sub>E</sub> <sup>(1)</sup> max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

**Note**  
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

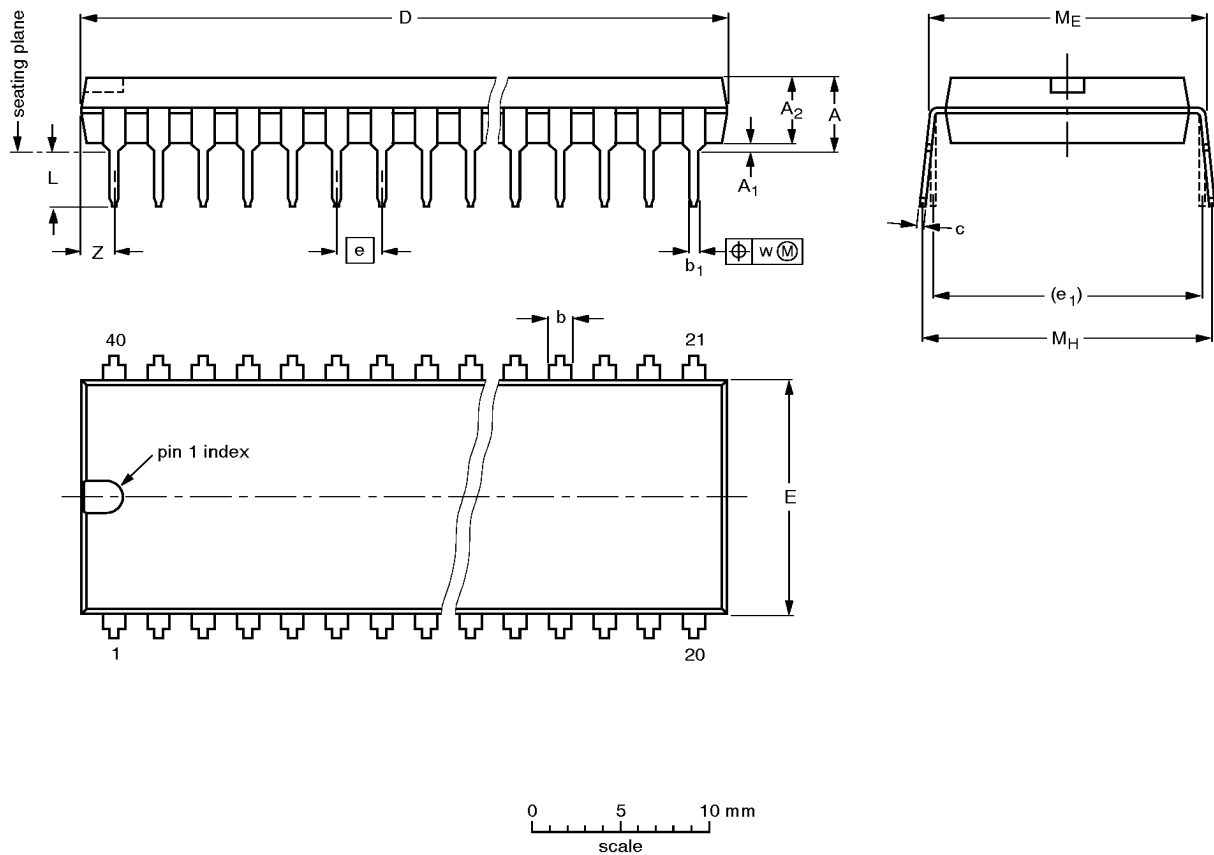
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				95-02-25 97-12-16

80C51 8-bit microcontroller family  
8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

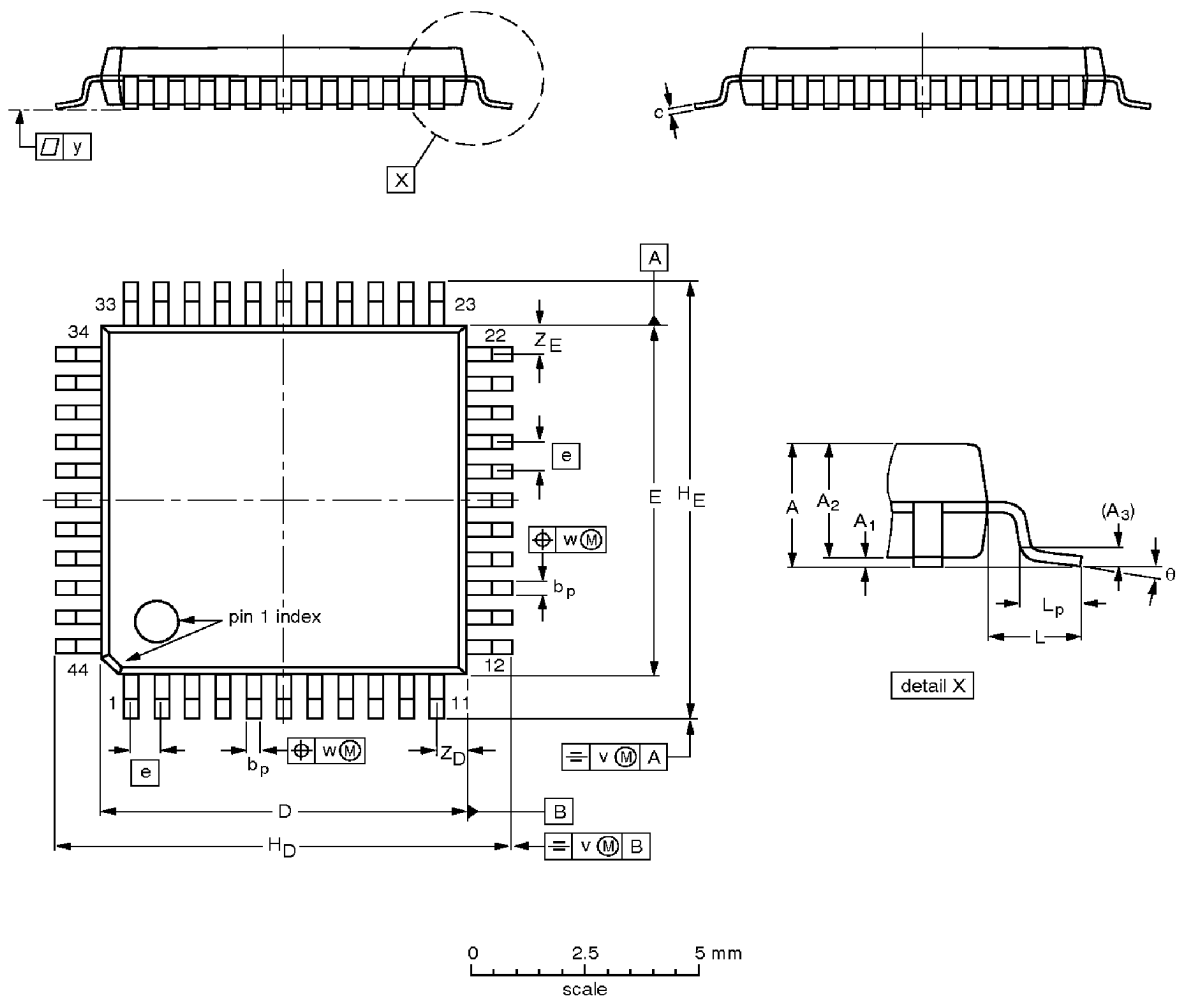
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				92-11-17 95-01-14

80C51 8-bit microcontroller family  
8K/16K/32K Flash with 256 RAM

89C52/89C54/89C58

**QFP44:** plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

**Note**  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						<del>95-02-04</del> 97-08-01