Total Power Solution for Portable Applications

General Description

The AAT2603 is a highly integrated power management solution for handheld mobile systems. It provides six regulated voltages from a single-cell Lithium-ion/polymer battery or a 5V supply.

The six outputs are produced by six regulators; two switching step-down regulators and four low-dropout (LDO) regulators. Each voltage regulator has its own independent enable pin.

The high efficiency step-down regulators are fully integrated and switch at a high 1.5 MHz fixed frequency. They automatically transition to variable frequency operation at light loads for improved efficiency. DC-DC1 (Buck1) is designed for high output current and low dropout voltage (200mV at 1.2A). DC-DC2 (Buck2) is a 600mA regulator with a two step dynamic output voltage capability. One option allows the output voltage of DC-DC2 (Buck2) to be set to either 1.0V or 1.3V with the SELB2 logic pin.

LDO regulators LDO1 and LDO2 can supply up to 400mA of load current with output voltages adjustable down to 1.5V. LDO regulators LDO3 and LDO4 can supply up to 200mA of current and provide good noise and power supply rejection. LDO3 and LDO4 have output voltages externally adjustable down to 1.2V.

The AAT2603 is available in a Pb-free, thermally enhanced 28-pin TQFN44 package and is rated for operation over the -40°C to +85°C temperature range.

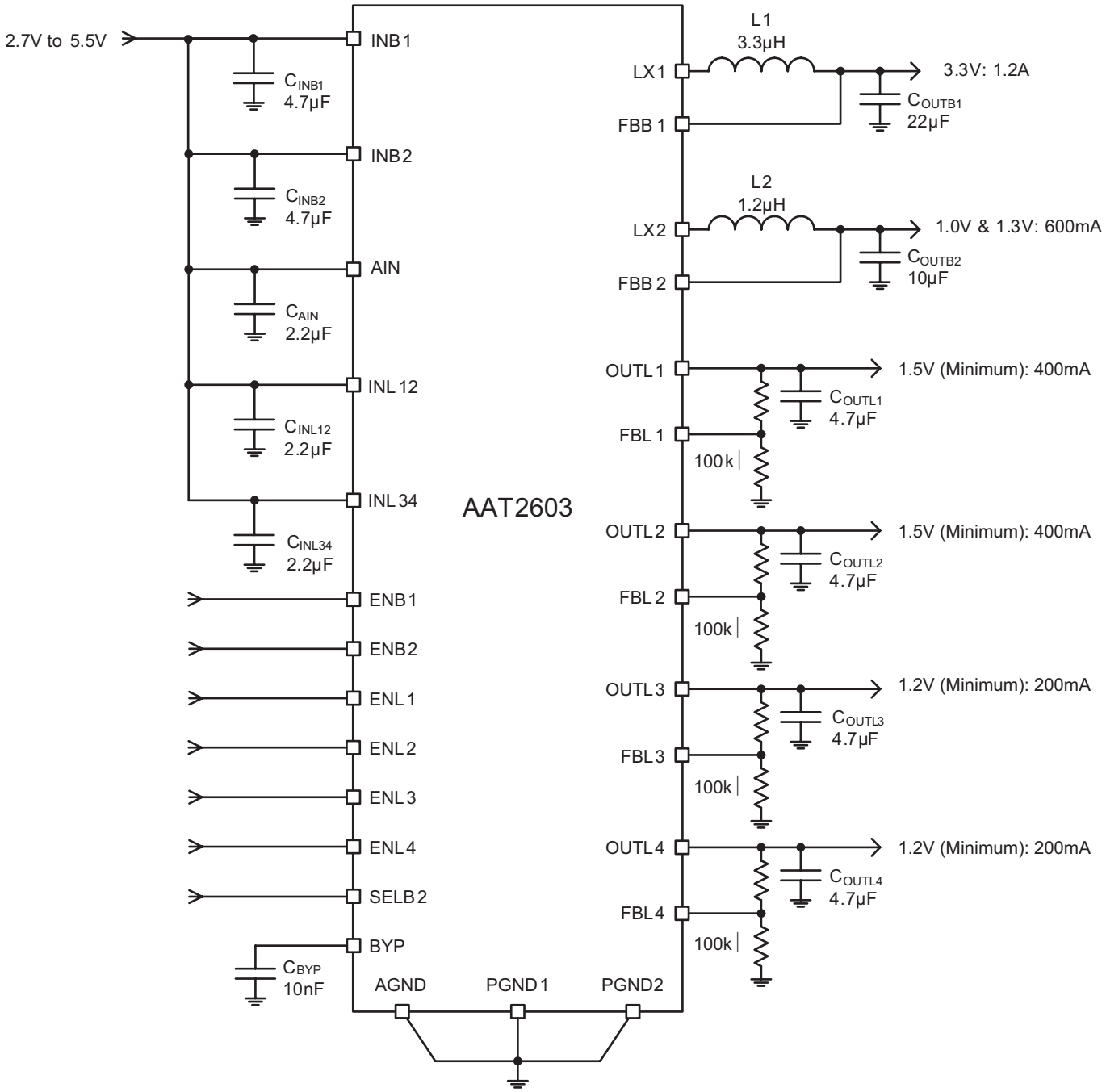
Features

- V_{IN} Range: 2.7V to 5.5V
- Two Step-Down Regulators
  - DC-DC1(Buck1): 1.2A, Low Dropout Voltage
    - Externally Adjustable: V_{FBB1} = 0.6V
      - V_{OUT} Range: 0.6V to V_{INB1}
    - Fixed: V_{OUT} = 3.3V
      - Factory Programmable to any Voltage Level from 0.6V to 4.0V
  - DC-DC2(Buck2): 0.6A, Low Dropout Voltage
    - Externally Adjustable: V_{FBB2} = 0.6V
      - V_{OUT} Range: 0.6V to V_{INB2}
    - Fixed: V_{OUT} = 1.0V[SELB2='1']/1.3V[SELB2='0']
      - Factory Programmable to any Two Voltage Levels from 0.6V to 4.0V
  - Fixed 1.5MHz Switching Frequency
  - Internally Compensated Current Mode Control
  - High Efficiency over the Entire Load Range
  - Four LDO Regulators
    - LDO1: 400mA LDO
    - LDO2: 400mA LDO
    - LDO3: 200mA, Low Noise LDO
    - LDO4: 200mA, Low Noise LDO
    - Fast Turn-On and Turn-Off time
- Short Circuit and Over-Current Protection
- Over-Temperature Protection
- Temperature Range: -40°C to +85°C
- TQFN44-28 Package

Applications

- Handheld GPS
- Handheld Instruments
- PDAs and Handheld Computers
- Portable Media Players
- Smart Phones

Typical Application Circuit



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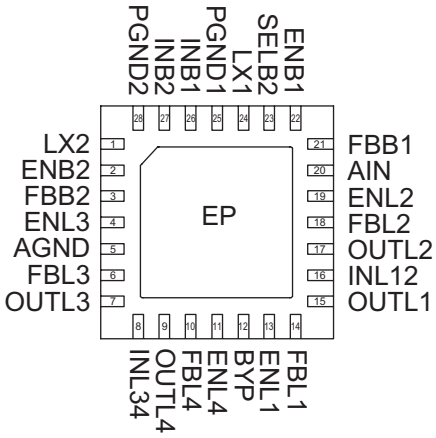
Pin Descriptions

Pin #	Symbol	Function
1	LX2	DC-DC2 (Buck2) switching node. Connect the output inductor to LX2. Connected internally to the drains o f both high-side and low-side switches.
2	ENB2	DC-DC2 (Buck2) enable input. Active high.
3	FBB2	DC-DC2 (Buck2) feedback input. For externally adjustable versions, connect a resistor divider from Buck2 output to FBB2 to AGND to set the Buck2 output voltage.
4	ENL3	LDO3 enable input. Active high.
5	AGND	Analog ground. Connect AGND to PGND1 and PGND2 as close as possible to the device.
6	FBL3	LDO3 feedback input. Connect a resistor divider from OUTL3 to FBL3 to AGND to set the LDO3 output voltage.
7	OUTL3	LDO3 output. Should be closely decoupled to AGND with a 4.7µF or greater capacitor.
8	INL34	LDO3 and LDO4 input. Should be closely decoupled to AGND with a 2.2µF or greater capacitor.
9	OUTL4	LDO4 output. Should be closely decoupled to AGND with a 4.7µF or greater capacitor.
10	FBL4	LDO4 feedback input. Connect a resistor divider from OUTL4 to FBL4 to AGND to set the LDO4 output voltage.
11	ENL4	LDO4 enable input. Active high.
12	BYP	Reference Bypass. Bypass BYP to AGND with a 0.01µF or greater capacitor to reduce the LDO1 output noise.
13	ENL1	LDO1 enable input. Active high.
14	FBL1	LDO1 feedback input. Connect a resistor divider from OUTL1 to FBL1 to AGND to set the LDO1 output voltage.
15	OUTL1	LDO1 output. Should be closely decoupled to AGND with a 4.7µF or greater capacitor.
16	INL12	LDO1 and LDO2 input. Should be closely decoupled to AGND with a 2.2µF or greater capacitor.
17	OUTL2	LDO2 output. Should be closely decoupled to AGND with a 4.7µF or greater capacitor.
18	FBL2	LDO2 feedback input. Connect a resistor divider from OUTL2 to FBL2 to AGND to set the LDO2 output voltage.
19	ENL2	LDO2 enable input. Active high.
20	AIN	Analog voltage input. AIN is the bias supply for the device. Should be closely decoupled to AGND with a 2.2µF or greater capacitor.
21	FBB1	DC-DC1 (Buck1) feedback input. For externally adjustable versions, connect a resistor divider from Buck1 output to FBB1 to AGND to set the Buck1 output voltage.
22	ENB1	DC-DC1 (Buck1) enable input. Active high.
23	SELB2	Dynamically adjusts the output voltage of DC-DC2 (Buck2) (Logic High=1.3V, Logic Low=1.0V)
24	LX1	DC-DC1 (Buck1) switching node. Connect the output inductor to LX1. Connected internally to the drains of both high-side and low-side switches.
25	PGND1	DC-DC1 (Buck1) power ground. Connected internally to the source of the Buck1 N-channel synchronous rectifier. Connect PGND1 to PGND2 and AGND as close as possible to the device.
26	INB1	DC-DC1 (Buck1) power input. Connected internally to the source of the Buck1 P-channel switch. Should be closely decoupled to PGND1 with a 4.7µF or greater capacitor.
27	INB2	DC-DC2 (Buck2) power input. Connected internally to the source of the Buck2 P-channel switch. Should be closely decoupled to PGND2 with a 4.7µF or greater capacitor.
28	PGND2	DC-DC2 (Buck2) power ground. Connected internally to the source of the Buck2 N-channel synchronous rectifier. Connect PGND2 to PGND1 and AGND as close as possible to the device.
EP		Exposed paddle (bottom). Connect to ground as close as possible to the device.

Pin Configuration

TQFN44-28
(Top View)



Part Number Descriptions

Part Number	Output Voltage[1]			
	DC-DC1 (Buck1)	DC-DC2 (Buck2) (SELB2 = Low)	DC-DC2 (Buck2) (SELB2 = High)	LDOs 1-4
AAT2603INJ-1-T1	Ext. Adj. (V_{FBB1} = 600mV)	Ext. Adj. (V_{FBB2} = 600mV)	Ext. Adj. (V_{FBB2} = 775mV)	Ext. Adj. (V_{FBLX} = 1.2V)
AAT2603INJ-2-T1	3.3V	1.3V	1.0V	Ext. Adj. (V_{FBLX} = 1.2V)
AAT2603INJ-3-T1	Ext. Adj. (V_{FBB1} = 600mV)	1.0V	1.3V	Ext. Adj. (V_{FBLX} = 1.2V)

Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
	INBX, INLXX, AIN to AGND	-0.3 to 6.0	V
	ENBX, ENLX, FBBX, FBLX, BYP to AGND	-0.3 to V_{AIN}+0.3	V
	LX1 to PGND1	-0.3 to V_{INB1}+0.3	V
	LX2 to PGND2	-0.3 to V_{INB2}+0.3	V
	PGNDX to AGND, PGND1 to PGND2	-0.3 to 0.3	V
	Operating Temperature Range	-40 to 150	°C
	Storage Temperature Range	-65 to 150	°C
	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Recommended Operating Conditions

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	50	°C/W
P_D	Maximum Power Dissipation	2	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Electrical Characteristics[1]

V_{AIN} = V_{INB1} = V_{INB2} = V_{INL12} = V_{INL34} = 3.6V, C_{BYP} = 10nF, T_A = -40°C to 85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{IN}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	V_{ENB1} = V_{ENL3} = 3.6V, No Load , V_{FBB1} = V_{FBL3} = 3.6V		100	200	µA
I_{SHDN}	Input Shutdown Current	V_{ENx} = AGND			1.0	µA
UVLO	Under-Voltage Lockout	V_{IN} rising			2.6	V
		V_{IN} falling	1.8			V
		Hysteresis		250		mV
F_{OSC}	Oscillator Frequency			1.5		MHz
$t_{S,BYP}$	Bypass Filter Startup Time	V_{ENB1} = 3.6V		200		µs
DC-DC1 (Buck1): 1.2A Step-Down Converter						
V_{OUT_RANGE}	Output Voltage Range		0.6		V_{INB1}	V
V_{OUT_ACC}	Output Voltage Accuracy	T_A = 25°C, 20mA Load	-1.5		+1.5	%
		T_A = -40°C to 85°C, 20mA Load	-2.5		+2.5	%
V_{OUT_TOL}	Output Voltage Tolerance	0A to 1.2A Load; V_{IN} = 2.7V to 5.5V	-3.0		+3.0	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	0A to 1.2A Load		0.4		%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.2		%/V
I_{SHDN}	Shutdown Current	V_{ENB1} = GND			1.0	µA
I_{LX_LEAK}	LX Leakage Current	V_{INB1} = 5.5V, V_{LX1} = 0V to V_{INB1}, EN_{B1} = Low			1.0	µA
I_{LIM}	P-Channel Current Limit			1.7		A
$R_{DS(ON)H}$	High Side Switch On-Resistance			145		mΩ
$R_{DS(ON)L}$	Low Side Switch On-Resistance			200		mΩ
t_S	Start-Up Time	Enable to Output Regulation		200		µs
DC-DC2 (Buck2): 600mA Step-Down Converter						
V_{OUT_RANGE}	Output Voltage Range		0.6		V_{INB2}	V
V_{OUT_ACC}	Output Voltage Accuracy	T_A = 25°C, 20mA Load	-1.5		+1.5	%
		T_A = - 40°C to 85°C, 20mA Load	-2.5		+2.5	%
V_{OUT_TOL}	Output Voltage Tolerance	0mA to 600mA Load; V_{IN} = 2.7V to 5.5V	-3.0		+3.0	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	0mA to 600mA Load		0.2		%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.2		%/V
I_{SHDN}	Shutdown Current	V_{ENB2} = GND			1.0	µA
I_{LX_LEAK}	LX Leakage Current	V_{INB2} = 5.5V, V_{LX2} = 0 to V_{INB2}, EN_{B2} = Low			1.0	µA
I_{LIM}	P-Channel Current Limit			1.3		A
$R_{DS(ON)H}$	High Side Switch On-Resistance			230		mΩ
$R_{DS(ON)L}$	Low Side Switch On-Resistance			180		mΩ
t_S	Start-Up Time	Enable to Output Regulation		200		µs

1. The AAT2603 is guaranteed to meet performance specification from -40°C to +85°C and is assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics[1]

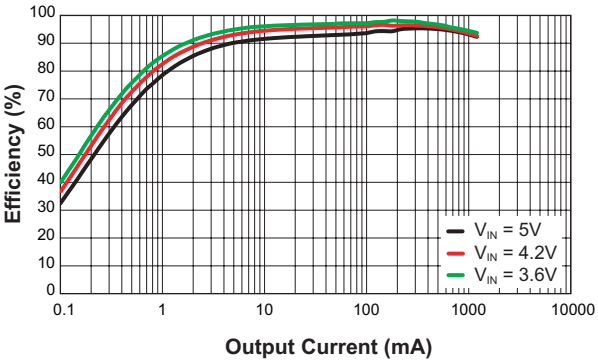
V_{AIN} = V_{INB1} = V_{INB2} = V_{INL12} = V_{INL34} = 3.6V, C_{BYP} = 10nF, T_A = -40°C to 85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
400mA LDO Regulators (LDO1, LDO2)						
V_{OUT_RANGE}	Output Voltage Range		1.5		V_{INL12}	V
V_{FB_ACC}	Feedback Voltage Accuracy	T_A = 25°C, 1mA Load	1.182	1.2	1.218	V
		T_A = -40°C to 85°C, 1mA Load	1.17	1.2	1.23	V
V_{FB_TOL}	Feedback Voltage Tolerance	0mA to 400mA Load, V_{IN} = 2.7V to 5.5V	1.164	1.2	1.236	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	1mA to 400mA Load		0.3		%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.3V to 5.5V, 100mA Load		0.08		%/V
$I_{OUT(MAX)}$	Maximum Output Current		400			mA
I_{LIM}	Output Current Limit			1500		mA
V_{DO}	Dropout Voltage	400mA Load		300	500	mV
PSRR	Power Supply Rejection Ratio	f < 10KHz, $C_{OUTL1,2}$ = 4.7µF, 10mA Load		50		dB
t_S	Start-Up Time	V_{BYP} already enabled; C_{OUT} = 4.7µF		200		µs
200mA LDO Regulators (LDO3, LDO4)						
V_{OUT_RANGE}	Output Voltage Range		1.2		V_{INL34}	V
V_{FB_ACC}	Feedback Voltage Accuracy	T_A = 25°C, 1mA Load	1.182	1.2	1.218	V
		T_A = -40°C to +85°C, 1mA Load	1.17	1.2	1.23	V
V_{FB_TOL}	Feedback Voltage Tolerance	0mA to 200mA Load, V_{IN} = 2.7V to 5.5V	1.164	1.2	1.236	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	0mA to 200mA Load		0.2		%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.3V to 5.5V, 100mA Load		0.02		%/V
$I_{OUT(MAX)}$	Maximum Output Current		200			mA
I_{LIM}	Output Current Limit			750		mA
V_{DO}	Dropout Voltage	200mA Load		200	350	mV
PSRR	Power Supply Rejection Ratio	f < 10KHz, $C_{OUTL3,4}$ = 4.7µF, 10mA Load		50		dB
e_N	RMS Output Noise	Power BW: 100~100KHz		45		µVrms
t_S	Start-Up Time	V_{BYP} already enabled; C_{OUT} = 4.7µF		200		µs
Logic Inputs/Outputs						
$V_{EN(H)}$	Input Logic High Voltage		1.4			V
$V_{EN(L)}$	Input Logic Low Voltage				0.4	V
I_{EN}	Logic Input Current	V_{EN} = 1.4V[2]			1.5	µA
Thermal						
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
$T_{SD(HYS)}$	Over-Temperature Shutdown Hysteresis			15		°C

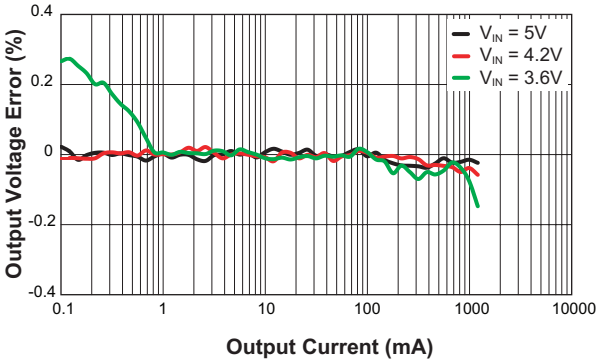
1. The AAT2603 is guaranteed to meet performance specification from -40°C to +85°C and is assured by design, characterization and correlation with statistical process controls.
2. The enable pins have internal 1.6MΩ pull-down resistors.

Typical Characteristics—DC-DC1 (Buck1)

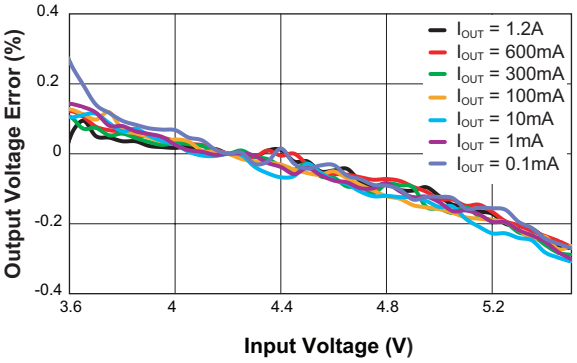
Efficiency vs. Output Current
(V_{OUTB1} = 3.3V; L = 3.3µH)



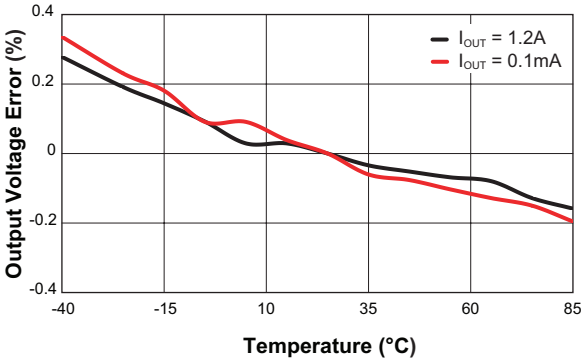
Load Regulation
(V_{OUTB1} = 3.3V; L = 3.3µH)



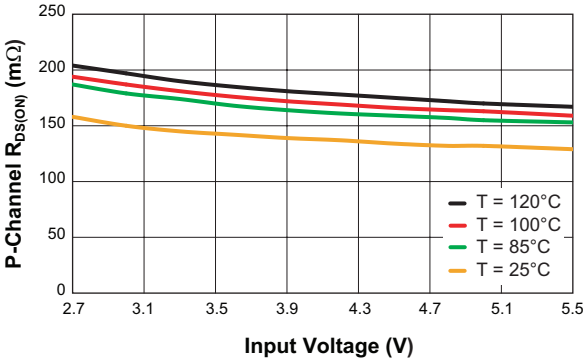
Line Regulation
(V_{OUTB1} = 3.3V; L = 3.3µH)



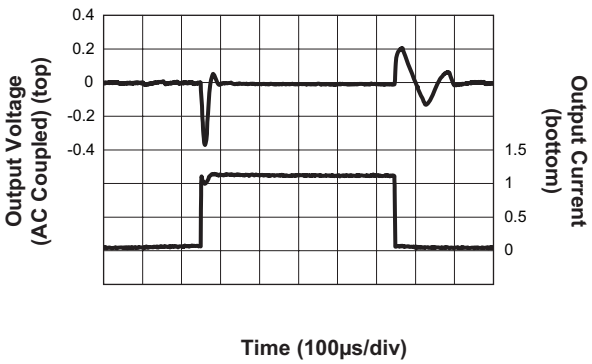
Output Voltage Error vs. Temperature
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V)



P-Channel $R_{DS(ON)}$ vs. Input Voltage
(V_{OUTB1} = 3.3V)

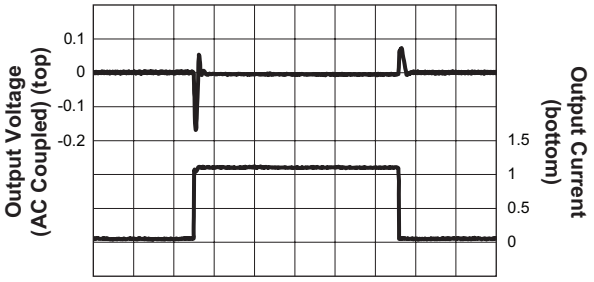


Load Transient
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V; I_{OUTB1} = 100mA to 1200mA; C_{FF} = 0pF)



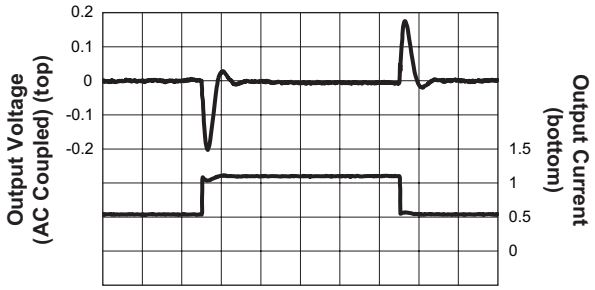
Typical Characteristics—DC-DC1 (Buck1)

Load Transient
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V; I_{OUTB1} = 100mA to 1200mA; C_{FF} = 100pF)



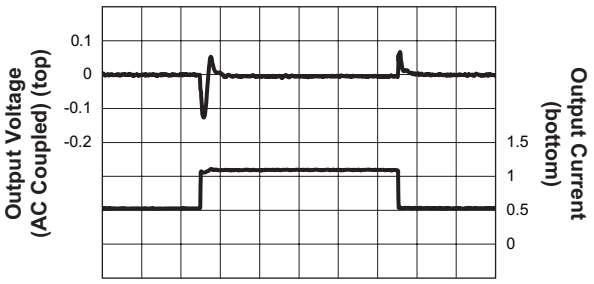
Time (100µs/div)

Load Transient
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V; I_{OUTB1} = 600mA to 1200mA; C_{FF} = 0pF)



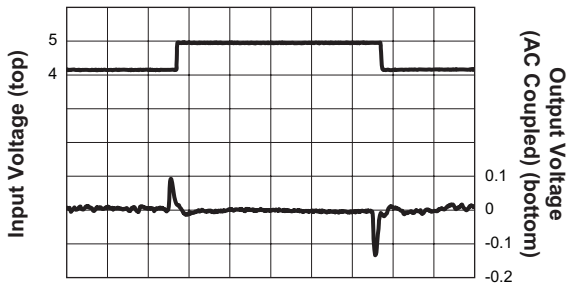
Time (50µs/div)

Load Transient
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V; I_{OUTB1} = 600mA to 1200mA; C_{FF} = 100pF)



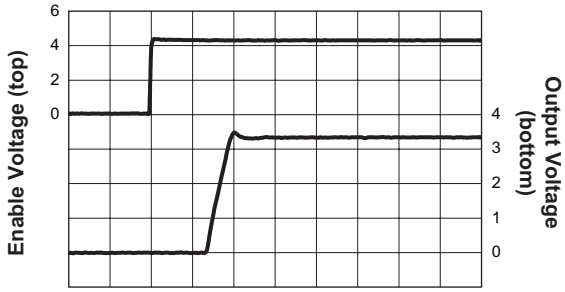
Time (50µs/div)

Line Transient
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V to 5V; I_{OUTB1} = 700mA)



Time (100µs/div)

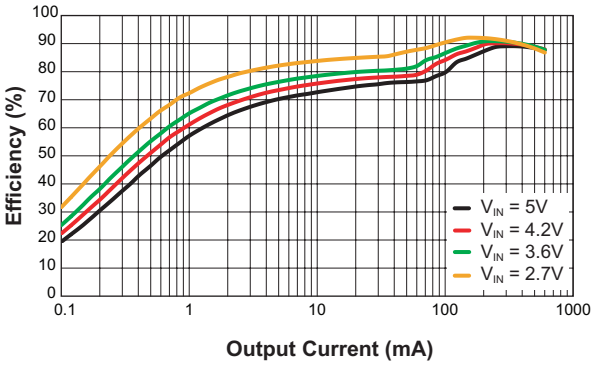
Soft-Start
(V_{OUTB1} = 3.3V; V_{IN} = 4.2V; I_{OUTB1} = 1.2A)



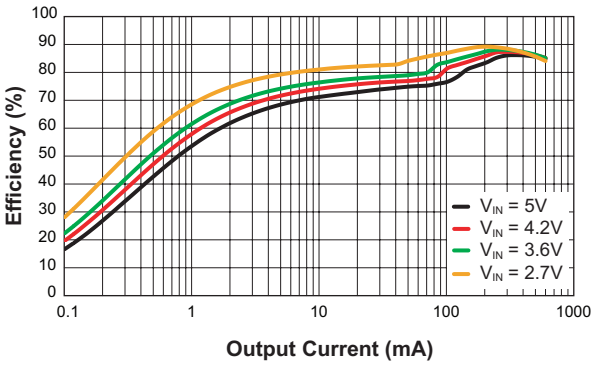
Time (100µs/div)

Typical Characteristics—DC-DC2 (Buck2)

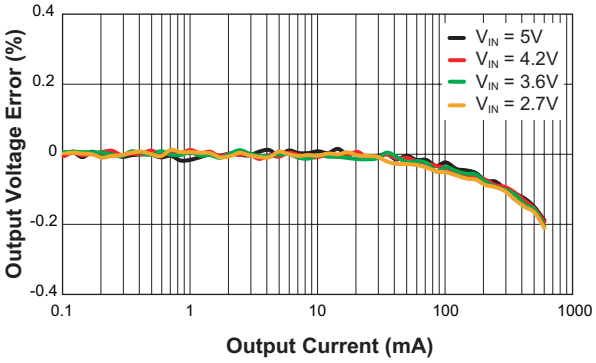
Efficiency vs. Output Current
(V_{OUTB2} = 1.3V; L = 1.5µH)



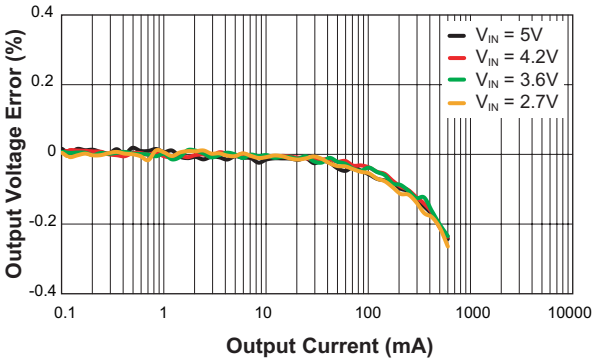
Efficiency vs. Output Current
(V_{OUTB2} = 1V; L = 1.2µH)



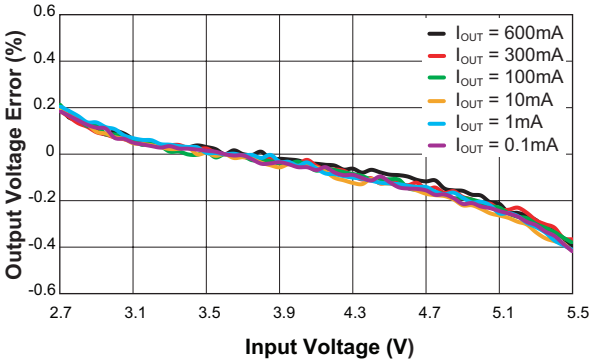
Load Regulation
(V_{OUTB2} = 1.3V; L = 1.5µH)



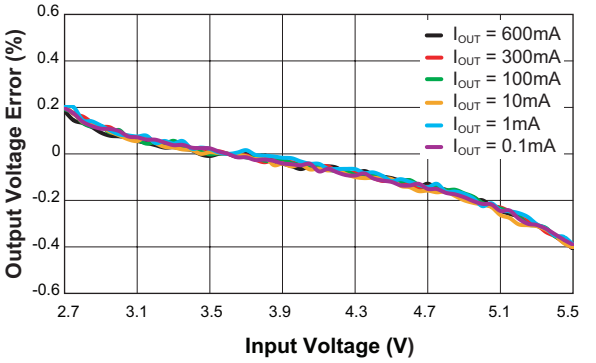
Load Regulation
(V_{OUTB2} = 1V; L = 1.2µH)



Line Regulation
(V_{OUTB2} = 1.3V; L = 1.5µH)

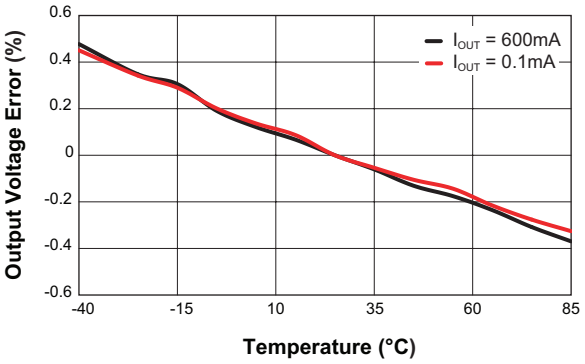


Line Regulation
(V_{OUTB2} = 1V; L = 1.2µH)

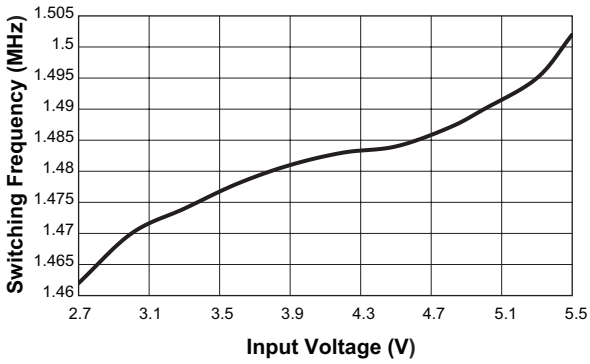


Typical Characteristics—DC-DC2 (Buck2)

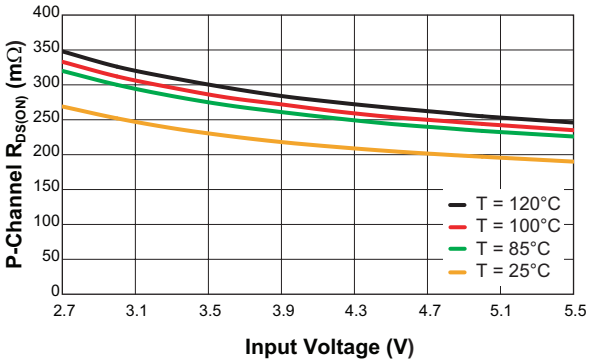
Output Voltage Error vs. Temperature
(V_{OUTB2} = 1.3V; V_{IN} = 3.6V)



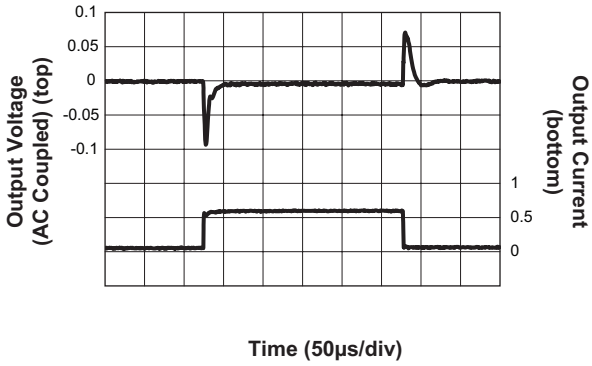
Switching Frequency vs. Input Voltage
(V_{OUTB2} = 1.3V; I_{OUTB2} = 600mA)



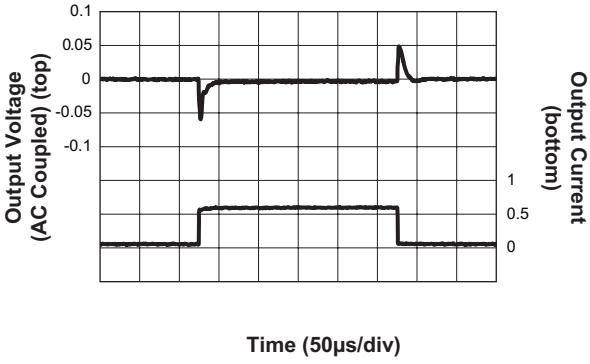
P-Channel $R_{DS(ON)}$ vs. Input Voltage
(V_{OUTB2} = 1.3V)



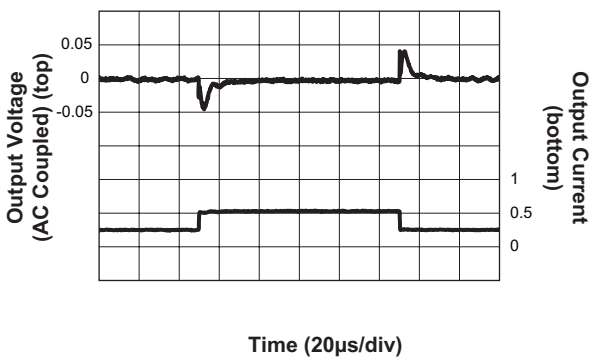
Load Transient
(V_{OUTB2} = 1.3V; V_{IN} = 3.6V; I_{OUTB2} = 100mA to 600mA; C_{FF} = 0pF)



Load Transient
(V_{OUTB2} = 1.3V; V_{IN} = 3.6V; I_{OUTB2} = 100mA to 600mA; C_{FF} = 100pF)

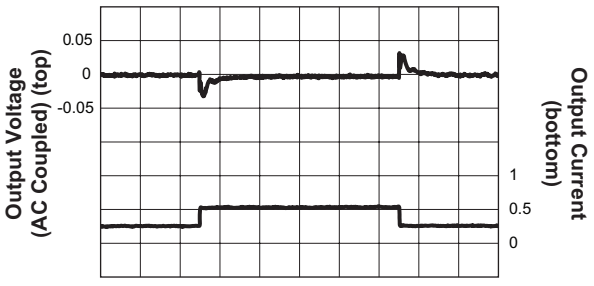


Load Transient
(V_{OUTB2} = 1.3V; V_{IN} = 3.6V; I_{OUTB2} = 300mA to 600mA; C_{FF} = 0pF)



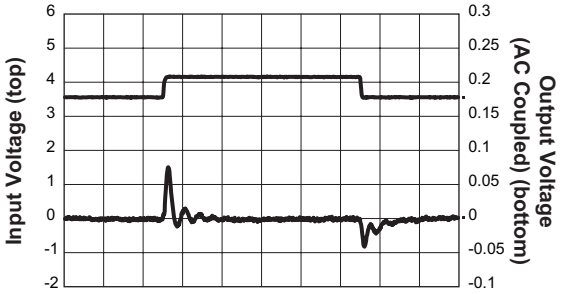
Typical Characteristics—DC-DC2 (Buck2)

Load Transient
(V_{OUTB2} = 1.3V; V_{IN} = 3.6V; I_{OUTB2} = 300mA to 600mA; C_{FF} = 100pF)



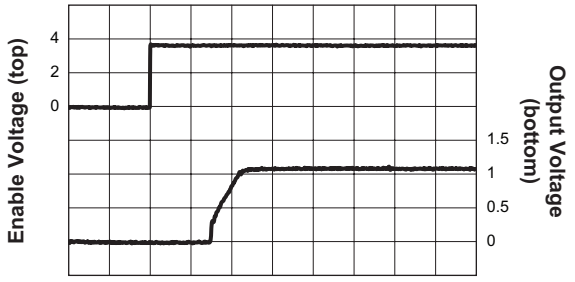
Time (20µs/div)

Line Transient
(V_{OUTB2} = 1.3V; V_{IN} = 3.6 to 4.2V; I_{OUTB2} = 300mA)



Time (50µs/div)

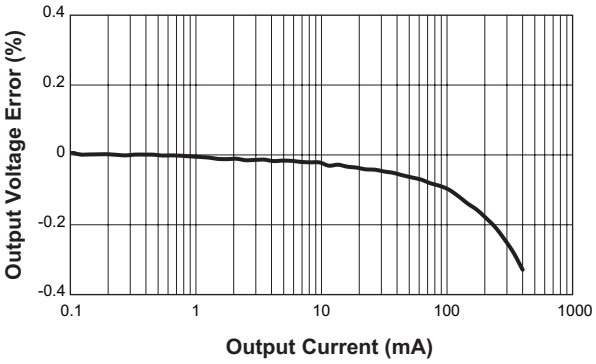
Soft-Start
(V_{OUTB2} = 1.3V; V_{IN} = 3.6V; I_{OUTB2} = 600mA)



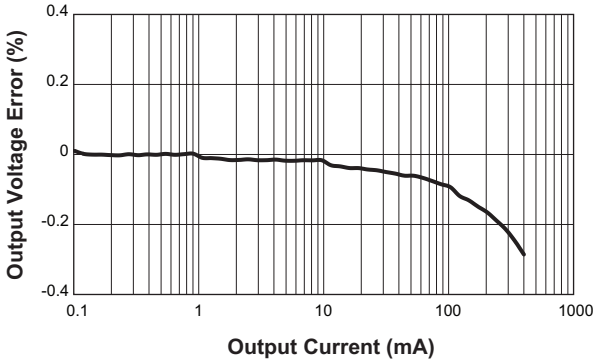
Time (100µs/div)

Typical Characteristics—LDO1/LDO2

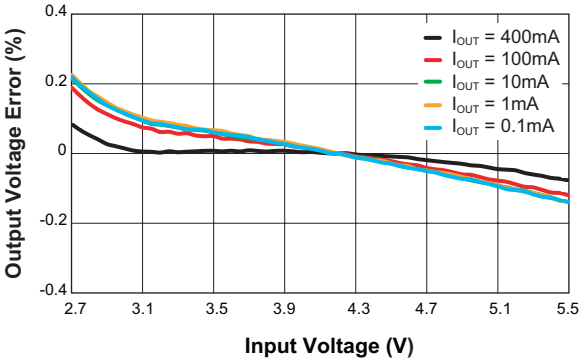
Load Regulation
($V_{OUTL1\&2}$ = 3V; V_{IN} = 3.6V)



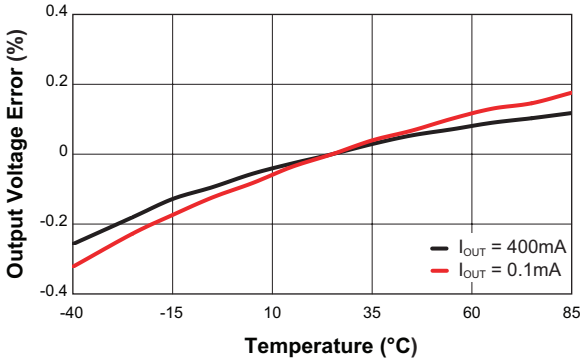
Load Regulation
($V_{OUTL1\&2}$ = 1.5V; V_{IN} = 3.6V)



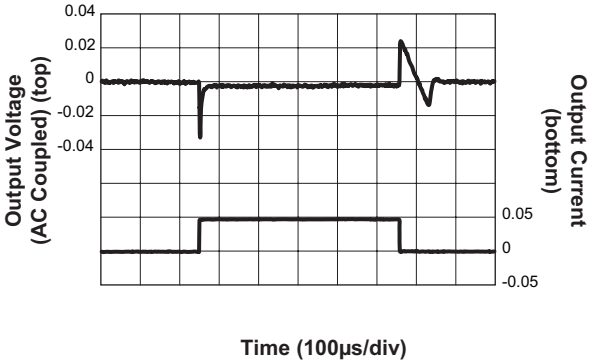
Line Regulation
($V_{OUTL1\&2}$ = 1.5)



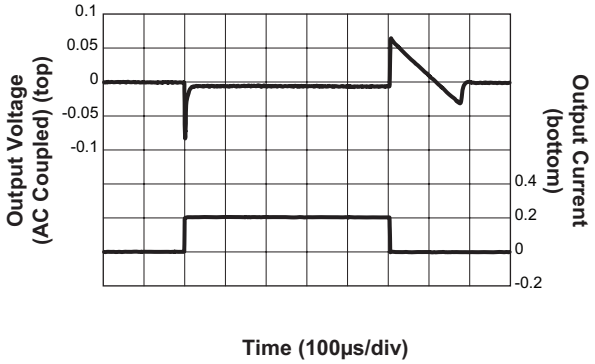
Output Voltage Error vs. Temperature
($V_{OUTL1\&2}$ = 2.8V; V_{IN} = 3.6V)



Load Transient
($V_{OUTL1\&2}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL1\&2}$ = 1mA to 50mA)

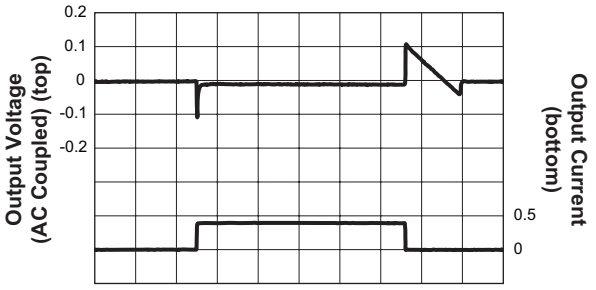


Load Transient
($V_{OUTL1\&2}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL1\&2}$ = 1mA to 200mA)



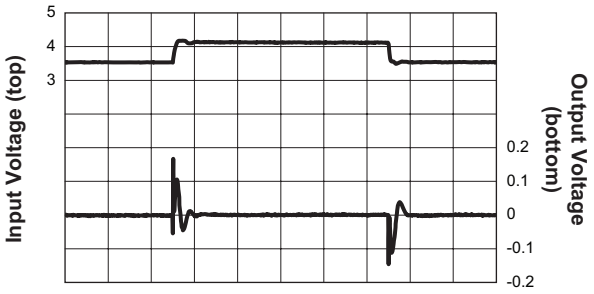
Typical Characteristics—LDO1/LDO2

Load Transient
($V_{OUTL1\&2}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL1\&2}$ = 1mA to 400mA)



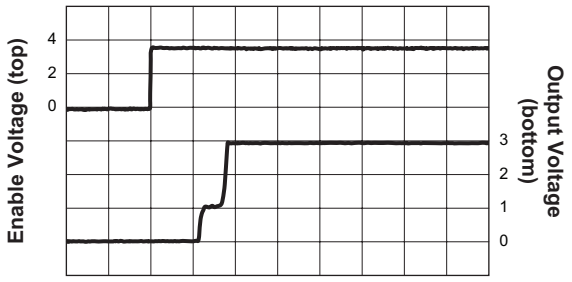
Time (200µs/div)

Line Transient
($V_{OUTL1\&2}$ = 2.8V; V_{IN} = 3.6 to 4.2V; $I_{OUTL1\&2}$ = 400mA)



Time (20µs/div)

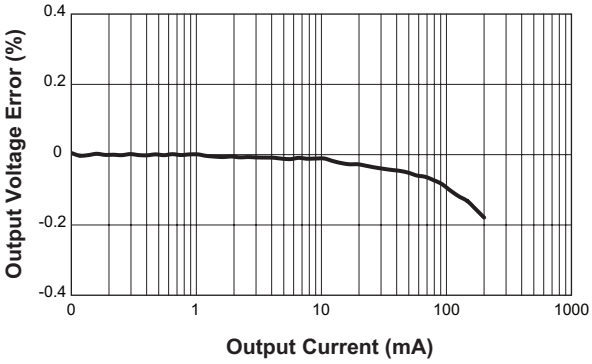
Soft-Start
($V_{OUTL1\&2}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL1\&2}$ = 400mA)



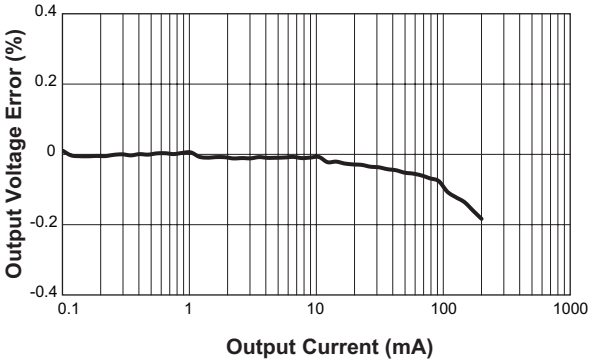
Time (500µs/div)

Typical Characteristics—LDO3/LDO4

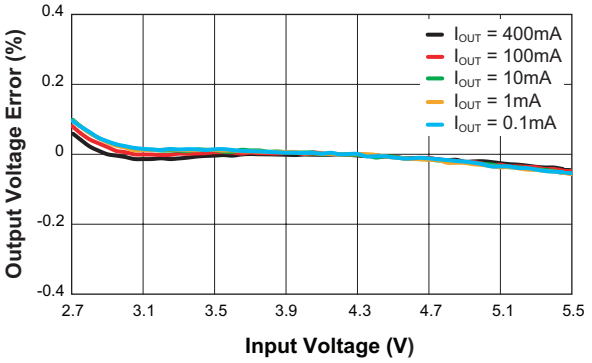
Load Regulation
($V_{OUTL3\&4}$ = 3V; V_{IN} = 3.6V)



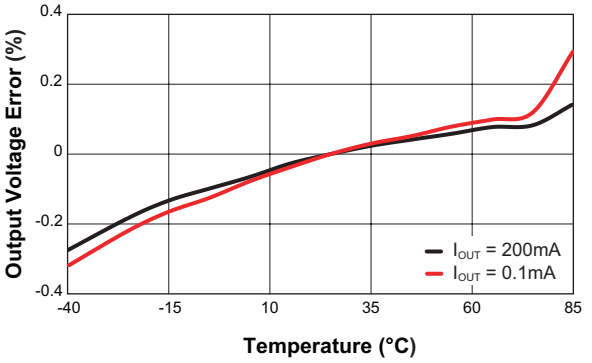
Load Regulation
($V_{OUTL3\&4}$ = 1.2V; V_{IN} = 3.6V)



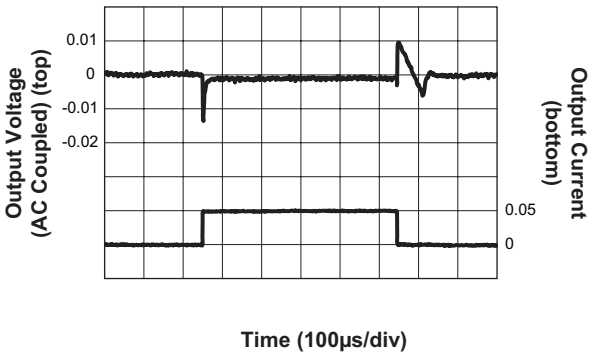
Line Regulation
($V_{OUTL3\&4}$ = 1.2V)



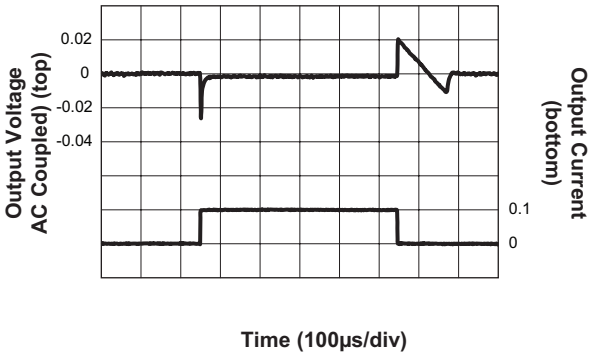
Output Voltage Error vs. Temperature
($V_{OUTL3\&4}$ = 2.8V; V_{IN} = 3.6V)



Load Transient
($V_{OUTL3\&4}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL3\&4}$ = 1mA to 50mA)

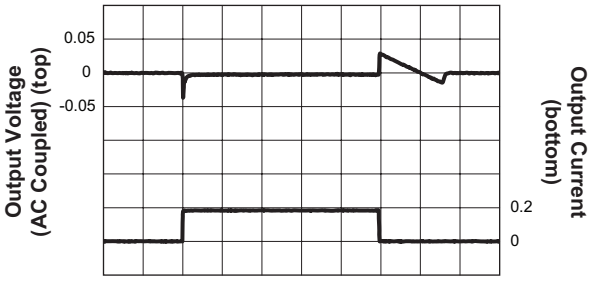


Load Transient
($V_{OUTL3\&4}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL3\&4}$ = 1mA to 100mA)

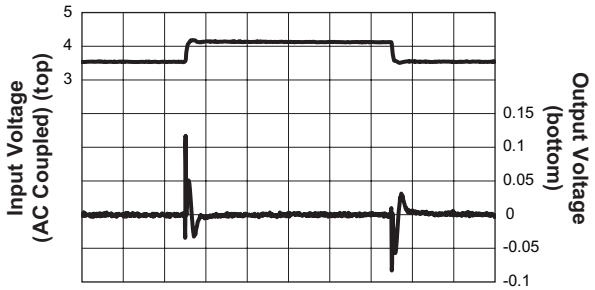


Typical Characteristics—LDO3/LDO4

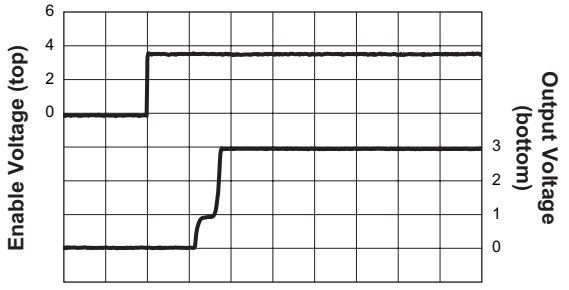
Load Transient
($V_{OUTL3\&4}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL3\&4}$ = 1mA to 200mA)



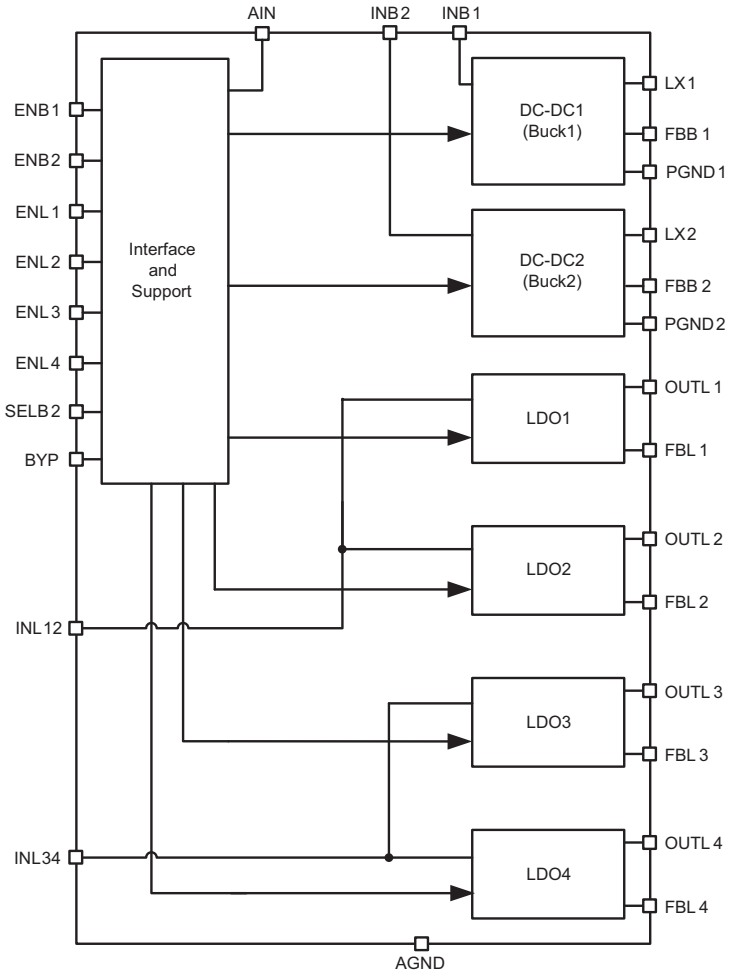
Line Transient
($V_{OUTL3\&4}$ = 2.8V; V_{IN} = 3.6 to 4.2V; $I_{OUTL3\&4}$ = 200mA)



Soft-Start
($V_{OUTL3\&4}$ = 2.8V; V_{IN} = 3.6V; $I_{OUTL3\&4}$ = 200mA)



Functional Block Diagram



Functional Description

The AAT2603 is a highly integrated voltage regulating power management unit for mobile handsets or other portable devices. It includes two switch-mode step-down converters (600mA [DC-DC2] and 1.2A [DC-DC1]), and four low-dropout (LDO) regulators (two: 200mA, two: 400mA). It operates from an input voltage between 2.7V and 5.5V making it ideal for lithium-ion or 5V regulated power sources. All six converters have separate enable pins for ease of use.

Step-Down Converters

The AAT2603 switch-mode, step-down converters are constant frequency peak current mode PWM converters with internal compensation. The input voltage range is 2.7V to 5.5V. The output voltage range is 0.6V to V_{IN}. The high 1.5MHz switching frequency allows the use of small external inductor and capacitor.

The step-down converters offer soft-start to limit the current surge seen at the input and eliminate output voltage overshoot. The current across the internal P-channel power switch is sensed and turns off when the current exceeds the current limit. Also, thermal protection completely disables switching if internal dissipation becomes excessive, thus protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

DC-DC1 (Buck1) is designed for a peak continuous output current of 1.2A. The high-side power switch has been designed with a low R_{DSON} of 145mΩ to allow for a minimum dropout voltage of 174mV at full load current.

It was designed to maintain over 90% efficiency at its maximum rated output current load of 1.2A with a 3.3V output. Peak efficiency is above 95%. Buck1 has excellent transient response, load and line regulation. Transient response time is typically less than 20µs. The peak input current is limited to 1.7A.

DC-DC2 (Buck2) is a 600mA step-down regulator designed to dynamically shift between two output voltages by toggling the SELB2 pin. The internal reference voltage of the buck regulator is changed based on the position of the SELB2 pin.

Buck2 is designed to maintain over 85% efficiency at its maximum rated output current of 600mA with a 1.2V output. Peak efficiency is above 90%. Buck2 has excellent transient response, load and line regulation. The peak inductor current is limited to 1.3A.

The two step-down converters on the AAT2603 have highly flexible output voltage programming capability. The output voltages can be factory programmed to preset output voltages or set by external resistors. The "Part Number Descriptions" table lists the available voltage options for step-down converters Buck1 and Buck2. Option 1 has externally adjustable output voltages for both step-down converters. The dynamic voltage scaling for Buck2 is still useable with external feedback resistors. When SELB2 is in the low position the feedback voltage is compared to a 600mV reference, while when SELB2 is high the reference voltage is 775mV. For most other options, the output voltages of Buck2 are factory programmed.

LDO Regulators

The AAT2603 includes four LDO regulators. The regulators operate from the 2.7V to 5.5V input voltage to a regulated output voltage. The LDO regulators have adjustable output voltages set by resistors. Each LDO consumes 50uA of quiescent current.

The two 200mA LDO regulators are stable with a small 4.7µF ceramic output capacitor. The low 200mV dropout voltage at 200mA load allows a regulated output voltage approaching the input voltage. Low output noise voltage and high power supply rejection make these regulators ideal for powering noise sensitive circuitry.

The two 400mA LDO regulators are stable with a small 4.7µF ceramic output capacitor. The low 300mV dropout voltage at 400mA load allows a regulated output voltage approaching the input voltage. These LDOs offer high power supply rejection.

Application Information

DC-DC1/DC-DC2

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. Table 1 displays suggested inductor values for various output voltages.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

It is recommended that the inductor current rating exceed the current limit of the step-down converter. See Table 2 for example inductor values/vendors.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input; see Table 3 for suggested capacitor components. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN} (C_{INB1}/C_{INB2}). The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

Manufacturer	Part Number/ Type	Inductance (µH)	Rated Current (A)	DCR (mΩ) (max)	Size (mm) LxWxH
TDK	LTF5022	1.2	4.3	25	5x5.2x2.2
		1.8	3.6	32	
		2.2	3.2	40	
		3.3	2.5	60	
Wurth Electronik	WE-TPC Type M	1	2.6	30	4.8x4.8x1.8
		1.8	2.35	50	
		2.7	2.03	60	
		3.3	1.8	65	
	WE-TPC Type MH	1.2	2.8	20	4.8x4.8x2.8
		1.8	2.45	25	
		2.2	2.35	28	
		2.7	1.95	30	
		3.3	1.8	35	
Murata	LQH55D	1	4	19 (typ)	5x5.7x4.7
		1.5	3.7	22 (typ)	
		2.2	3.2	29 (typ)	
		3.3	2.9	36 (typ)	

Table 1: Suggested Inductor Components.

Configuration	Output Voltage	Inductor Value
Adjustable and Fixed Output Voltage	1V, 1.2V, 1.3V	1.0µH to 1.2µH
	1.5V, 1.8V	1.5µH to 1.8µH
	2.5V	2.2µH to 2.7µH
	2.8V, 3.3V	3.3µH

Table 2: Inductor Values for Specific Output Voltages.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
AVX	0603ZD105K	1µF	10	X5R	0603
	0603ZD225K	2.2µF	10		
TDK	C1608X5R1E105K	1µF	25	X5R	0603
	C1608X5R1C225K	2.2µF	16		
	C1608X5R1A475K	4.7µF	10		
	C2012X5R1A106K	10µF	10		0805
	C3216X5R1A226K	22µF	10		1206
Murata	GRM188R61C105K	1µF	16	X5R	0603
	GRM188R61A225K	2.2µF	10		
	GRM219R61A106K	10µF	10		0805
	GRM31CR71A226K	22µF	10	X7R	1206
Taiyo Yuden	LMK107BJ475KA	4.7µF	10	X5R	0603

Table 3: Suggested Capacitor Components.

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2603 step-down switching regulators. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple. A 10µF X5R or X7R ceramic capacitor is required for DC-DC2 and a 22µF X5R or X7R ceramic capacitor is required for DC-DC1; see Table 3 for suggested capacitor components.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within several switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the several switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF for DC-DC2 and 22µF for DC-DC1. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Feedback Resistor Selection

Resistors R1 and R2 of Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 42 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

The AAT2603 step-down regulators, combined with an external feedforward capacitor (C_{FF} in Figure 1), deliver enhanced transient response for extreme pulsed load applications.

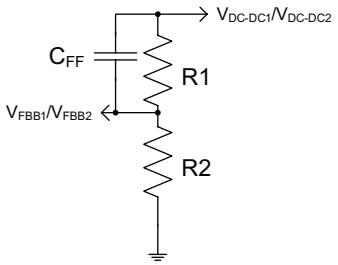


Figure 1: AAT2603 DC-DC1/DC-DC2 External Resistor Output Voltage Programming.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 221kΩ R1 (kΩ)
0.9	29.4	113K
1.0	39.2	150K
1.1	49.9	187K
1.2	59.0	221K
1.3	68.1	261K
1.4	78.7	301K
1.5	88.7	332K
1.8	118	442K
1.85	124	464K
2.0	137	523K
2.5	187	715K
3.3	267	1.00M

Table 4: Feedback Resistors for DC-DC1 and DC-DC2.

LDO1/LDO2/LDO3/LDO4

Input Capacitor

Typically, a 2.2µF or larger capacitor is recommended for $C_{INL12}/C_{INL34}/C_{AIN}$ in most applications. The input capacitor should be located as close to the input (INL12/INL34/AIN) of the device as practically possible. $C_{INL12}/C_{INL34}/C_{AIN}$ values greater than 2.2µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for $C_{INL12}/C_{INL34}/C_{AIN}$. There is no specific capacitor ESR requirement for $C_{INL12}/C_{INL34}/C_{AIN}$. However, for 200mA/400mA LDO regulators output operation, ceramic capacitors are recommended for $C_{INL12}/C_{INL34}/C_{AIN}$ due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins VOUTLX and AGND. The C_{OUTLX} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT2603 LDO regulators have been specifically designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it will also work with higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 4.7µF to 10µF. If desired, C_{OUTLX} may be increased without limit.

Bypass Capacitor and Low Noise Applications

A bypass capacitor pin is provided to enhance the very low noise characteristics of the AAT2603 LDO3 and LDO4 regulators. The bypass capacitor is not necessary for operation of the AAT2603. However, for best device performance, a small ceramic capacitor should be placed between the bypass pin (BYP) and the device analog ground pin (AGND). The value of C_{BYP} should be 10nF. For lowest noise and best possible power supply ripple rejection performance a 10nF capacitor should be used. To practically realize the highest power supply ripple rejection and lowest output noise performance, it is critical that the capacitor connection between the BYP pin and AGND pin be direct and PCB traces should be as short as possible. Refer to the PCB Layout Recommendations section of this datasheet for examples.

There is a relationship between the bypass capacitor value and the LDO regulator turn-on time. In applications where fast device turn-on time is desired, the value of C_{BYP} should be reduced.

In applications where low noise performance and/or ripple rejection are less of a concern, the bypass capacitor may be omitted. The fastest device turn-on time will be realized when no bypass capacitor is used.

DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance. For this reason, the use of a low leakage, high quality ceramic (NPO or C0G type) or film capacitor is highly recommended.

Feedback Resistor Selection

Resistors R1 and R2 of Figure 2 program the output to regulate at a voltage higher than 1.5V for LDO1/LDO2 and 1.2V for LDO3/LDO4. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 100kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Tables 5 and 6 summarize the resistor values for various output voltages with R2 set to 100kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{1.2V} - 1\right) \cdot 100k\Omega = 24.9k\Omega$$

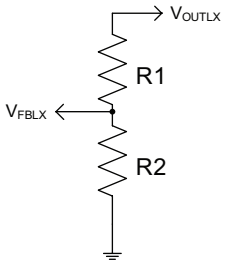


Figure 2: AAT2603 LDO1/LDO2/LDO3/LDO4 External Resistor Output Voltage Programming.

V_{OUT} (V)	R2 = 100kΩ R1 (kΩ)
1.3	8.25
1.4	16.5
1.5	24.9
1.6	33.2
1.7	41.2
1.8	49.9
1.9	59
2	66.5
2.1	75
2.2	82.5
2.3	90.9
2.4	100
2.5	107
2.6	118
2.7	124
2.8	133
2.9	140
3	150
3.1	158
3.2	165
3.3	174

Table 5: Feedback Resistor Values for LDO3 and LDO4.

V_{OUT} (V)	R2 = 100kΩ R1 (kΩ)
1.5	24.9
1.6	33.2
1.7	41.2
1.8	49.9
1.9	59
2	66.5
2.1	75
2.2	82.5
2.3	90.9
2.4	100
2.5	107
2.6	118
2.7	124
2.8	133
2.9	140
3	150
3.1	158
3.2	165
3.3	174

Table 6: Feedback Resistor Values for LDO1 and LDO2.

Thermal Calculations

There are three types of losses associated with the AAT2603 total power management solution [two step-down and four LDO regulators]: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the internal power switches/FETs of both of the step-down regulators and the power loss associated with the voltage difference across the pass switch/FET of the four LDO regulators. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by the following (quiescent and switching losses are ignored, since conduction losses are so dominant):

$$P_{DC\text{-}DC1} = \frac{I_{O1}^2 \cdot (R_{DS(ON)H1} \cdot V_{OB1} + R_{DS(ON)L1} \cdot [V_{INB1} - V_{OB1}])}{V_{INB1}}$$

$$P_{DC\text{-}DC2} = \frac{I_{O2}^2 \cdot (R_{DS(ON)H2} \cdot V_{OB2} + R_{DS(ON)L2} \cdot [V_{INB2} - V_{OB2}])}{V_{INB2}}$$

$$P_{LDO1} = I_{LDO1} \cdot (V_{INL12} - V_{OL1})$$

$$P_{LDO2} = I_{LDO2} \cdot (V_{INL12} - V_{OL2})$$

$$P_{LDO3} = I_{LDO3} \cdot (V_{INL34} - V_{OL3})$$

$$P_{LDO4} = I_{LDO4} \cdot (V_{INL34} - V_{OL4})$$

$$P_{TOTAL} = P_{DC\_DC1} + P_{DC\_DC2} + P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4}$$

$P_{DC\text{-}DCX}$: Power dissipation of the specific DC-DC regulator
I_{OX}: Output current of the specific DC-DC regulator
$R_{DS(ON)HX}$: Resistance of the internal high-side switch/FET
$R_{DS(ON)LX}$: Resistance of the internal low-side switch/FET
V_{OBX}: Output voltage of the specific DC-DC regulator
V_{INBX}: Input voltage of the specific DC-DC regulator
P_{LDOX}: Power dissipation of the specific LDO regulator
I_{LDOX}: Output current of the specific LDO regulator
V_{INLXX}: Input voltage of the specific LDO regulator
V_{OLX}: Output voltage of the specific LDO regulator
P_{TOTAL}: Total power dissipation of the AAT2603

Since $R_{DS(ON)}$ and conduction losses all vary with input voltage, the dominant losses should be investigated over the complete input voltage range. Given the total conduction losses, the maximum junction temperature (125°C) can be derived from the θ_{JA} for the TQFN44-28 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_A$$

$T_{J(MAX)}$: Maximum junction temperature
P_{TOTAL}: Total conduction losses
Θ_{JA}: Thermal impedance of the package
T_A: Ambient temperature

Layout

The suggested PCB layout for the AAT2603 is shown in Figures 4 and 5. The following guidelines should be used to help ensure a proper layout.

1. The input capacitors (C1, C2, C7, C13, and C16) should connect as closely as possible to INB1 (Pin 26), INB2 (Pin 27), AIN (Pin 20), INL12 (Pin 16), INL34 (Pin 8), and AGND/PGND1/PGND2 (Pins 5, 25, and 27).
2. C3/C18 (step-down regulator output capacitors) and L1/L2 should be connected as closely as possible. The connection of L1/L2 to the LX1/LX2 pins should be as short as possible.
3. The feedback trace or FBXX pin (Pins 3, 6, 10, 14, 18, and 21) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FBXX pin (Pins 3, 6, 10, 14, 18, and 21) to minimize the length of the high impedance feedback trace.
4. The resistance of the trace from the load return to the PGND1/PGND2 (Pins 25 and 28) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the TDFN44-28 exposed paddle to the ground plane.

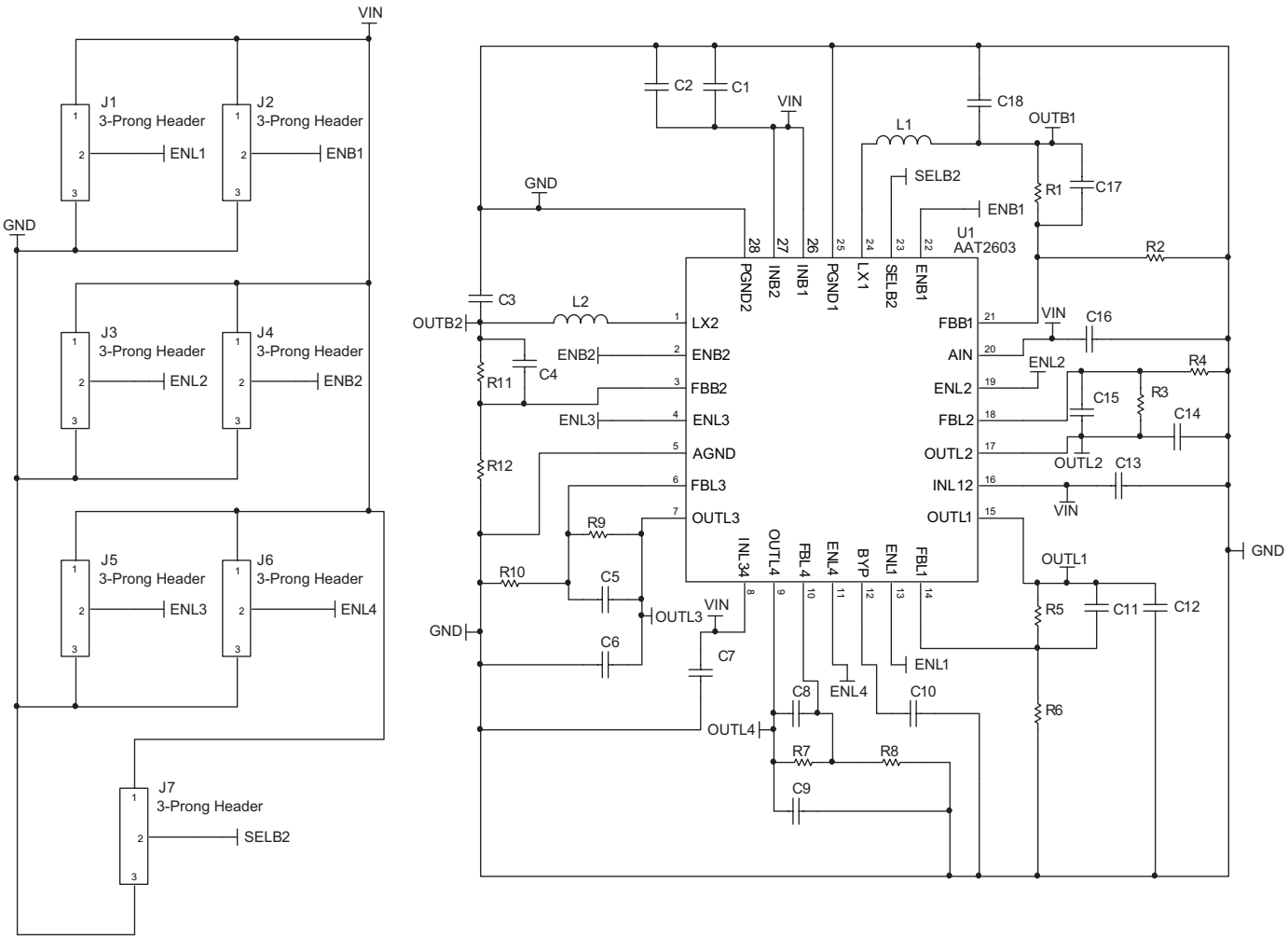


Figure 3: AAT2603 Evaluation Board Schematic.

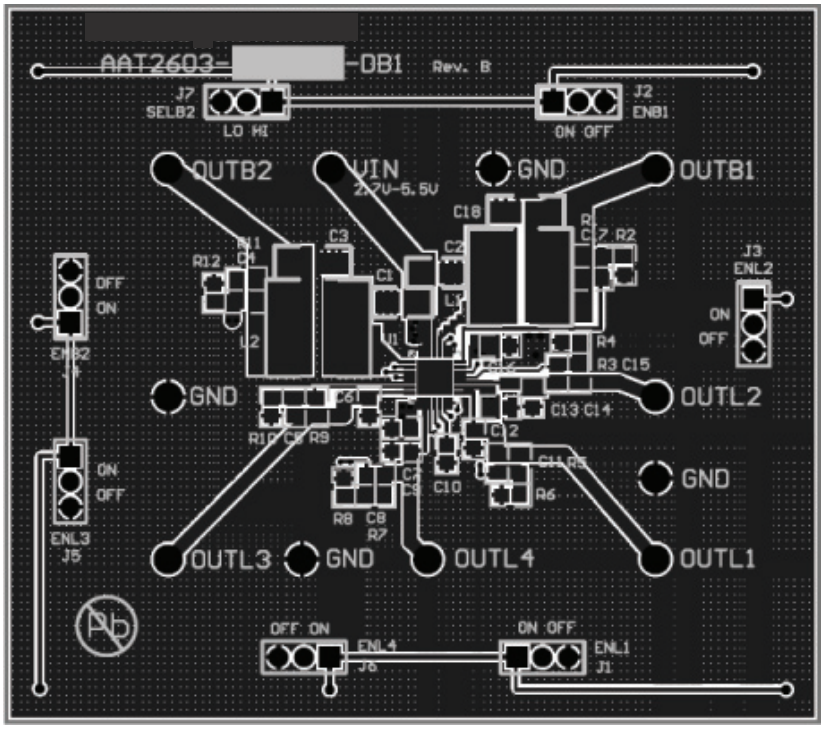


Figure 4: AAT2603 Evaluation Board Top Side PCB Layout.

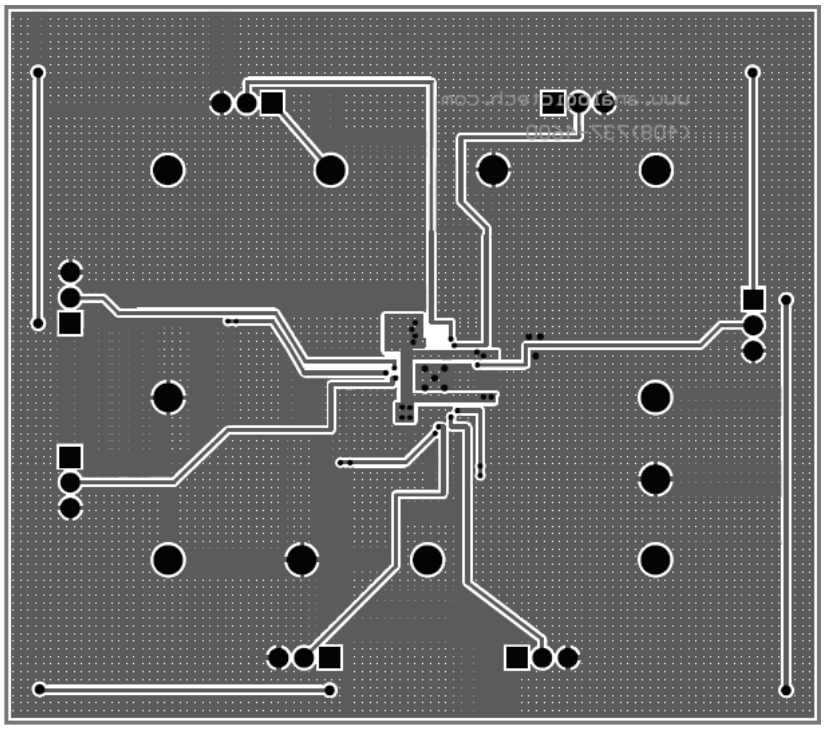


Figure 5: AAT2603 Evaluation Board Bottom Side PCB Layout.

Ordering Information

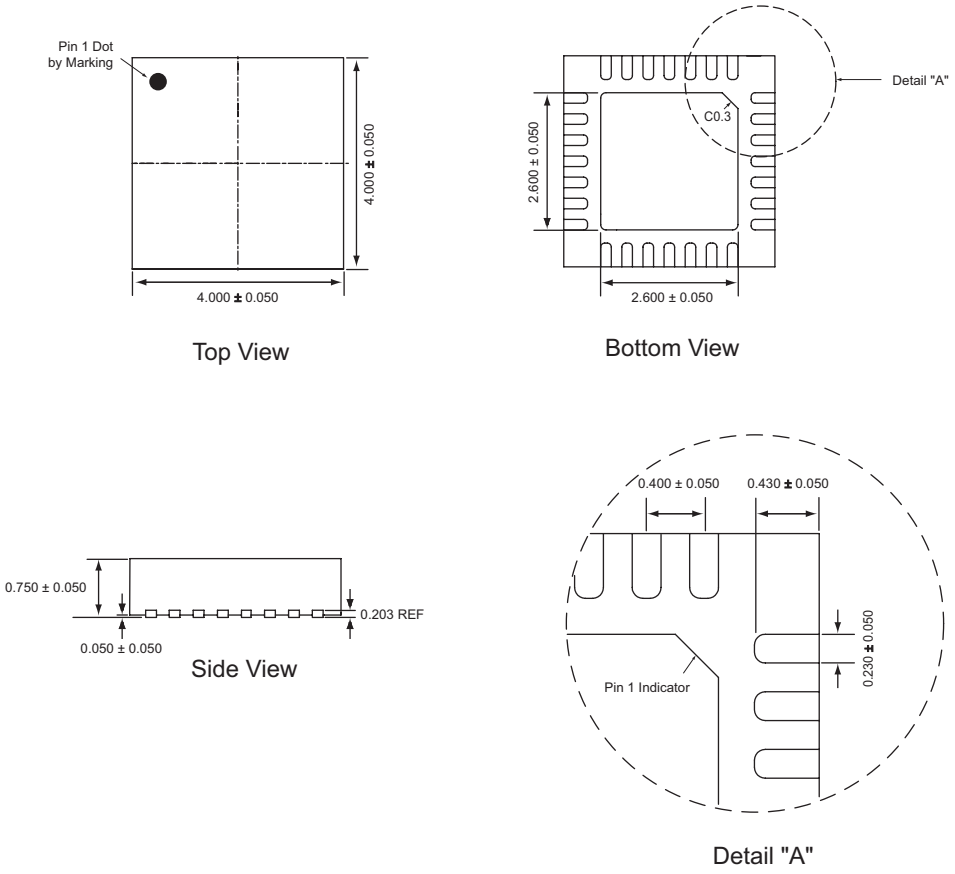
Package	Output Voltage[1]			Marking[2]	Part Number (Tape and Reel)[3]
	DC-DC1 (Buck1)	DC-DC2 (Buck2) (SELB2 = Low)	DC-DC2 (Buck2) (SELB2 = High)		
TQFN44-28	Ext. Adj. (V_{REF} = 600mV)	Ext. Adj. (VV_{REF} = 600mV)	Ext. Adj. (VV_{REF}= 775mV)	3AXYY	**AAT2603INJ-1-T1**
TQFN44-28	3.3V	1.3V	1.0V	9TXYY	**AAT2603INJ-2-T1**
TQFN44-28	Ext. Adj. (V_{REF} = 600mV)	1.0V	1.3V		AAT2603INJ-3-T1

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

1. Buck 1 and Buck 2 output voltages can be factory programmed to most common output voltages. Contact your local sales representative for availability and minimum order quantities.
2. XYY = assembly and date code.
3. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information

TQFN44-28



1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.