



CMOS, 2.5 Ω Low Voltage, Triple/Quad SPDT Switches in Chip Scale

Preliminary Technical Data

ADG786/ADG788

FEATURES

+1.8 V to +5.5 V Single Supply
+/-3 V Dual Supply
2.5 Ω On Resistance
0.5 Ω On Resistance Flatness
100pA Leakage Currents
19ns Switching Times
Triple SPDT : ADG786
Quad SPDT : ADG788
Small Chip Scale Package
Low Power Consumption
TTL/CMOS Compatible Inputs

APPLICATIONS

Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching
Battery Powered Systems

GENERAL DESCRIPTION

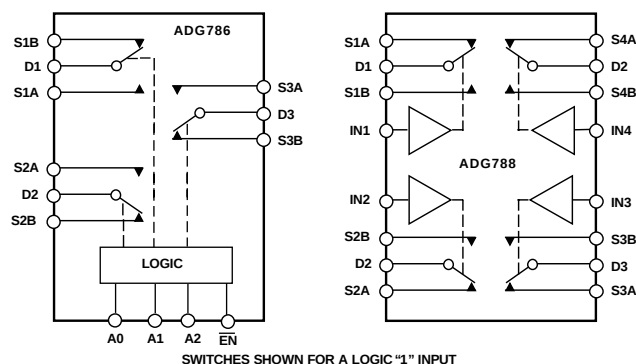
The ADG786 and ADG788 are low voltage, CMOS devices comprising three independently selectable SPDT (single pole, double throw) switches and four independently selectable SPDT switches respectively.

Low power consumption and operating supply range of +1.8 V to +5.5 V and dual +/-3 V make the ADG786 and ADG788 ideal for battery powered, portable instruments. All channels exhibit break before make switching action preventing momentary shorting when switching channels. An $\overline{\text{EN}}$ input on the ADG786 is used to enable or disable the device. When disabled, all channels are switched OFF.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, high signal bandwidths and low leakage currents. On resistance is in the region of a few Ohms, is closely matched between switches and very flat over the full signal range. These parts can operate equally well in either direction and have an input signal range which extends to the supplies.

The ADG786 and ADG788 are available in small Chip Scale packages.

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. Single/Dual Supply Operation. The ADG786 and ADG788 are fully specified and guaranteed with +3 V and +5 V single supply and +/-3 V dual supply rails.
2. Low On Resistance (2.5 Ω typical).
3. Low Power Consumption (<0.01 μW).
4. Guaranteed Break-Before-Make Switching Action.
5. Available in Chip Scale Package (CSP).

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ADG786/ADG788—SPECIFICATIONS¹

($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version		Units	Test Conditions/Comments	
	+25°C	−40°C to +85°C			
ANALOG SWITCH					
Analog Signal Range	0 V to V _{DD}		V	V _S = 0 V to V _{DD} , I _{DS} = 10 mA; Test Circuit 1 V _S = 0 V to V _{DD} , I _{DS} = 10 mA V _S = 0 V to V _{DD} , I _{DS} = 10 mA	
On-Resistance (R _{ON})	2.5		Ω typ		
	4.5	5.0	Ω max		
On-Resistance Match Between Channels (ΔR _{ON})		0.1	Ω typ		
		0.4	Ω max		
On-Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ		
		1.2	Ω max		
LEAKAGE CURRENTS					
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = 5.5 V V _D = 4.5 V/1 V, V _S = 1 V/4.5 V; Test Circuit 2 V _D = V _S = 1 V, or 4.5V; Test Circuit 3	
	±10	±20	nA max		
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ		
	±10	±20	nA max		
DIGITAL INPUTS					
Input High Voltage, V _{INH}		2.4	V min	V _{IN} = V _{INL} or V _{INH}	
Input Low Voltage, V _{INL}		0.8	V max		
Input Current					
I _{INL} or I _{INH}	0.005		μA typ		
		±0.1	μA max		
C _{IN} , Digital Input Capacitance	4		pF typ		
DYNAMIC CHARACTERISTICS ²					
t _{ON}	19	34	ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 3 V, Test Circuit 4 R _L = 300 Ω, C _L = 35 pF; V _S = 3 V, Test Circuit 4 R _L = 300 Ω, C _L = 35 pF; V _S = 3 V, Test Circuit 5 R _L = 300 Ω, C _L = 35 pF; V _S = 3 V, Test Circuit 5 R _L = 300 Ω, C _L = 35 pF; V _S = 3 V, Test Circuit 6 V _S = 2 V, R _S = 0 Ω, C _L = 1 nF; Test Circuit 7 R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 8 R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 9 R _L = 50 Ω, C _L = 5 pF, Test Circuit 8	
			ns max		
t _{OFF}	7	12	ns typ		
			ns max		
ADG786 t _{ON(EN)}	20	40	ns typ		
			ns max		
t _{OFF(EN)}	7	12	ns typ		
			ns max		
Break-Before-Make Time Delay, t _D	13	1	ns typ		
			ns min		
Charge Injection	±3		pC typ		
Off Isolation	-62		dB typ		
	-82		dB typ		
Channel to Channel Crosstalk	-62		dB typ		
	-82		dB typ		
-3 dB Bandwidth	200		MHz typ		
C _S (OFF)	11		pF typ		
C _D , C _S (ON)	34		pF typ		
POWER REQUIREMENTS					
I _{DD}	0.001	1.0	μA typ		V _{DD} = +5.5 V
			μA max	Digital Inputs = 0 V or +5.5 V	

NOTES

¹Temperature range is as follows: B Version: –40°C to +85°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Preliminary Technical Data

ADG786/ADG788

SPECIFICATIONS¹ ($V_{DD} = 3V \pm 10\%$, $V_{SS} = 0V$, $GND = 0V$, unless otherwise noted)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On-Resistance (R _{ON})	6		Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA; Test Circuit 1
	11	12	Ω max	
On-Resistance Match Between Channels (ΔR _{ON})		0.1	Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
On-Resistance Flatness (R _{FLAT(ON)})		0.5	Ω max	
		3	Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = 3.3 V
	±10	±20	nA max	V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	V _S = V _D = +1 V or +3 V; Test Circuit 3
	±10	±20	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	
Input Low Voltage, V _{INL}		0.4	V max	
Input Current I _{INL} or I _{INH}	0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1	μA max	
C _{IN} , Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	28		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V, Test Circuit 4
		55	ns max	
t _{OFF}	9		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V, Test Circuit 4
		16	ns max	
ADG786 t _{ON} (EN)	29		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V, Test Circuit 5
		60	ns max	
t _{OFF} (EN)	9		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V, Test Circuit 5
		16	ns max	
Break-Before-Make Time Delay, t _D	22		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V, Test Circuit 6
		1	ns min	
Charge Injection	±3		pC typ	V _S = 1 V, R _S = 0 Ω, C _L = 1 nF; Test Circuit 7
Off Isolation	-62		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 8
	-82		dB typ	
Channel to Channel Crosstalk	-62		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 9
	-82		dB typ	
-3 dB Bandwidth	200		MHz typ	R _L = 50 Ω, C _L = 5 pF, Test Circuit 8
C _S (OFF)	11		pF typ	
C _D , C _S (ON)	34		pF typ	
POWER REQUIREMENTS				
I _{DD}	0.001		μA typ	V _{DD} = +3.3 V
		1.0	μA max	Digital Inputs = 0 V or +3.3 V

NOTES

¹Temperature ranges are as follows: B Version: -40°C to +85°C.²Guaranteed by design, not subject to production test.

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ADG786/ADG788

Preliminary Technical Data

Dual Supply¹ ($V_{DD} = +3\text{ V} \pm 10\%$, $V_{SS} = -3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	2.5		Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1
	4.5	5.0	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.1	Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
		0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
		1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = +3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$ $V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 2
	± 10	± 20	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$, Test Circuit 3
	± 10	± 20	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS ²				
t_{ON}	21		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 4
		35	ns max	
t_{OFF}	10		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 4
		16	ns max	
ADG786 $t_{ON(EN)}$	21		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 5
		40	ns max	
$t_{OFF(EN)}$	10		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 5
		16	ns max	
Break-Before-Make Time Delay, t_D	13		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, Test Circuit 6
		1	ns min	
Charge Injection	± 5		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 7
Off Isolation	-62		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
	-82		dB typ	
Channel to Channel Crosstalk	-62		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 9
	-82		dB typ	
-3 dB Bandwidth	200		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	11		pF typ	
C_D , C_S (ON)	34		pF typ	
POWER REQUIREMENTS				
				$V_{DD} = +3.3\text{ V}$
I_{DD}	0.001		μA typ	Digital Inputs = 0 V or +3.3 V
		1.0	μA max	
I_{SS}	0.001		μA typ	$V_{SS} = -3.3\text{ V}$
		1.0	μA max	Digital Inputs = 0 V or +3.3 V

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.²Guaranteed by design, not subject to production test.

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Preliminary Technical Data

ADG786/ADG788

ABSOLUTE MAXIMUM RATINGS¹(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+7 V
V _{DD} to GND	-0.3 V to +7 V
V _{SS} to GND	+0.3 V to -3.5 V
Analog Inputs ²	V _{SS} - 0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	-0.3V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C

Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
20 Lead CSP, θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature	+220°C
ESD	2kV

NOTES

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

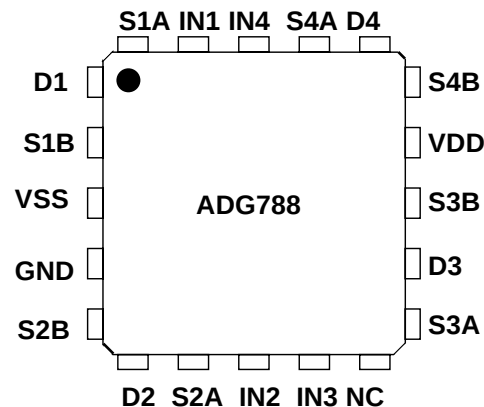
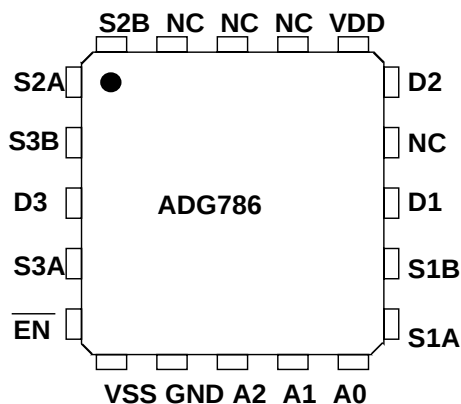
²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG786/ADG788 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
ADG786BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-20
ADG788BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-20

PIN CONFIGURATIONS

Exposed Pad tied to Substrate, V_{SS}

ADG786/ADG788

Preliminary Technical Data

Table 1. ADG786 Truth Table

A2	A1	A0	$\overline{E} \overline{N}$	ON Switch
X	X	X	1	NONE
0	0	0	0	D1-S1A, D2-S2A, D3-S3A
0	0	1	0	D1-S1B, D2-S2A, D3-S3A
0	1	0	0	D1-S1A, D2-S2B, D3-S3A
0	1	1	0	D1-S1B, D2-S2B, D3-S3A
1	0	0	0	D1-S1A, D2-S2A, D3-S3B
1	0	1	0	D1-S1B, D2-S2A, D3-S3B
1	1	0	0	D1-S1A, D2-S2B, D3-S3B
1	1	1	0	D1-S1B, D2-S2B, D3-S3B

X = Don't Care

Table 1. ADG788 Truth Table

Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most Negative power supply in a dual supply application. In single supply applications, this should be tied to ground close to the device.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
$V_D (V_S)$	Analog voltage on terminals D, S
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels, i.e. $R_{ONmax} - R_{ONmin}$
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
$I_{INL}(I_{INH})$	Input current of the digital input.
C_S (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
C_D, C_S (ON)	"ON" switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
$t_{TRANSITION}$	Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
$t_{ON}(EN)$	Delay time between the 50% and 90% points of the EN digital input and the switch "ON" condition.
$t_{OFF}(EN)$	Delay time between the 50% and 90% points of the EN digital input and the switch "OFF" condition.
t_{OPEN}	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The frequency at which the output is attenuated by 3dBs.
On Response	The Frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS

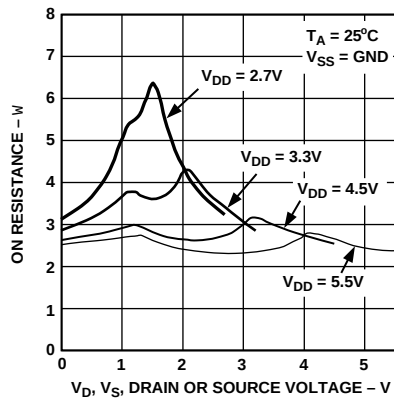


Figure 1. On Resistance as a Function of $V_D(V_S)$ for Single Supply

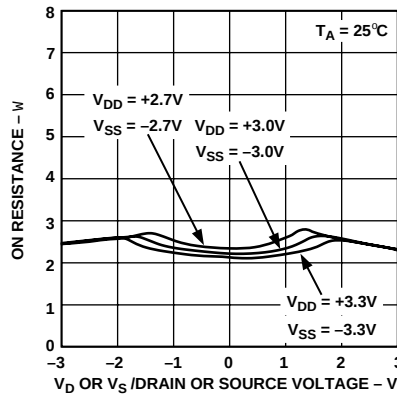


Figure 2. On Resistance as a Function of $V_D(V_S)$ for Dual Supply

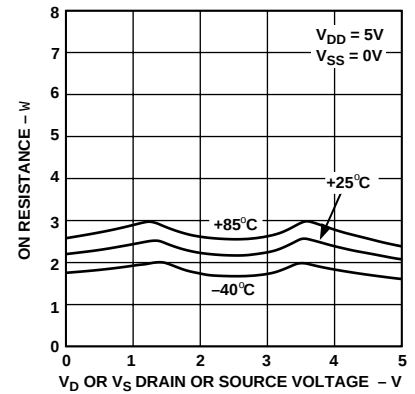


Figure 3. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply

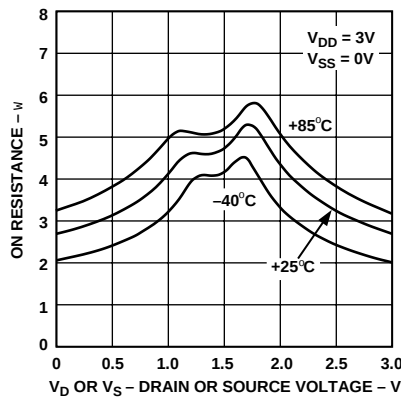


Figure 4. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply

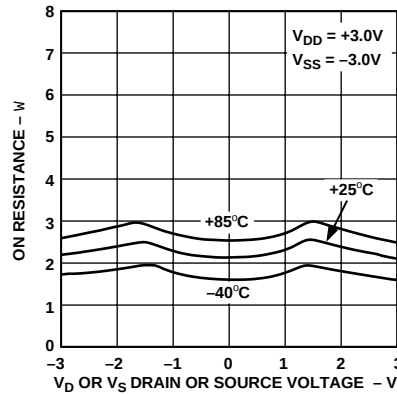


Figure 5. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Dual Supply

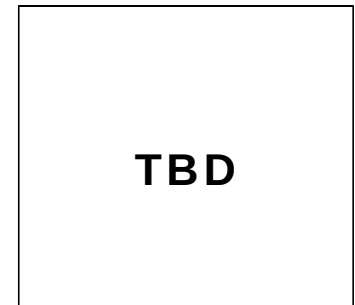


Figure 6. Leakage Currents as a function of $V_D(V_S)$

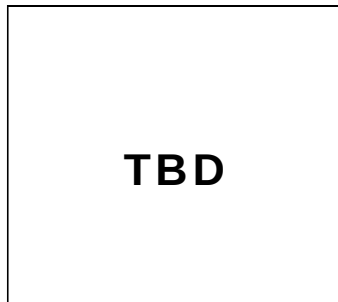


Figure 7. Leakage Currents as a function of $V_D(V_S)$

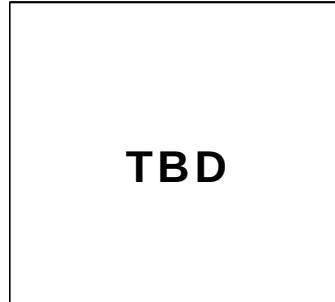


Figure 8. Leakage Currents as a function of $V_D(V_S)$

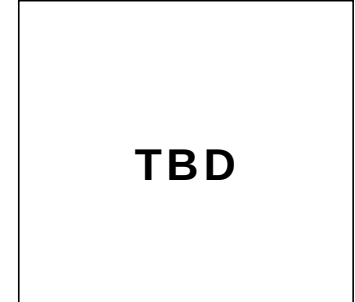


Figure 9. Leakage Currents as a function of Temperature

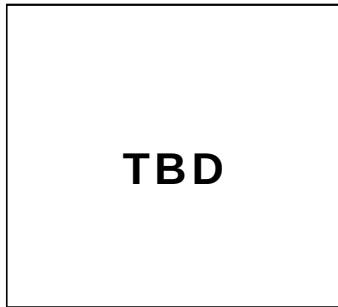


Figure 10. Leakage Currents as a Function of Temperature

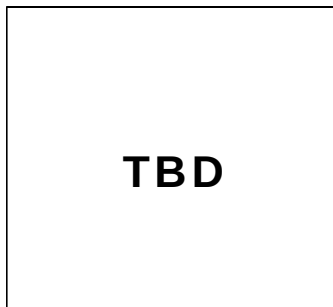


Figure 11. T_{ON}/T_{OFF} Times vs. Temperature

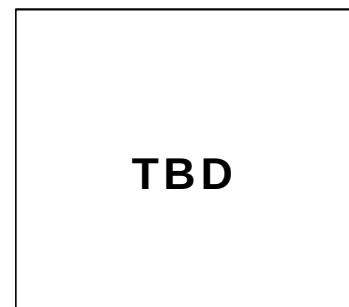


Figure 12. On Response vs. Frequency

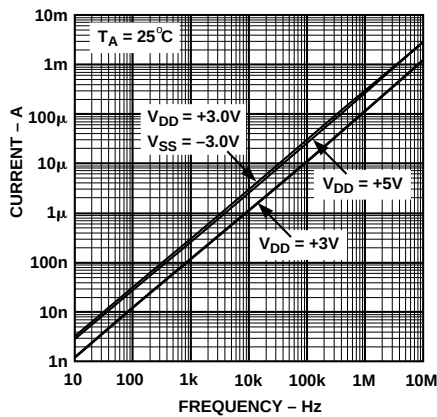


Figure 13. Supply Currents vs. Input Switching Frequency

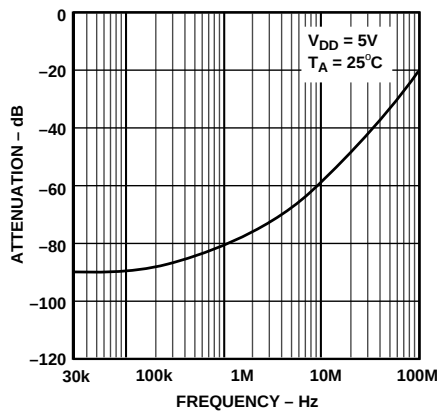


Figure 14. Off Isolation vs. Frequency

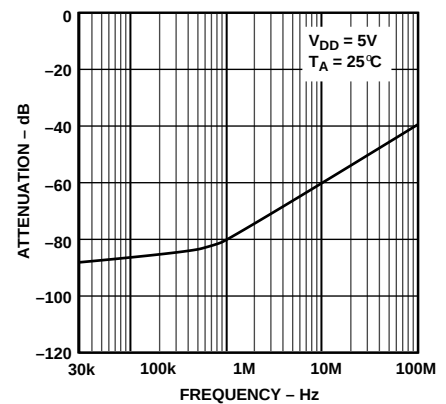


Figure 15. Crosstalk vs. Frequency

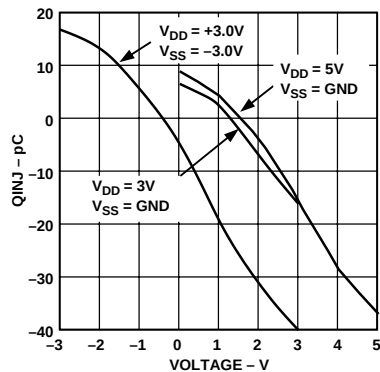
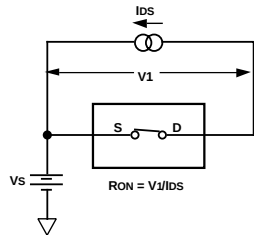
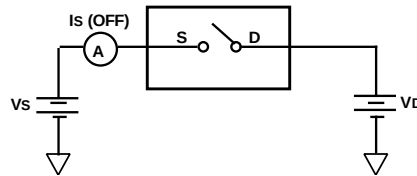


Figure 16. Charge Injection vs. Source Voltage

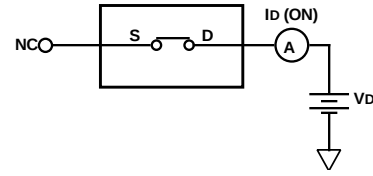
Test Circuits



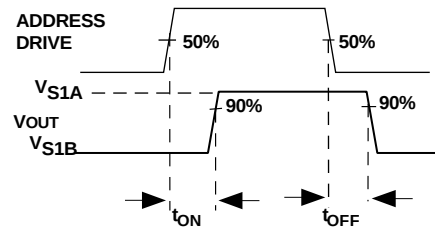
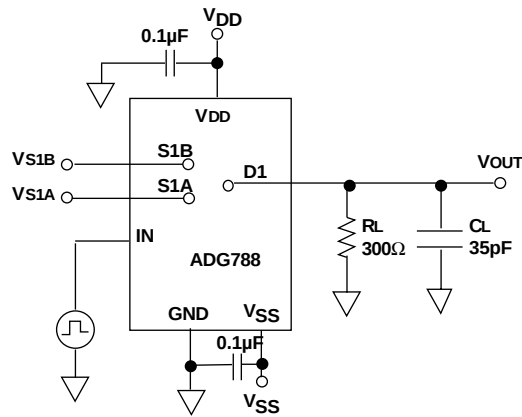
Test Circuit 1. On Resistance.



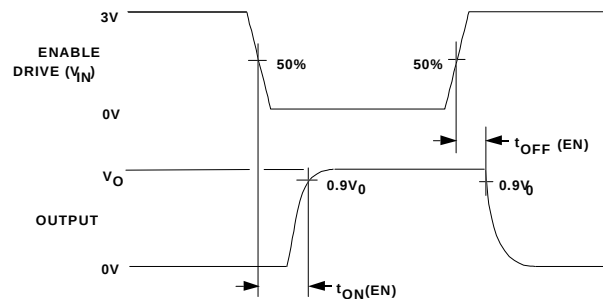
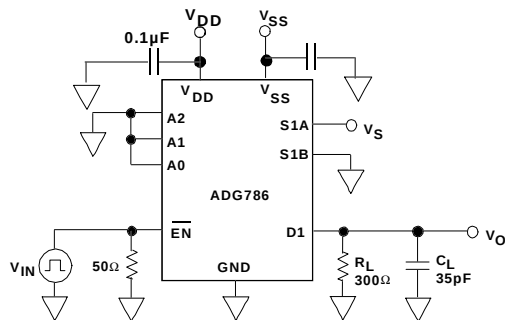
Test Circuit 2. I_S (OFF).



Test Circuit 3. I_D (ON)



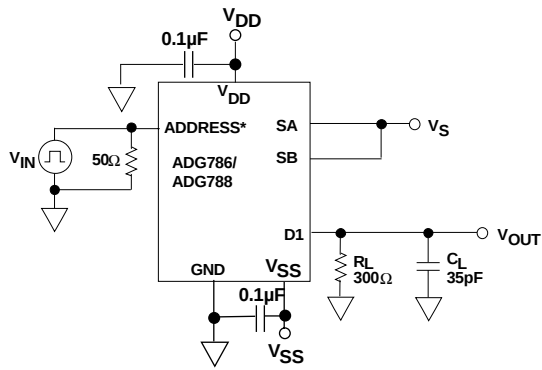
Test Circuit 4. Switching Times.



Test Circuit 5. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$.

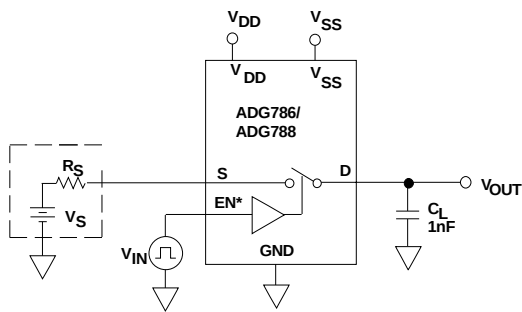
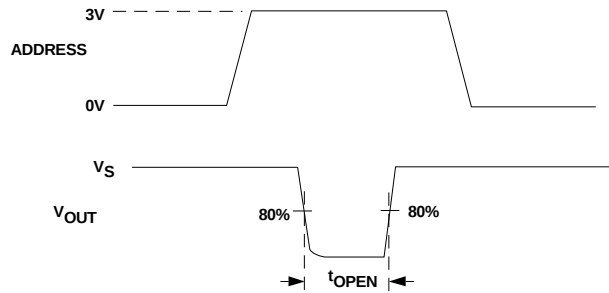
ADG786/ADG788

Preliminary Technical Data



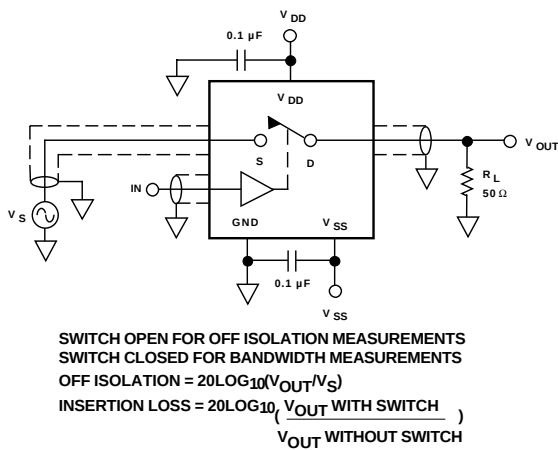
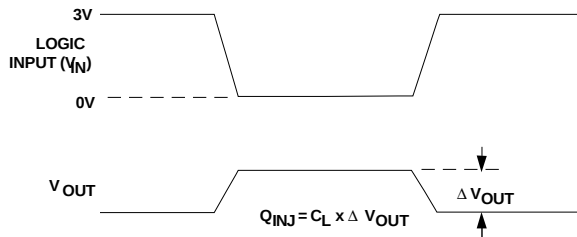
*A0, A1, A2 for ADG786, IN1-4 for ADG788

Test Circuit 6. Break Before Make Delay, t_{OPEN} .



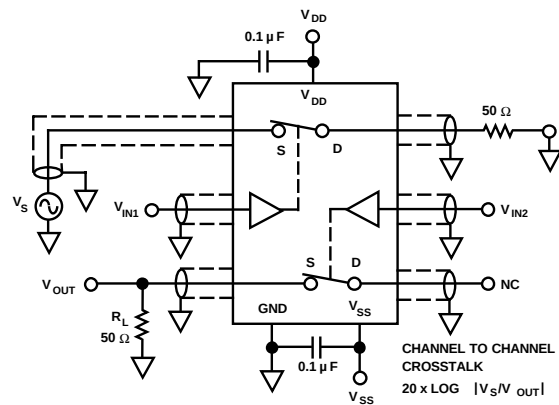
* IN1-4 for ADG786

Test Circuit 7. Charge Injection.



SWITCH OPEN FOR OFF ISOLATION MEASUREMENTS
SWITCH CLOSED FOR BANDWIDTH MEASUREMENTS
OFF ISOLATION = $20 \log_{10}(V_{OUT}/V_S)$
INSERTION LOSS = $20 \log_{10} \left(\frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}} \right)$

Test Circuit 8. OFF Isolation and Bandwidth.



Test Circuit 9. Channel-to-Channel Crosstalk.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**20-Lead CSP
(CP-20)**