# 74AHC08; 74AHCT08

### **Quad 2-input AND gate**

Rev. 4 — 26 May 2020

**Product data sheet** 

### 1. General description

The 74AHC708; 74AHC708 are quad 2-input AND gates. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

#### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Input levels:
  - For 74AHC08: CMOS level
  - For 74AHCT08: TTL level
- · Balanced propagation delays
- · All inputs have a Schmitt-trigger action
- Overvoltage tolerant inputs to 5.5 V
- · High noise immunity
- · CMOS low power dissipation
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- · Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

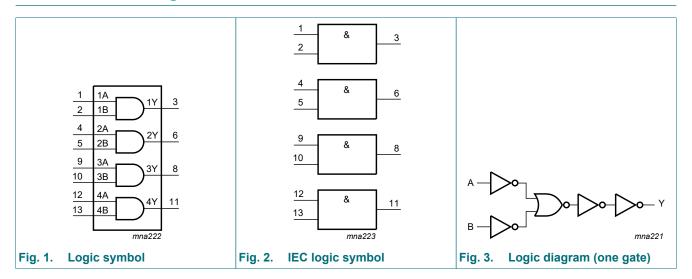
### 3. Ordering information

#### **Table 1. Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74AHC08D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1
74AHCT08D			body width 3.9 mm	
74AHC08PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1
74AHCT08PW			body width 4.4 mm	
74AHC08BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal	SOT762-1
74AHCT08BQ			enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	

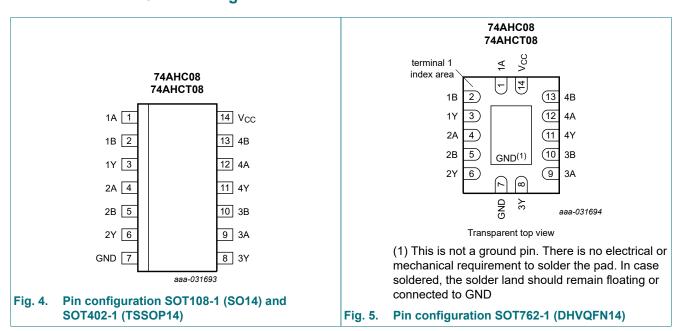


### 4. Functional diagram



### 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Table 2. I ill description		
Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data inputs
1B, 2B, 3B, 4B	2, 5, 10, 13	data inputs
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data outputs
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

### 6. Functional description

#### **Table 3. Function selection**

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care$ 

Input		Output
nA	nB	nY
L	X	L
Х	L	L
Н	Н	Н

### 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
V <sub>I</sub>	input voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1]	-20	-	mA
I <sub>OK</sub>	output clamping current	$V_{O}$ < -0.5 V or $V_{O}$ > $V_{CC}$ + 0.5 V	[1]	-	±20	mA
Io	output current	$V_O = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I <sub>CC</sub>	supply current			-	75	mA
I <sub>GND</sub>	ground current			-75	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

### 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		74AHC08			74AHCT08			
			Min	Тур	Max	Min	Тур	Max		
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V	
VI	input voltage		0	-	5.5	0	-	5.5	V	
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V	
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C	
Δt/ΔV	input transition rise and	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	-	-	-	ns/V	
	fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V	

<sup>[2]</sup> For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

### 9. Static characteristics

#### **Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC0	8									
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	٧
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	٧
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	٧
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	٧
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	٧
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	٧
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.4	-	٧
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.7	-	٧
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 V$	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	μA
Cı	input capacitance		-	3.0	10	-	10	-	10	pF
74AHCT	08									
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	8.0	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 V$								
	output voltage	I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 V$								
	output voltage	I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
lı	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>cc</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C t	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
ΔI <sub>CC</sub>		per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other pins at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance		-	3.0	10	-	10	-	10	pF

### 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

GND = 0 V; For test circuit see Fig. 7.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C t	Unit	
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC0	8										•
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6	[2]								
	delay	V <sub>CC</sub> = 3.0 V to 3.6 V									
		C <sub>L</sub> = 15 pF		-	4.0	8.8	1.0	10.5	1.0	11.0	ns
		C <sub>L</sub> = 50 pF		-	5.6	12.3	1.0	14	1.0	15.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF		-	3.0	5.9	1.0	7.0	1.0	7.5	ns
		C <sub>L</sub> = 50 pF			4.2	7.9	1.0	9.0	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$	[3]	-	10.0	-	-	-	-	-	pF
74AHCT	08										
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6	[2]								
	delay	V <sub>CC</sub> = 4.5 V to 5.5 V									
		C <sub>L</sub> = 15 pF		-	3.2	6.9	1.0	8.0	1.0	9.0	ns
		C <sub>L</sub> = 50 pF		-	4.2	7.9	1.0	9.0	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$	[3]	-	12.0	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ( $V_{CC}$  = 3.3 V and  $V_{CC}$  = 5.0 V).
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
   [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

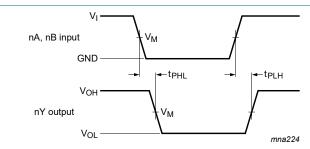
 $C_L$  = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

#### 10.1. Waveform and test circuit



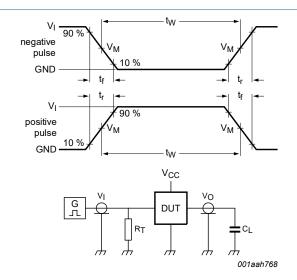
Measurement points are given in Table 8.

 $\ensuremath{V_{\text{OL}}}$  and  $\ensuremath{V_{\text{OH}}}$  are typical voltage output levels that occur with the output load.

Fig. 6. The input (nA, nB) to output (nY) propagation delays

**Table 8. Measurement points** 

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74AHC08	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74AHCT08	1.5 V	0.5V <sub>CC</sub>



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $C_L$  = load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

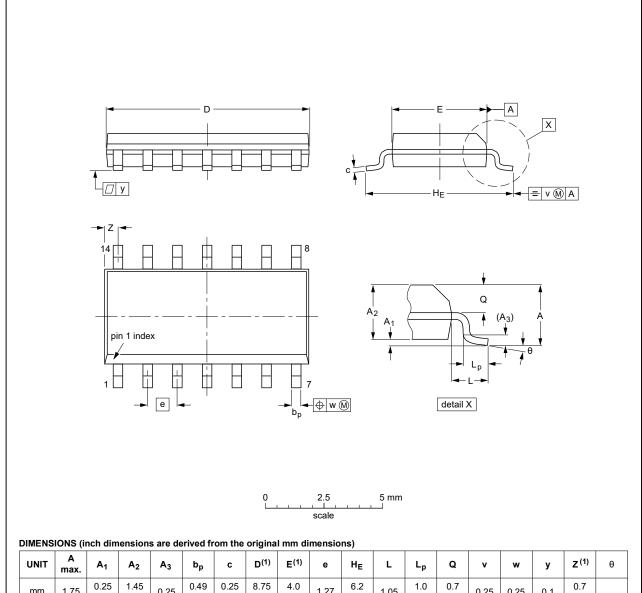
Table 9. Test data

Туре	Input Lo		Load	Test		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL			
74AHC08	V <sub>CC</sub>	≤ 3.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>		
74AHCT08	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>		

### 11. Package outline

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	Α3	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

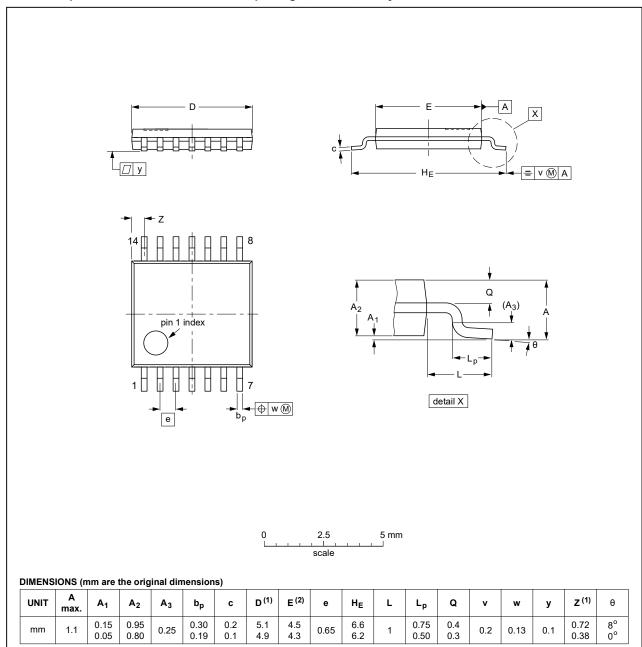
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				<del>99-12-27</del> 03-02-18

Fig. 9. Package outline SOT402-1 (TSSOP14)

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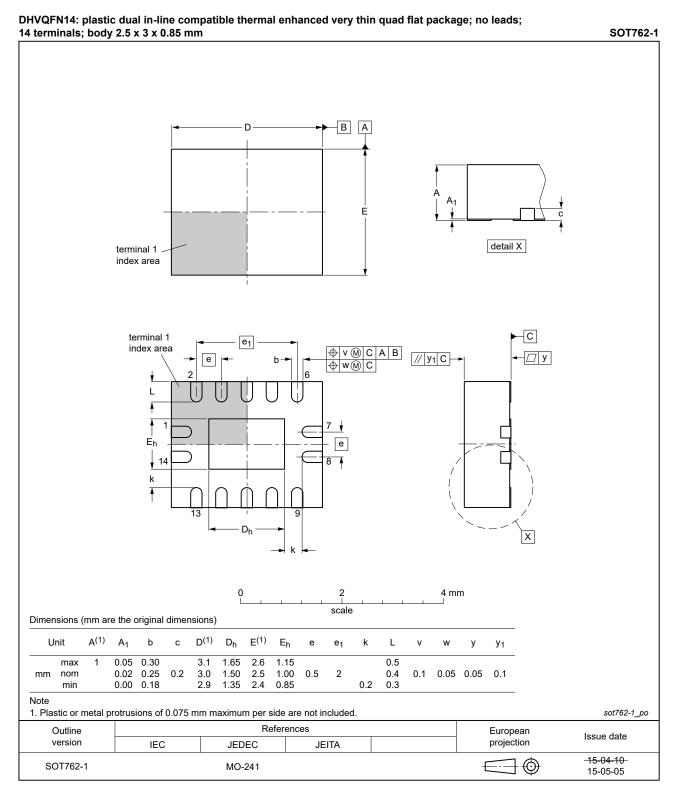


Fig. 10. Package outline SOT762-1 (DHVQFN14)

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### 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

## 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74AHC_AHCT08 v.4	20200526	Product data sheet	-	74AHC_AHCT08 v.3	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 1 and Section 2 updated.</li> <li>Section 7: Derating values for P<sub>tot</sub> total power dissipation have been updated.</li> <li>Fig. 7: Test circuit corrected (Errata).</li> <li>Package outline drawing of SOT762-1 (Fig. 10) updated.</li> </ul>				
74AHC_AHCT08 v.3	20071114	Product data sheet	-	74AHC_AHCT08 v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 3: DHVQFN14 package added.</li> <li>Section 7: derating values added for DHVQFN14 package.</li> <li>Section 11: outline drawing added for DHVQFN14 package.</li> </ul>				
74AHC_AHCT08 v.2	19990924	Product specification	-	74AHC_AHCT08 v.1	
74AHC_AHCT08 v.1	19981218	Product specification	-	-	

### 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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