128KX32 SRAM/FLASH MODULE

FEATURES

- Access Times of 25ns (SRAM) and 70, 90 and 120ns (FLASH)
- Packaging:
  - 66-pin, PGA Type, 1.385 inch square HIP, Hermetic Ceramic HIP (Package 402)
- 128Kx32 SRAM
- 128Kx32 5V Flash
- Organized as 128Kx32 of SRAM and 128Kx32 of Flash Memory with common Data Bus
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight – 13 grams typical

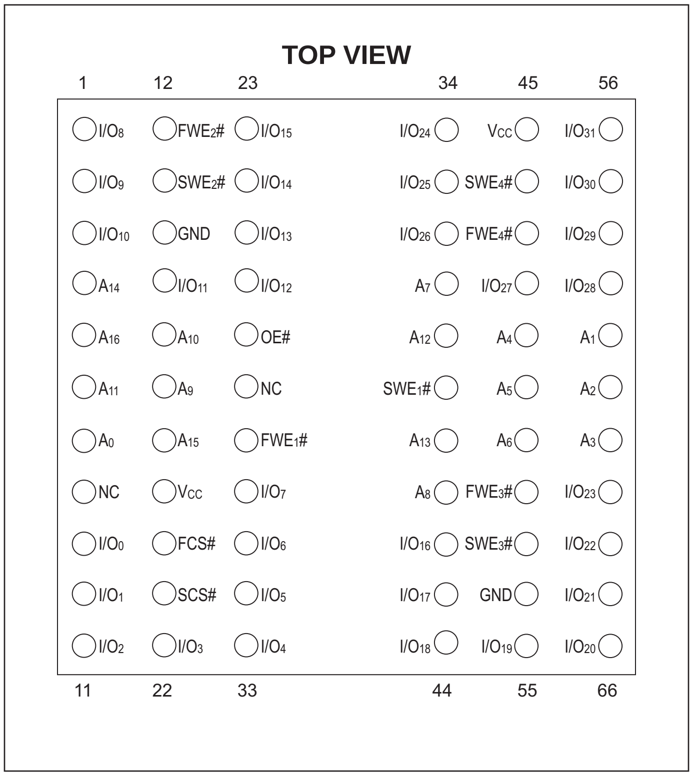
FLASH MEMORY FEATURES

- 10,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 16K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

* This product is under development, not fully characterized, and is subject to change without notice.

Note: Programming information available upon request.

FIGURE 1 – PIN CONFIGURATION FOR WSF128K32-XH2X



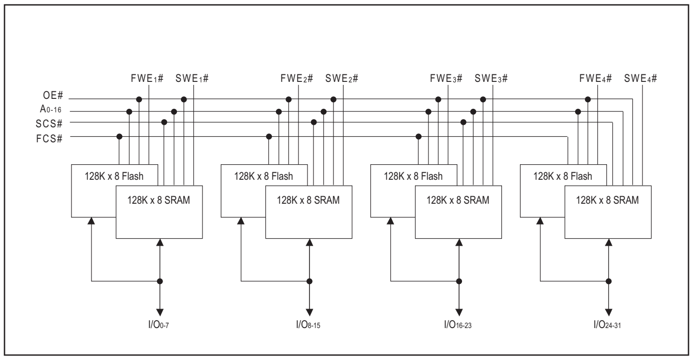
TOP VIEW

1	12	23	34	45	56
I/O$_8$	FWE$_2$#	I/O$_{15}$	I/O$_{24}$	V$_{CC}$	I/O$_{31}$
I/O$_9$	SWE$_2$#	I/O$_{14}$	I/O$_{25}$	SWE$_4$#	I/O$_{30}$
I/O$_{10}$	GND	I/O$_{13}$	I/O$_{26}$	FWE$_4$#	I/O$_{29}$
A$_{14}$	I/O$_{11}$	I/O$_{12}$	A$_7$	I/O$_{27}$	I/O$_{28}$
A$_{16}$	A$_{10}$	OE#	A$_{12}$	A$_4$	A$_1$
A$_{11}$	A$_9$	NC	SWE$_1$#	A$_5$	A$_2$
A$_0$	A$_{15}$	FWE$_1$#	A$_{13}$	A$_6$	A$_3$
NC	V$_{CC}$	I/O$_7$	A$_8$	FWE$_3$#	I/O$_{23}$
I/O$_0$	FCS#	I/O$_6$	I/O$_{16}$	SWE$_3$#	I/O$_{22}$
I/O$_1$	SCS#	I/O$_5$	I/O$_{17}$	GND	I/O$_{21}$
I/O$_2$	I/O$_3$	I/O$_4$	I/O$_{18}$	I/O$_{19}$	I/O$_{20}$
11	22	33	44	55	66

PIN DESCRIPTION

D0-31	Data Inputs/Outputs
A0-16	Address Inputs
SWE1-4#	SRAM Write Enable
SCS#	SRAM Chip Selects
OE#	Output Enable
V$_{CC}$	Power Supply
GND	Ground
NC	Not Connected
FWE1-4#	Flash Write Enable
FCS#	Flash Chip Select

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	7.0	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

Parameter	
Flash Data Retention	10 years
Flash Endurance (write/erase cycles)	10,000

NOTE:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

SRAM TRUTH TABLE

SCS#	OE#	SWE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

NOTE:

1. FCS# must remain high when SCS# is low.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

CAPACITANCE

Ta = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	80	pF
F/S WE$_{1-4}$# capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
F/S CS# capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
D$_{0-31}$ capacitance	$C_{I/O}$	V_{IN} = 0 V, f = 1.0 MHz	30	pF
A$_{0-16}$ capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	80	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	SCS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
SRAM Operating Supply Current x 32 Mode	I_{CCx32}	SCS# = V_{IL}, OE# = FCS# = V_{IH}, f = 5MHz, V_{CC} = 5.5		670	mA
Standby Current	I_{SB}	FCS# = SCS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		80	mA
SRAM Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
SRAM Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V
Flash V_{CC} Active Current for Read (1)	I_{CC1}	FCS# = V_{IL}, OE# = SCS# = V_{IH}		220	mA
Flash V_{CC} Active Current for Program or Erase (2)	I_{CC2}	FCS# = V_{IL}, OE# = SCS# = V_{IH}		280	mA
Flash Output Low Voltage	V_{OL}	I_{OL} = 8.0mA, V_{CC} = 4.5		0.45	V
Flash Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Flash Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	V_{CC} -0.4		V
Flash Low V_{CC} Lock Out Voltage	V_{LKO}		3.2		V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

SRAM AC CHARACTERISTICS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	**Symbol**	**-25**		**Units**
Read Cycle		**Min**	**Max**	
Read Cycle Time	t_{RC}	25		ns
Address Access Time	t_{AA}		25	ns
Output Hold from Address Change	t_{OH}	0		ns
Chip Select Access Time	t_{ACS}		25	ns
Output Enable to Output Valid	t_{OE}		15	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12	ns

1. This parameter is guaranteed by design but not tested.

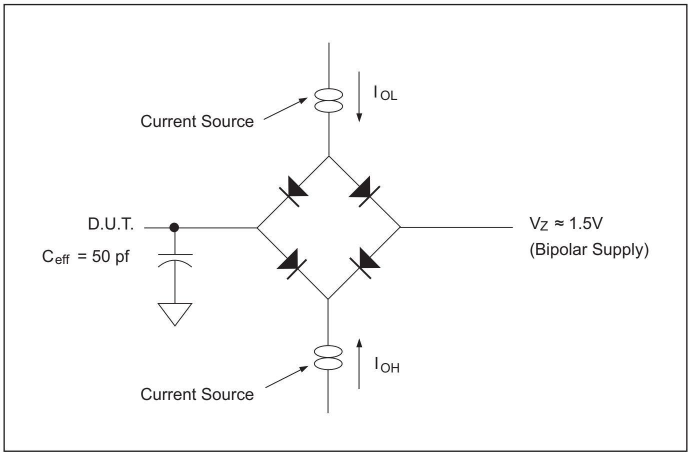
SRAM AC CHARACTERISTICS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	**Symbol**	**-25**		**Units**
Write Cycle		**Min**	**Max**	
Write Cycle Time	t_{WC}	25		ns
Chip Select to End of Write	t_{CW}	20		ns
Address Valid to End of Write	t_{AW}	20		ns
Data Valid to End of Write	t_{DW}	15		ns
Write Pulse Width	t_{WP}	20		ns
Address Setup Time	t_{AS}	3		ns
Address Hold Time	t_{AH}	0		ns
Output Active from End of Write	t_{OW}[1]	3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		15	ns
Data Hold from Write Time	t_{DH}	0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – AC TEST CIRCUIT

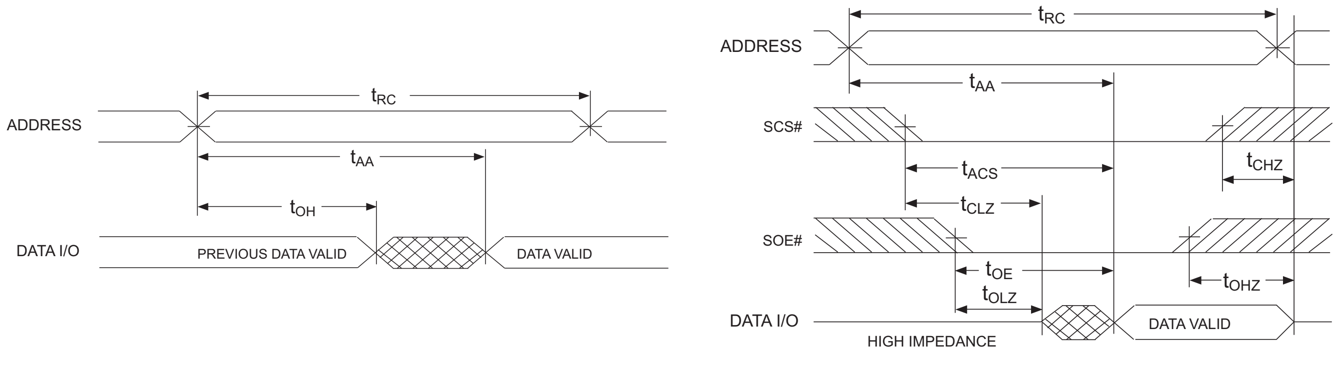


AC TEST CONDITIONS

Parameter	**Typ**	**Unit**
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

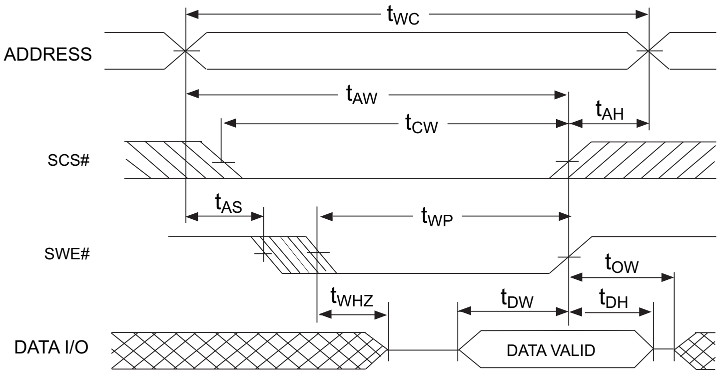
FIGURE 3 – SRAM TIMING WAVEFORM - READ CYCLE



READ CYCLE 1, (SCS# = OE# = V_{IL}, SWE# = FCS# = V_{IH})

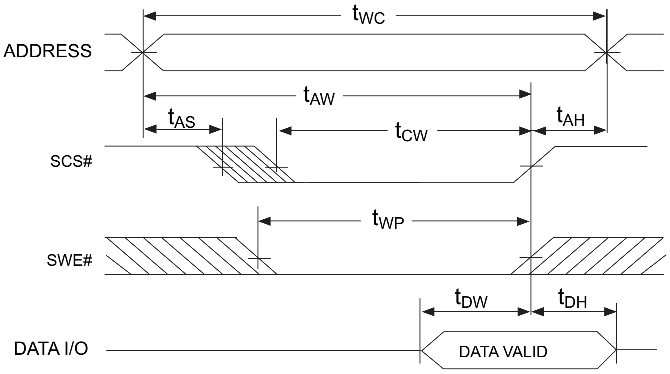
READ CYCLE 2, (SWE# = FCS# = V_{IH})

FIGURE 4 – SRAM WRITE CYCLE - SWE# CONTROLLED



WRITE CYCLE 1, SWE# CONTROLLED (FCS# = V_{IH})

FIGURE 5 – SRAM WRITE CYCLE - SCS# CONTROLLED



WRITE CYCLE 2, SCS# CONTROLLED (FCS# = V_{IH})

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FWE# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-70		-90		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		45		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		45		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		50		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (min)	t_{WHWH1}		14		14		14		µs
Chip and Sector Erase Time	t_{WHWH2}		2.2	60	2.2	60	2.2	60	sec
Read Recovery Time Before Write	t_{GHWL}		0		0		0		µs
V_{CC} Set-up Time		t_{VCS}	50		50		50		µs
Chip Programming Time				12.5		12.5		12.5	sec
Output Enable Setup Time		t_{OES}	0		0		0		ns
Output Enable Hold Time (1)		t_{OEH}	10		10		10		ns

1. For Toggle and Data# Polling.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-70		-90		-120		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	70		90		120		ns
Address Access Time	t_{AVQV}	t_{ACC}		70		90		120	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		70		90		120	ns
OE# to Output Valid	t_{GLQV}	t_{OE}		35		40		50	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		25		30	ns
OE# High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		25		30	ns
Output Hold from Address, FCS# or OE# Change, whichever is first	t_{AXQX}	t_{OH}	0		0		0		ns

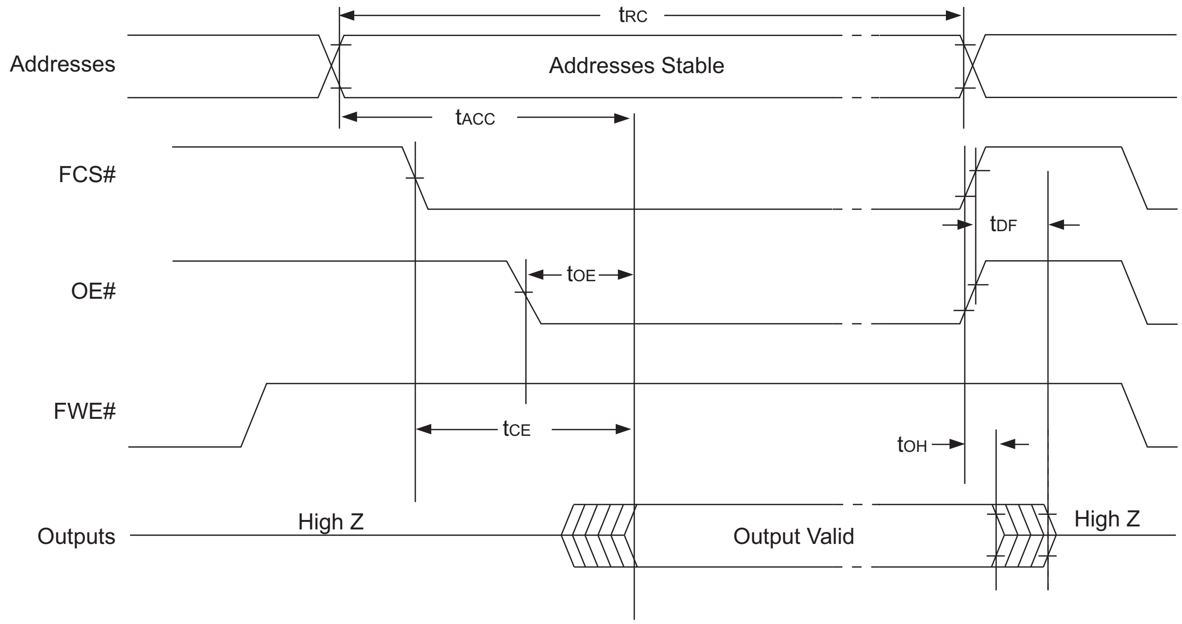
1. Guaranteed by design, not tested.

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

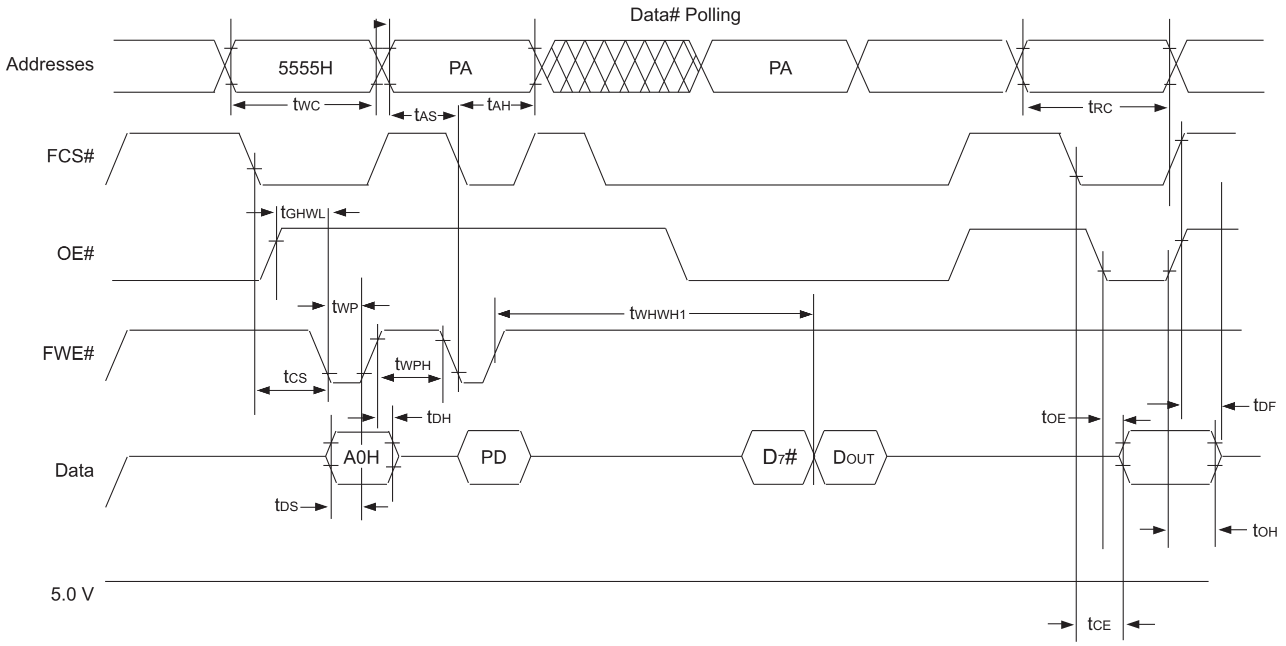
Parameter	Symbol		-70		-90		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		ns
FWE# Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
FCS# Pulse Width	t_{ELEH}	t_{CP}	35		45		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	30		45		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		50		ns
FWE# Hold from FWE# High	t_{EHWH}	t_{WH}	0		0		0		ns
FCS# Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Programming Operation	t_{WHWH1}		14		14		14		µs
Duration of Erase Operation	t_{WHWH2}		2.2	60	2.2	60	2.2	60	sec
Read Recovery before Write	t_{GHEL}		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5	sec

FIGURE 6 – AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS



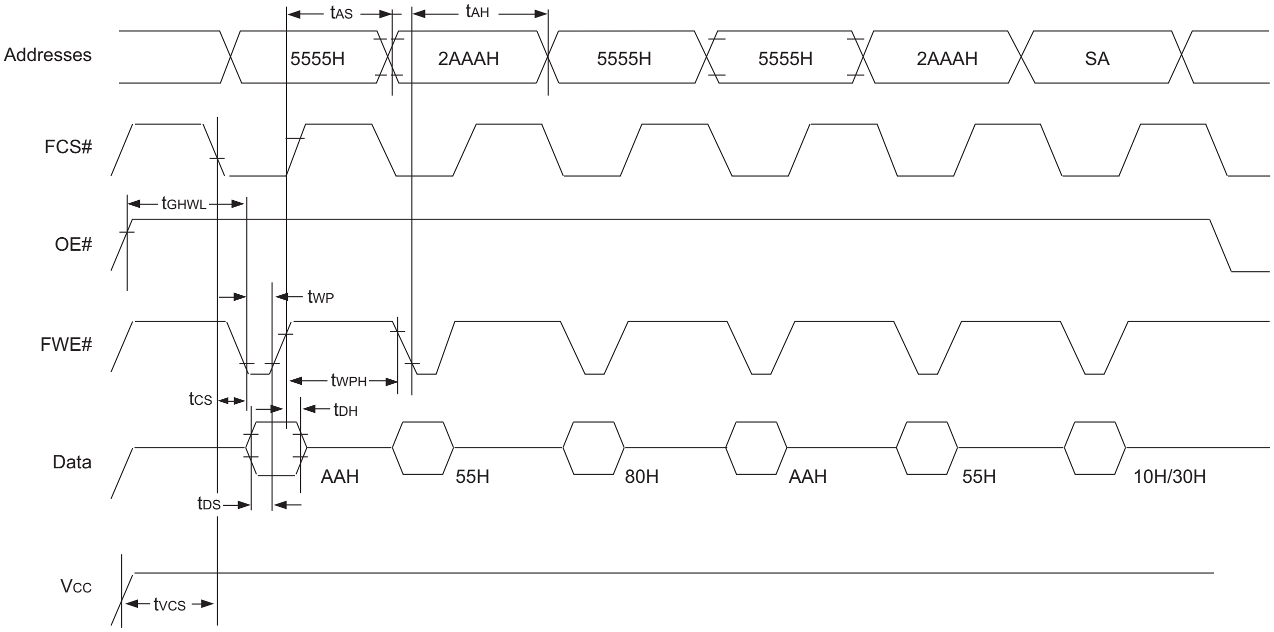
NOTE: SCS# = VIH

FIGURE 7 – WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FWE# CONTROLLED



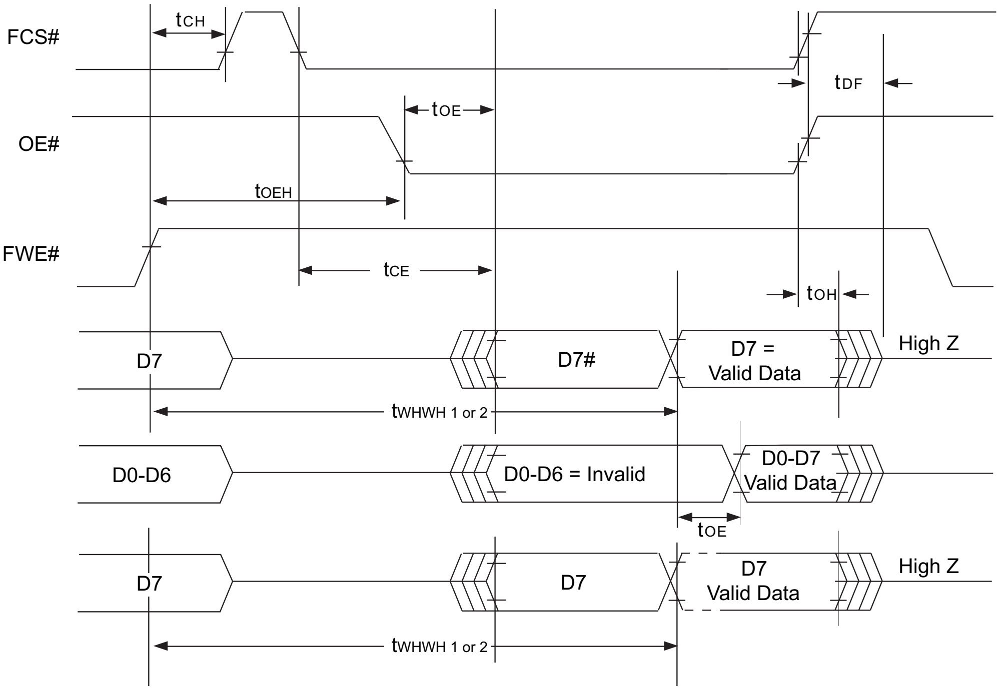
NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D_7# is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. SCS# = V_{IH}

FIGURE 8 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



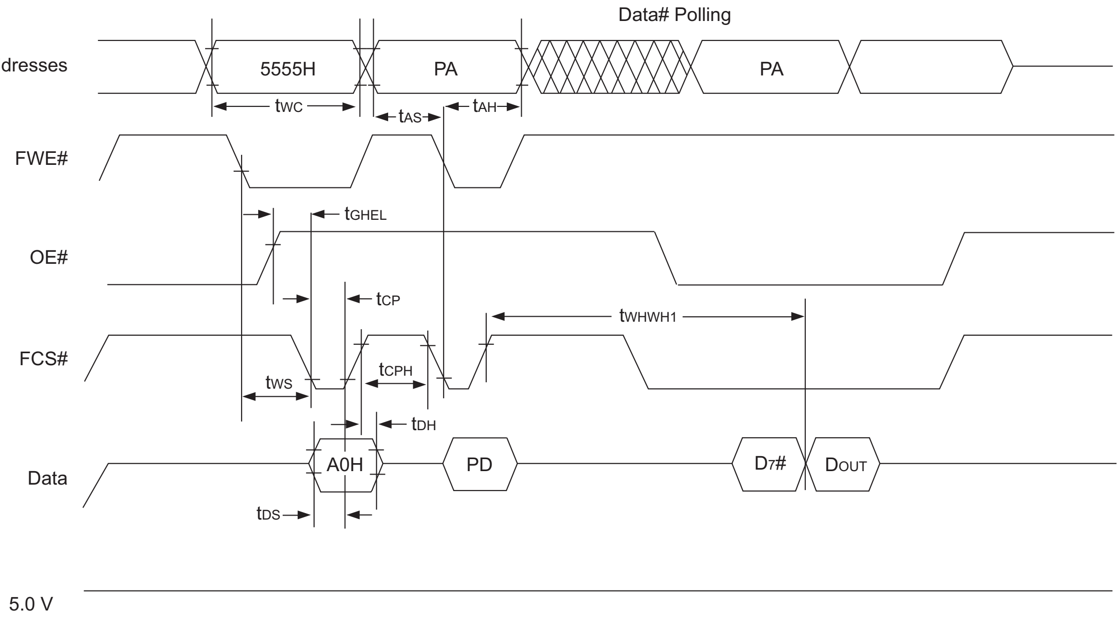
NOTES:
1. SA is the sector address for Sector Erase.
2. SCS# = V_{IH}

FIGURE 9 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY



NOTE: SCS# = V_{IH}

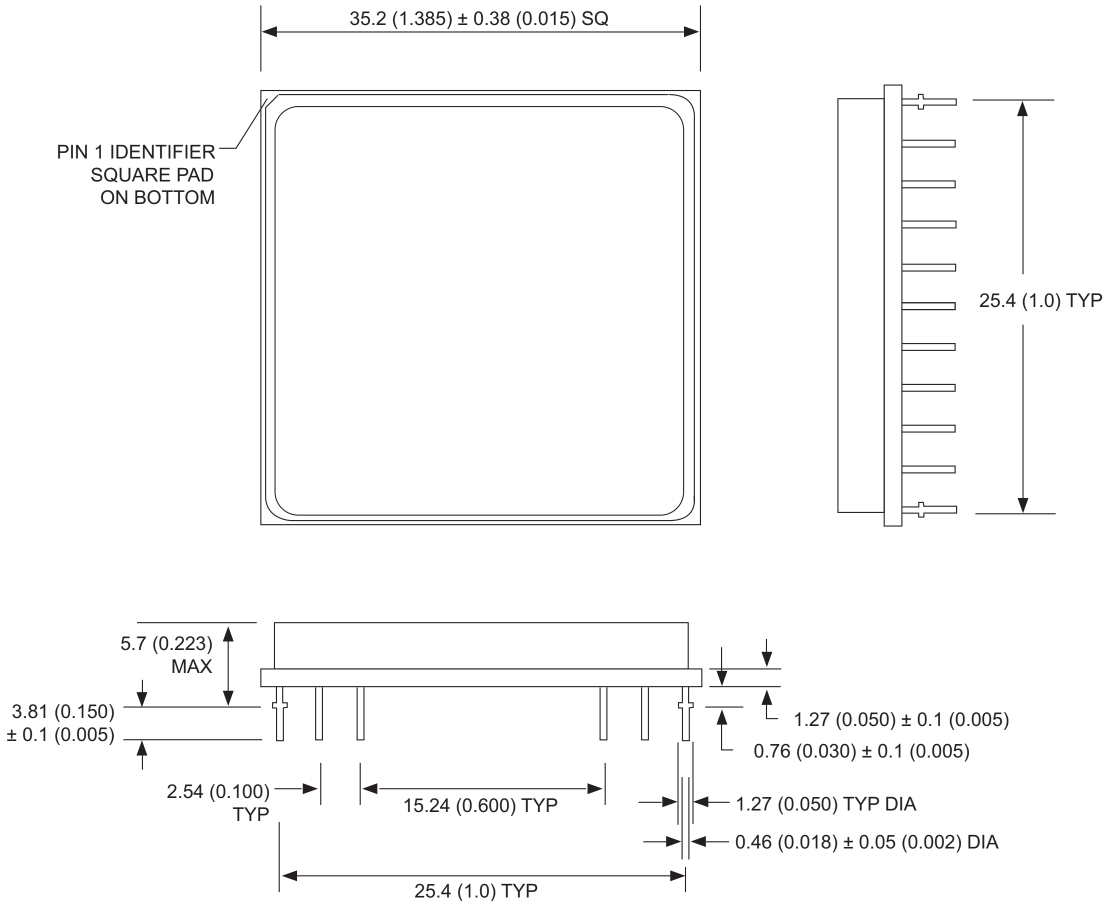
FIGURE 10 – WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, CS# CONTROLLED



NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.
6. SCS# = VIH

PACKAGE 402 – 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S F 128K32 - XX H2 X X

MICROSEMI CORPORATION

SRAM

FLASH PROM

ORGANIZATION, 128K x 32

ACCESS TIME (ns)
- 22 = 25ns SRAM and 120ns FLASH
- 29 = 25ns SRAM and 90ns FLASH
- 27 = 25ns SRAM and 70ns FLASH

PACKAGE TYPE:
- H2 = Ceramic Hex In-line Package, HIP (Package 402)

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

Document Title

128Kx32 SRAM/FLASH MODULE

Revision History

Rev #	History	Release Date	Status
Rev 5	Changes (Pg. 1-14) 5.1 Change document layout from White Electronic Designs to Microsemi 5.2 Add document Revision History page	August 2011	Preliminary