

Dual and Quad, JFET Input Precision High Speed Op Amps

FEATURES

- 14V/ μ s Slew Rate
 - 5MHz Gain-Bandwidth Product
 - Fast Settling Time
 - 150 μ V Offset Voltage (LT1057)
 - 180 μ V Offset Voltage (LT1058)
 - 2 μ V/ $^{\circ}$ C V_{OS} Drift
 - 50pA Bias Current at 70 $^{\circ}$ C
 - Low Voltage Noise
- 10V/ μ s Min.
 1.3 μ s to 0.02%
 450 μ V Max.
 600 μ V Max.
 7 μ V/ $^{\circ}$ C Max.
 13nV/ $\sqrt{\text{Hz}}$ @ 1kHz
 26nV/ $\sqrt{\text{Hz}}$ @ 10Hz

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample and Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters

DESCRIPTION

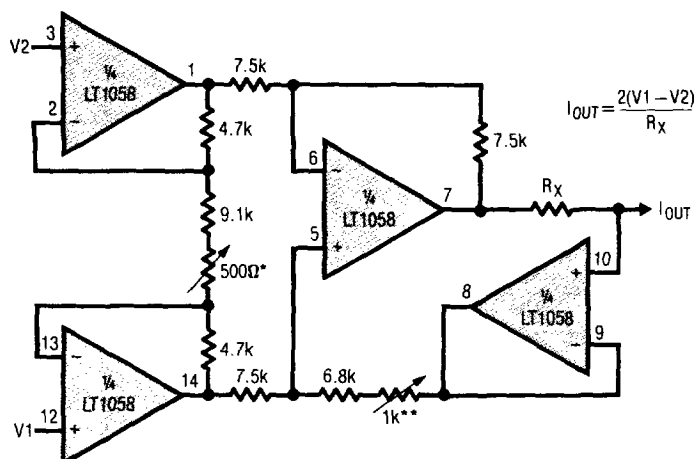
The LT1057 is a matched JFET input dual op amp in the industry standard 8 pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

The LT1058 is the lowest offset quad JFET input operational amplifier in the standard 14 pin configuration. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. It can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

Both the LT1057 and LT1058 are available in all standard packages: plastic and hermetic DIP and (LT1057 only) metal can.

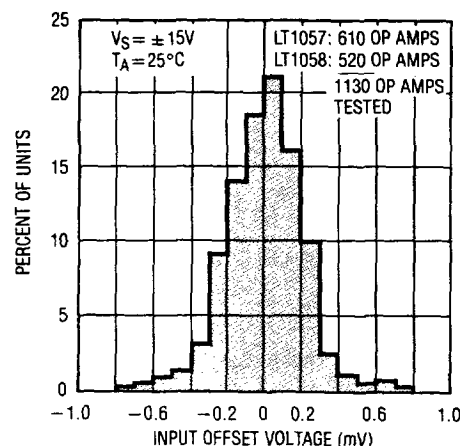
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**Current Output, High Speed, High Input Impedance
Instrumentation Amplifier**



*GAIN ADJUST
 **COMMON-MODE REJECTION ADJUST
 BANDWIDTH $\approx$ 2MHz

**Distribution of Offset Voltage
(All Packages, LT1057 and LT1058)**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 20V$
Differential Input Voltage	$\pm 40V$
Input Voltage	$\pm 20V$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1057AM/LT1057M/	
LT1058AM/LT1058M	$-55^{\circ}C$ to $125^{\circ}C$
LT1057AC/LT1057C/	
LT1058AC/LT1058C	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	
All Devices	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NO.
	LT1057AMH LT1057MH LT1057ACH LT1057CH
	LT1057AMJ8 LT1057MJ8 LT1057ACJ8 LT1057CJ8 LT1057ACN8 LT1057CN8
	LT1058AMJ LT1058MJ LT1058ACJ LT1058CJ LT1058ACN LT1058CN

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^{\circ}C$, $V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057 LT1058		150 180	450 600		200 250	800 1000	μV μV
I_{OS}	Input Offset Current	Fully Warm Up		3	40		4	50	pA
I_b	Input Bias Current	Fully Warm Up		± 5	± 50		± 7	± 75	pA
	Input Resistance-Differential			10^{12}			10^{12}		Ω
	-Common-Mode	$V_{CM} = -11V$ to $8V$ $V_{CM} = 8V$ to $11V$		10^{12} 10^{11}			10^{12} 10^{11}		Ω Ω
	Input Capacitance			4			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.0 2.4			2.1 2.5		μV_{p-p} μV_{p-p}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$ (Note 2)		26 13	22		28 14	24	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_0 = 10Hz$, 1kHz (Note 3)		1.5	4		1.8	6	$fA/\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$ $V_O = \pm 10V$, $R_L = 1k$	150 120	350 250		100 80	300 220		V/mV V/mV
	Input Voltage Range		± 10.5	14.3 -11.5		± 10.5	14.3 -11.5		V
CMRR	Common-Mode Rejection Ratio	LT1057 LT1058	86 84	100 98		82 80	98 96		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	103		86	102		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13		± 12	± 13		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate		10	14		8	13		V/ μs
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 5)	3.5	5		3	5		MHz
I_S	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AC LT1058AC			LT1057C LT1058C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057	●		250	800		330	1400	μV
		LT1058	●		300	1200		400	1800	μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057 H/J8 Package	●		1.8	7		2.3	12	$\mu V/^\circ C$
		N8 Package	●		3	10		4	16	$\mu V/^\circ C$
		LT1058 J Package (Note 4)	●		2.5	10		3	15	$\mu V/^\circ C$
		N Package (Note 4)	●		4	15		5	22	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$			18	150		20	250	pA
I_b	Input Bias Current	Warmed Up, $T_A = 70^\circ C$			± 50	± 250		± 60	± 350	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	70	220		50	200		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	102		84	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.8		± 12	± 12.8		V
I_S	Supply Current Per Amplifier	$T_A = 70^\circ C$	●			2.8			3.2	mA
					1.4			1.5		mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AM LT1058AM			LT1057M LT1058M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057	●		300	1100		400	2000	μV
		LT1058	●		380	1600		550	2500	μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057	●		2.0	7		2.5	12	$\mu V/^\circ C$
		LT1058 (Note 4)	●		2.5	10		3	15	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125^\circ C$			0.15	2		0.2	3	nA
I_b	Input Bias Current	Warmed Up, $T_A = 125^\circ C$			± 0.6	± 4.5		± 0.7	± 6	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120		30	110		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	86	100		83	98		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.7		± 12	± 12.6		V
I_S	Supply Current Per Amplifier	$T_A = 125^\circ C$			1.25	1.9		1.3	2.2	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; i.e., out of 100 LT1058s or (100 LT1057s), typically 240 op amps (or 120 for the LT1057) will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$$i_n = (2qI_b)^{1/2}$$

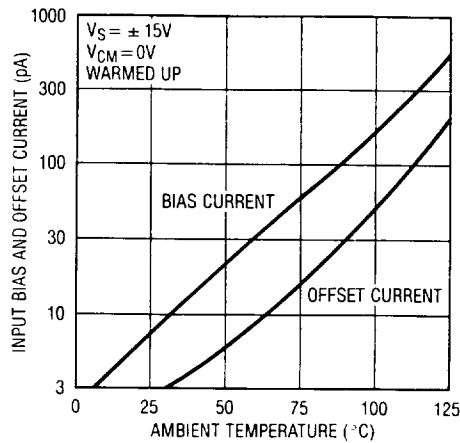
where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1G Ω swamps the contribution of current noise.

Note 4: This parameter is not 100% tested.

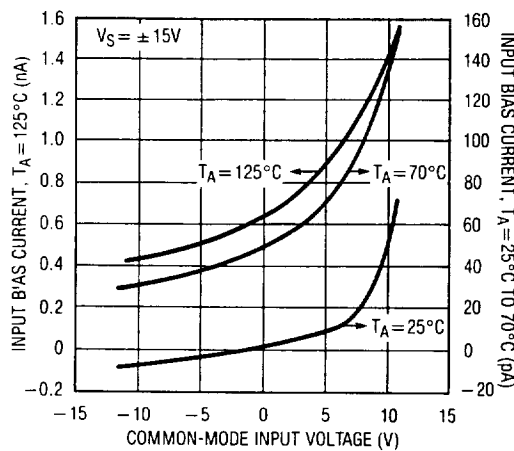
Note 5: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

TYPICAL PERFORMANCE CHARACTERISTICS

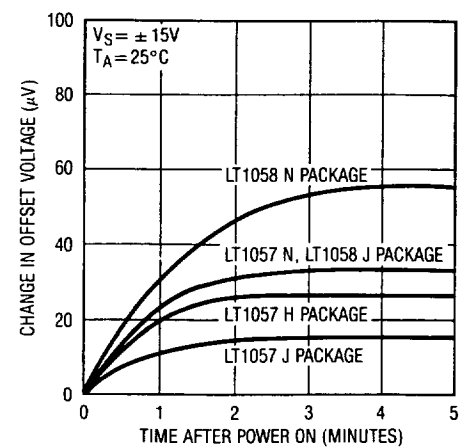
Input Bias and Offset Currents vs Temperature



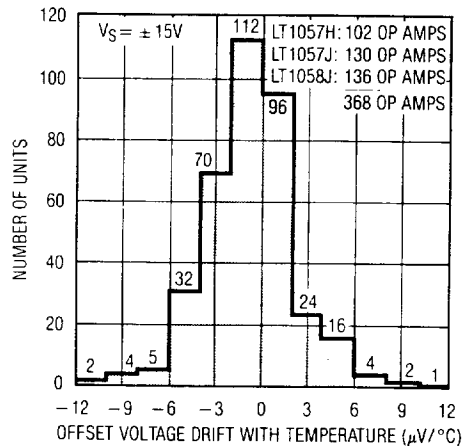
Input Bias Current Over the Common-Mode Range



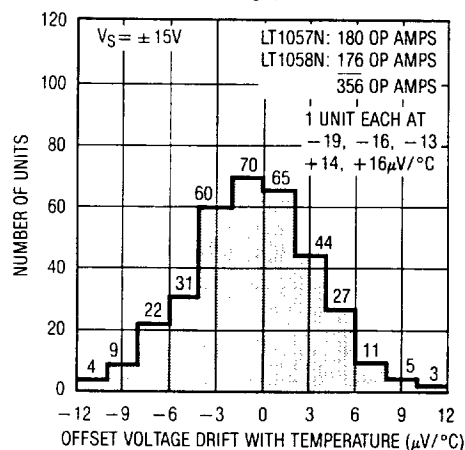
Warm-Up Drift



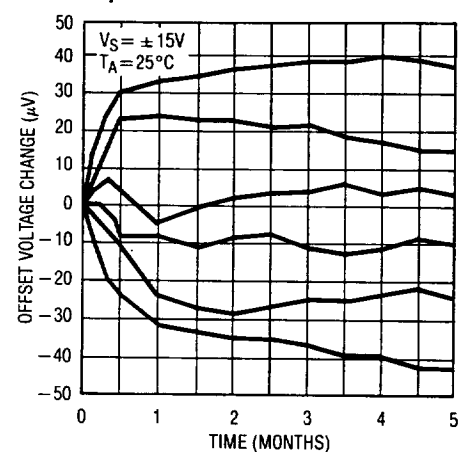
Distribution of Offset Voltage Drift with Temperature (H and J Package)



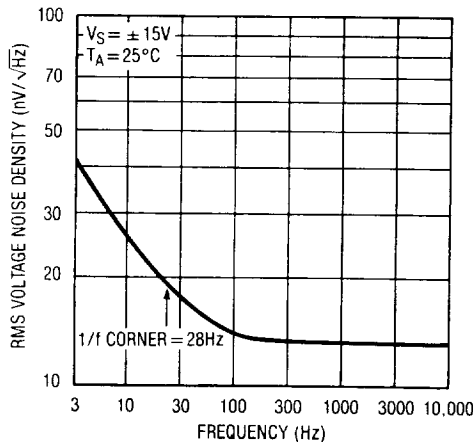
Distribution of Offset Voltage Drift with Temperature (Plastic N Package)



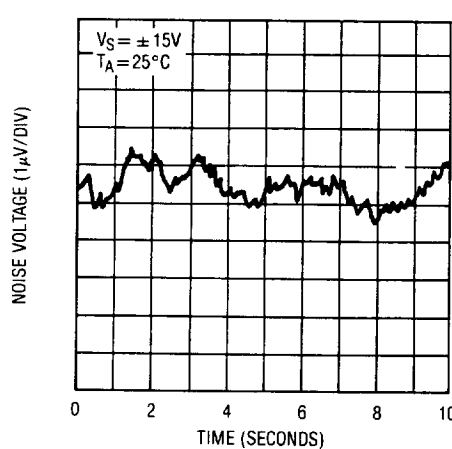
Long Term Drift of Representative Units



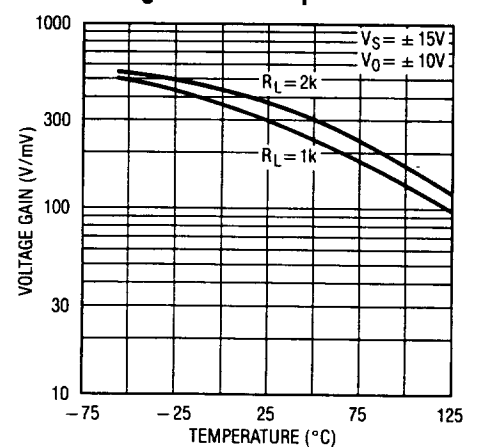
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise

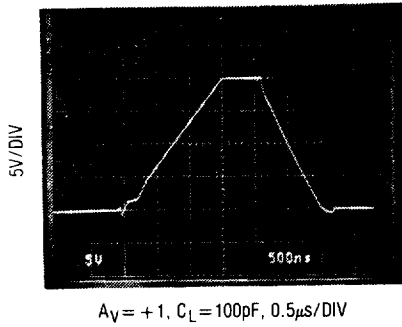


Voltage Gain vs Temperature

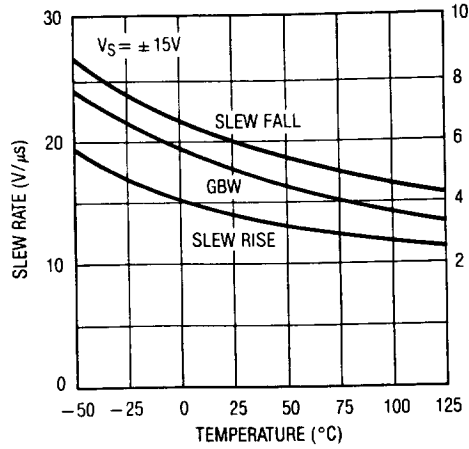


TYPICAL PERFORMANCE CHARACTERISTICS

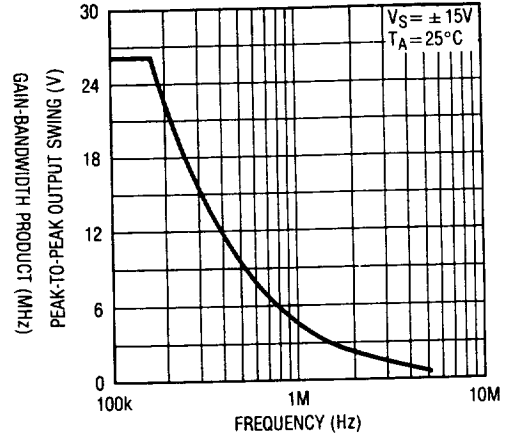
Large Signal Response



Slew Rate, Gain-Bandwidth Product vs Temperature

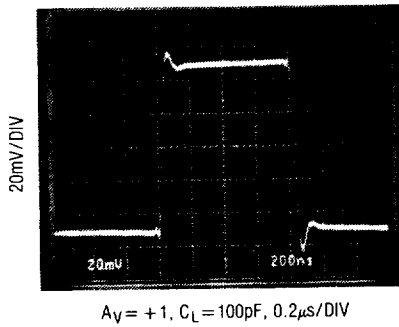


Undistorted Output Swing vs Frequency

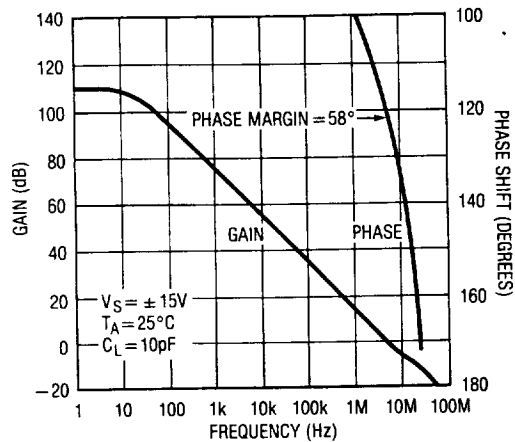


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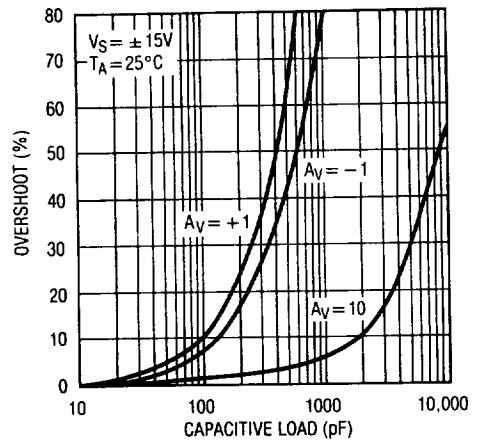
Small Signal Response



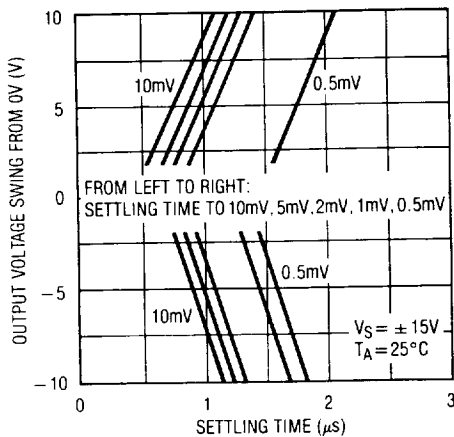
Gain, Phase Shift vs Frequency



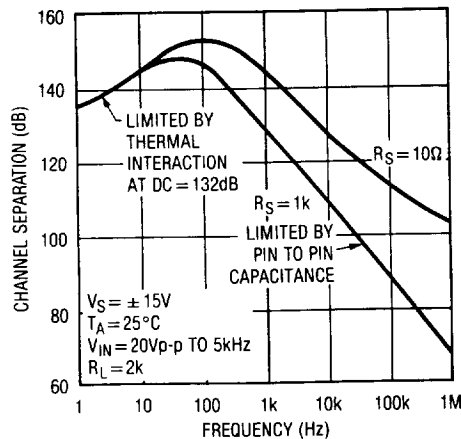
Capacitive Load Handling



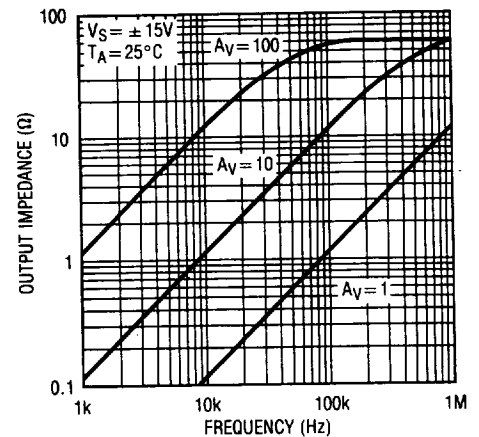
Settling Time



Channel Separation vs Frequency

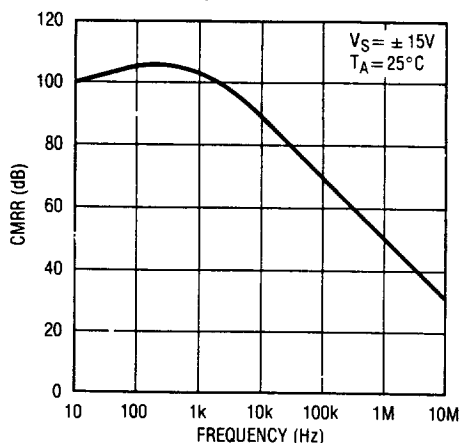


Output Impedance vs Frequency

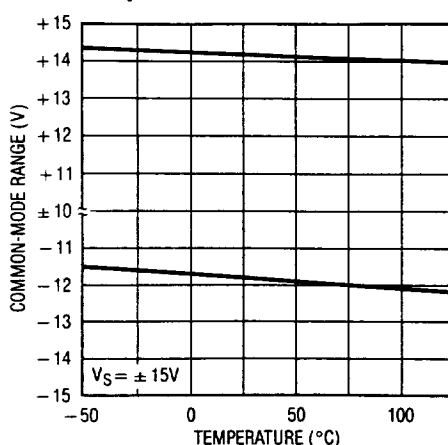


TYPICAL PERFORMANCE CHARACTERISTICS

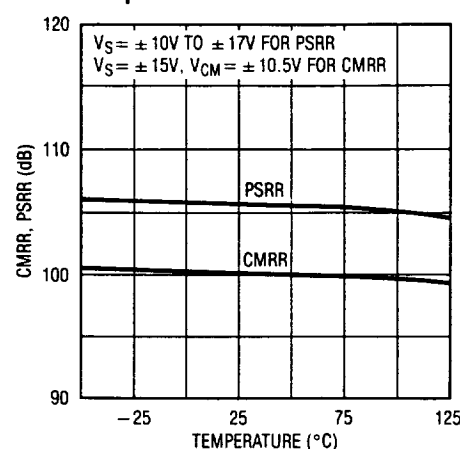
Common-Mode Rejection Ratio vs Frequency



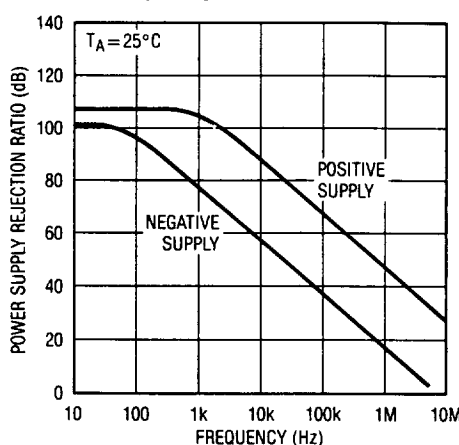
Common-Mode Range vs Temperature



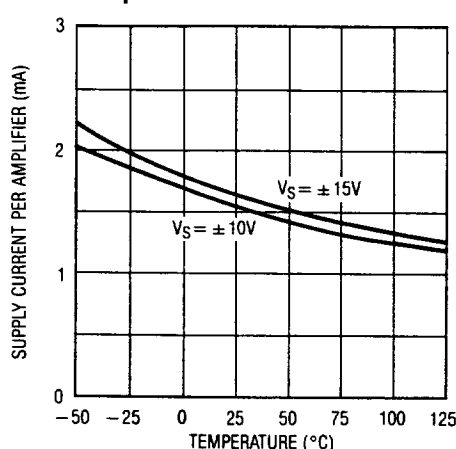
Common-Mode and Power Supply Rejections vs Temperature



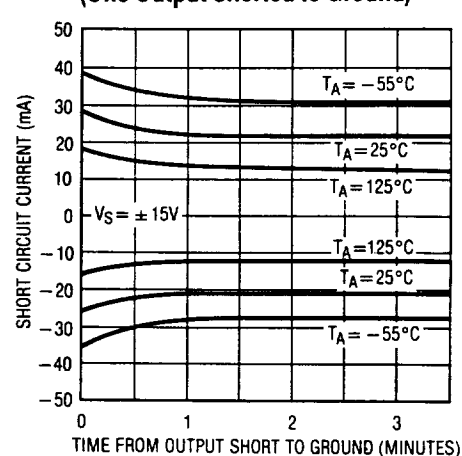
Power Supply Rejection Ratio vs Frequency



Supply Current vs Temperature



Short Circuit Current vs Time (One Output Shorted to Ground)



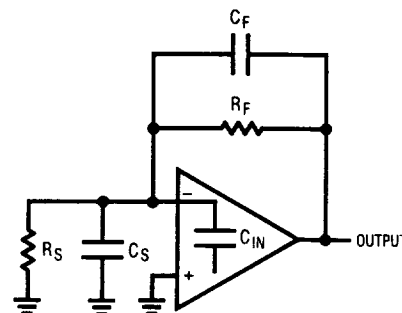
APPLICATIONS INFORMATION

The LT1057 may be inserted directly into LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074, TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F , the source resistance and capacitance (R_S , C_S), and the amplifier input capacitance ($C_{IN} \approx 4\text{pF}$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor

(C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Teflon™ is a trademark of DuPont.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical $40\mu\text{V}$ hysteresis ($50\mu\text{V}$ on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than $20\mu\text{V}$) hysteresis effect.

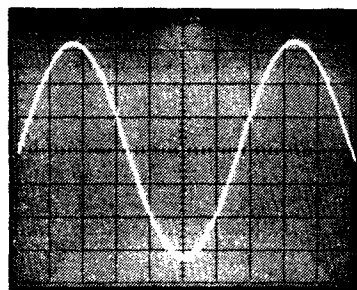
The offset voltage and drift performance are also affected by packaging. In the plastic N package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently, for best drift performance, as shown in the typical performance distribution plots, the J or H packages are recommended.

In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

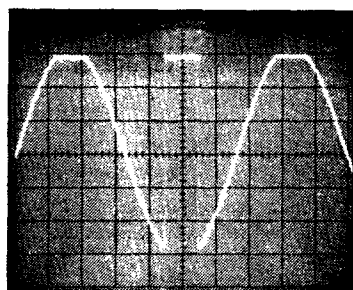
Phase Reversal Protection

Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., below -12V with $\pm 15\text{V}$ supplies). The photos show a $\pm 16\text{V}$ sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.

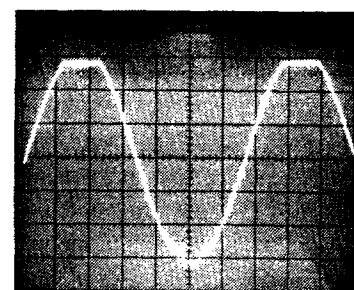


A

(A) $\pm 16\text{V}$ Sine Wave Input

B

(B) LF412A Output



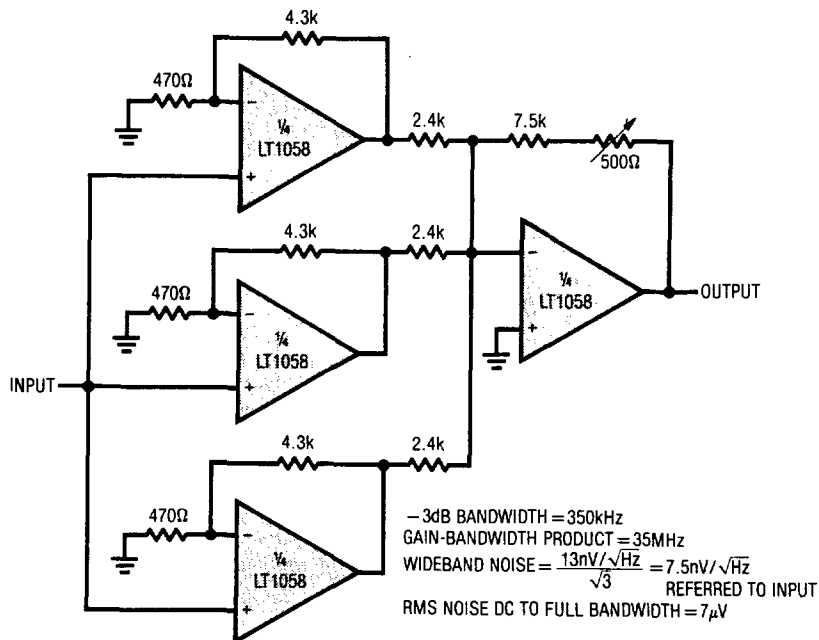
C

(C) LT1057/LT1058 Output

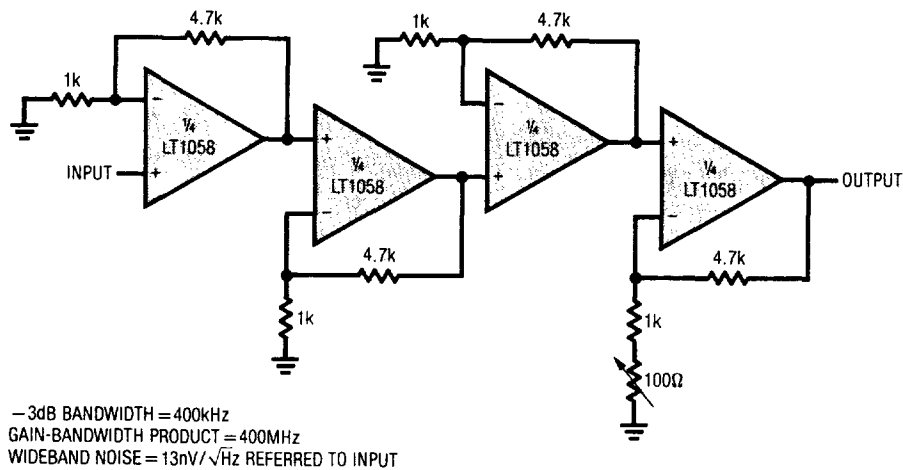
All Photos 5V/Div Vertical Scale, 50 μs /Div Horizontal Scale

APPLICATIONS

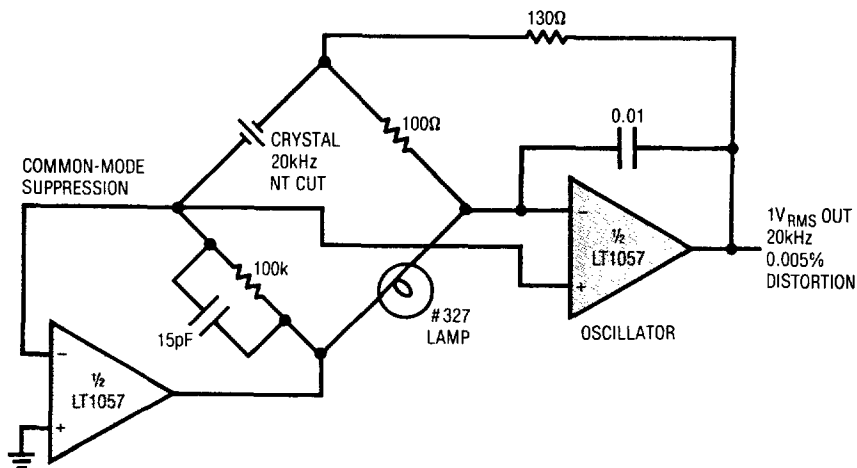
Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



Wideband, High Input Impedance, Gain = 1000 Amplifier



Low Distortion, Crystal Stabilized Oscillator



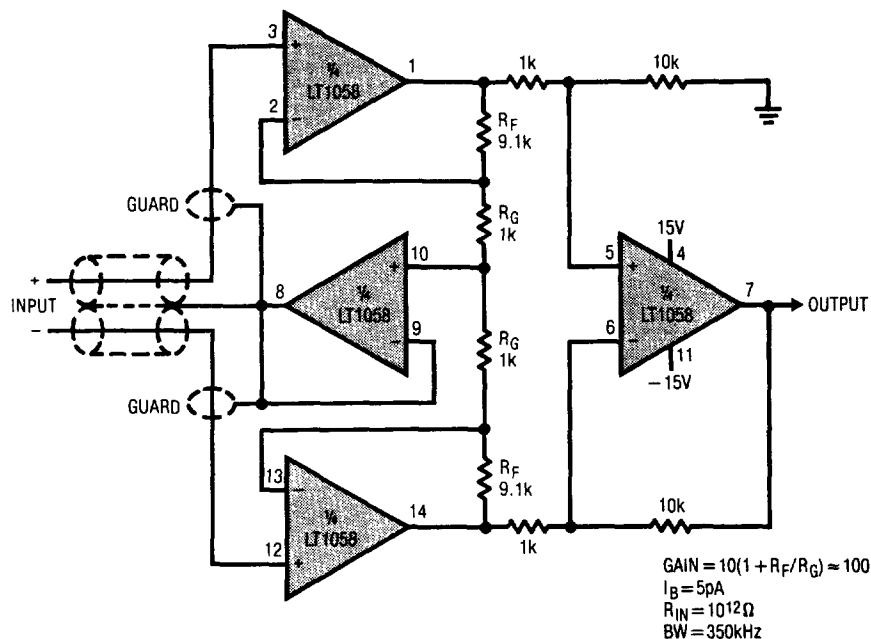
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The circuit diagram illustrates a precision current-to-voltage converter using two halves of the LT1057 operational amplifier. The first half (bottom) features a 2N2907 transistor at its non-inverting input, a 75k resistor and a 1μF capacitor at its inverting input, and a feedback network consisting of a 30pF capacitor and a 22k resistor. The second half (top) includes an LTC1043 switch at its non-inverting input, a 1k resistor and an LT1004 diode at its inverting input, and a feedback network with an 80.6k resistor, a 20k potentiometer, and a 1μF capacitor. The output is labeled $OUTPUT = \frac{A}{B}$.

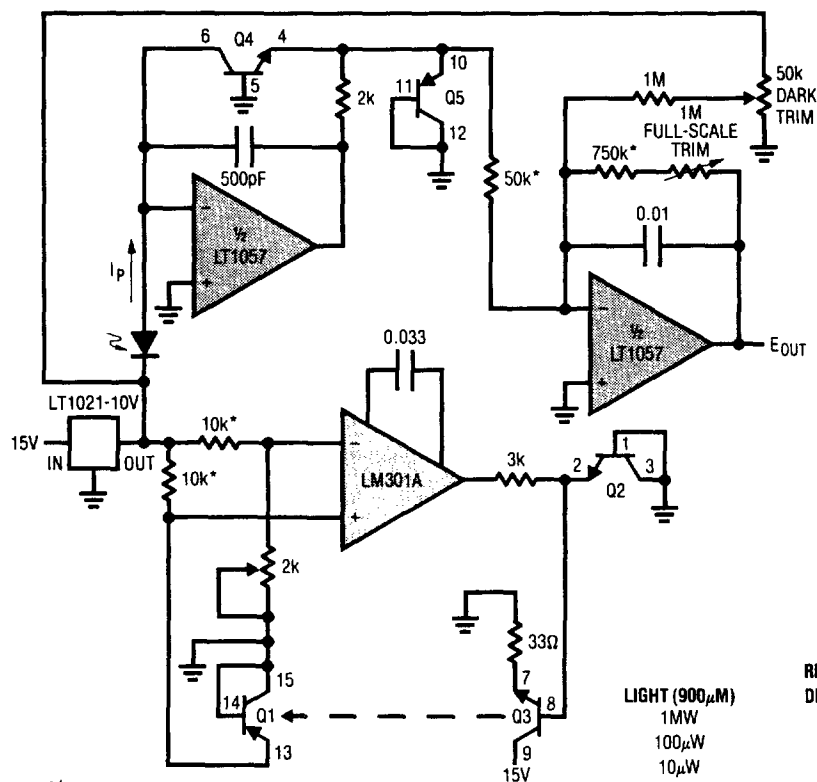
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APPLICATIONS

Instrumentation Amplifier with Shield Driver



100dB Range Logarithmic Photodiode Amplifier



$\text{HP-5082-4204 PIN PHOTODIODE.}$
 $Q1-Q5 = CA3096.$

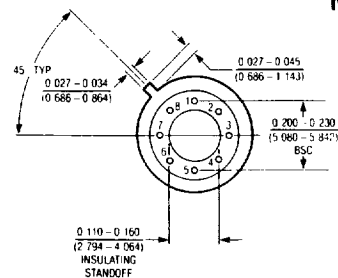
CONNECT SUBSTRATE OF CA3096
 ARRAY TO Q4'S EMITTER.
 *1% RESISTOR

100dB RANGE LOGARITHMIC PHOTODIODE AMPLIFIER

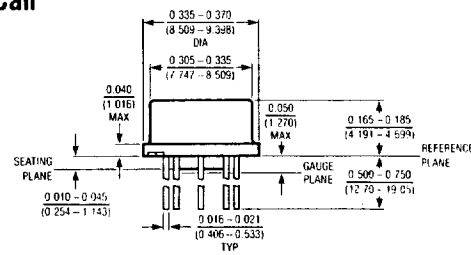
LIGHT (900μM)	RESPONSE DATA DIODE CURRENT	CIRCUIT OUTPUT
1mW	350μA	10.0V
100μW	35μA	7.85V
10μW	3.5μA	5.70V
1μW	350nA	3.55V
100nW	35nA	1.40V
10nW	3.5nA	-0.75V

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can

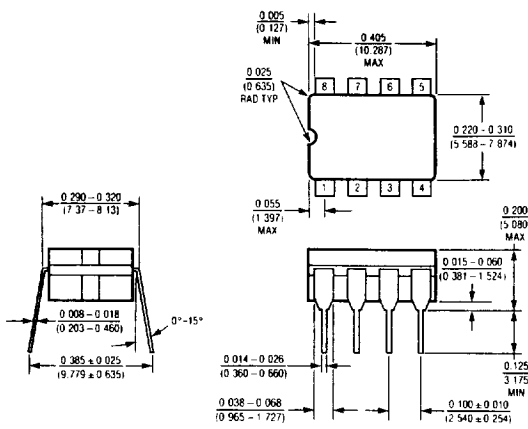


NOTE LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE



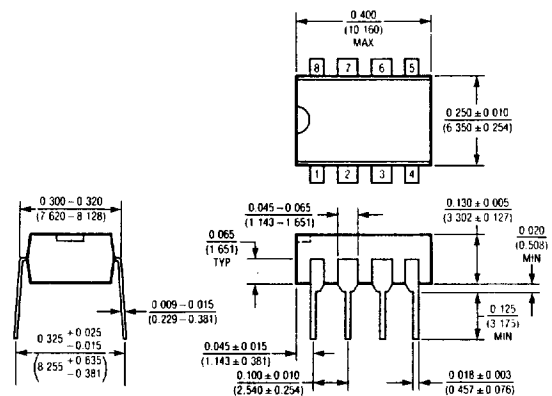
T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

J8 Package 8 Lead Hermetic Dip



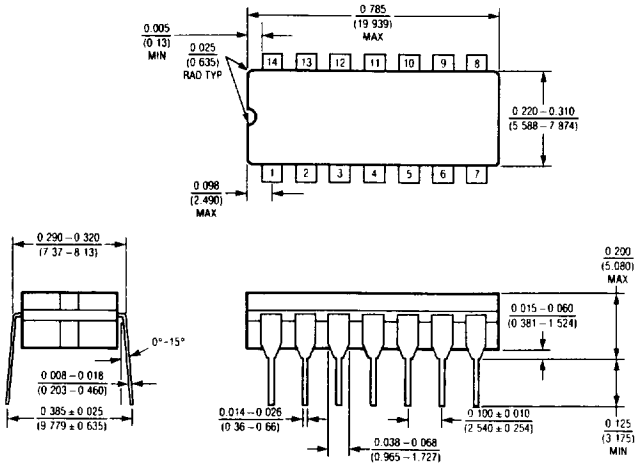
T_{jmax}	θ_{ja}
150°C	100°C/W

N8 Package 8 Lead Plastic



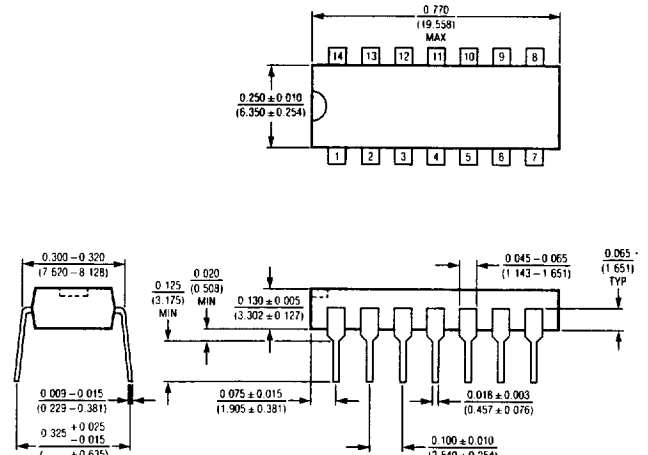
T_{jmax}	θ_{ja}
100°C	130°C/W

J Package 14-Lead Hermetic DIP



T_{jmax}	θ_{ja}
150°C	100°C/W

N Package 14-Lead Plastic



T_{jmax}	θ_{ja}
110°C	130°C/W