Programmable Touch Controller for Single Electrode Capacitance Sensors

Data Sheet **AD7148**

FEATURES

- Programmable capacitance-to-digital converter (CDC)
  - Femtofarad (fF) resolution
  - 8 capacitance sensor inputs
  - 25 ms update rate, all 8 sensor inputs
  - No external RC components required
  - Automatic conversion sequencer
- On-chip automatic calibration logic
  - Automatic compensation for environmental changes
  - Automatic adaptive threshold and sensitivity levels
  - Register map compatible with AD7143
- On-chip RAM to store calibration data
- I²C-compatible serial interface
- Separate V_{DRIVE} level for serial interface
- Interrupt output
- 16-lead, 4 mm × 4 mm LFCSP
- 2.6 V to 3.3 V supply voltage
- Low operating current
  - Full power mode: 1 mA
  - Low power mode: 21.5 µA

APPLICATIONS

- Cell phones
- Personal music and multimedia players
- Smart handheld devices
- Television, A/V, and remote controls
- Gaming consoles
- Digital still cameras

FUNCTIONAL BLOCK DIAGRAM

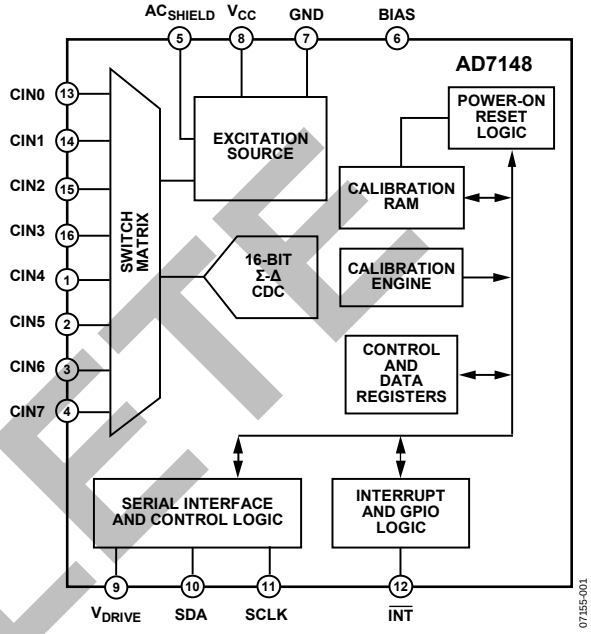


Figure 1.

GENERAL DESCRIPTION

The AD7148 is designed for use with capacitance sensors implementing functions such as buttons, scroll bars, and wheels. The sensors need only one PCB layer, enabling ultrathin applications.

The AD7148 is an integrated capacitance-to-digital converter (CDC) with on-chip environmental calibration. The CDC has eight inputs channeled through a switch matrix to a 16-bit, 250 kHz sigma-delta (Σ-Δ) converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. The external sensors can be arranged as a series of buttons, as a scroll bar or wheel, or as a combination of sensor types. By programming the registers, the user has full control over the CDC setup.

High resolution sensors require minimal software to run on the host processor.

The AD7148 is designed for single electrode capacitance sensors (grounded sensors). There is an active shield output to minimize noise pickup in the sensor. For floating, or two, electrode sensors, use the AD7143.

The AD7148 has on-chip calibration logic to compensate for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals as long as the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7148 has an I²C-compatible serial interface, as well as an interrupt output. There is a V_{DRIVE} pin to set the voltage level for the serial interface independent of V_{CC}.

The AD7148 is available in a 16-lead, 4 mm × 4 mm LFCSP and operates from a 2.6 V to 3.6 V supply. The operating current consumption in low power mode is typically 26 µA.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/15—Rev. A to Rev. B

Changes to Figure 4 ... 7
Updated Outline Dimensions ... 56
Changes to Ordering Guide ... 56

1/10—Rev. 0 to Rev. A

Changes to Figure 4 and Table 6 ... 7
Changes to BIAS Pin Section ... 11
Changes to Table 15 ... 28
Changes to Figure 45 ... 33
Added Exposed Pad Notation to Outline Dimensions ... 56

12/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE-TO-DIGITAL CONVERTER					
Update Rate	24.25	25	25.75	ms	8 conversion stages in sequencer; decimation rate = 256
Resolution		16		Bits	
CINx Input Range		±8		pF	
No Missing Codes	16			Bits	Guaranteed by design, not production tested
Total Unadjusted Error			±20	%	
Output Noise (Peak-to-Peak)		7		Codes	Decimation rate = 128
		3		Codes	Decimation rate = 256
Output Noise (RMS)		0.8		Codes	Decimation rate = 128
		0.5		Codes	Decimation rate = 256
C_{STRAY} Offset Range		±20		pF	6-bit DAC
C_{STRAY} Offset Resolution		0.32		pF	
Low Power Mode Delay Accuracy			4	%	% of 200 ms, 400 ms, 600 ms, or 800 ms
EXCITATION SOURCE					
Frequency		250		kHz	
Output Voltage	0		V_{CC}	V	Oscillating
AC_{SHIELD}					
Short-Circuit Source Current		10		mA	
Short-Circuit Sink Current		10		mA	
Maximum Output Load			150	pF	Capacitance load on AC_{SHIELD} to ground
LOGIC INPUTS (SCLK, SDA,)					
Input High Voltage, V_{IH}	0.7 × V_{DRIVE}			V	
Input Low Voltage, V_{IL}			0.4	V	
Input High Voltage, I_{IH}	−1			µA	V_{IN} = V_{DRIVE}
Input Low Voltage, I_{IL}			1	µA	V_{IN} = GND
Hysteresis		150		mV	
OPEN-DRAIN OUTPUTS (SCLK, SDA, $\overline{INT}$)					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = −1 mA
Output High Leakage Current, I_{OH}		+0.1	±1	µA	V_{OUT} = V_{DRIVE}
POWER					
V_{CC}	2.6	3.3	3.6	V	
V_{DRIVE}	1.65		3.6	V	Serial interface operating voltage
I_{CC}		0.9	1	mA	In full power mode, V_{CC} + V_{DRIVE}
		15.5	21.5	µA	Low power mode, converter idle, V_{CC} + V_{DRIVE}
		2.3	7.5	µA	Full shutdown, V_{CC} + V_{DRIVE}

TYPICAL AVERAGE CURRENT IN LOW POWER MODE

V_{CC} = 3.6 V, T = 25°C, load of 50 pF, unless otherwise noted.

Table 2.

		Current Values of Conversion Stages (µA)							
Low Power Mode Delay	**Decimation Rate**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
200 ms	64	20.83	24.18	27.52	30.82	34.11	37.37	40.6	43.81
	128	25.3	31.92	38.45	44.87	51.21	57.45	63.6	69.66
	256	34.11	46.99	59.51	71.66	83.47	94.94	106.1	116.96
400 ms	64	18.17	19.86	21.55	23.23	24.9	26.57	28.23	29.88
	128	20.43	23.79	27.12	30.43	33.72	36.98	40.22	43.43
	256	24.9	31.53	38.06	44.5	50.83	57.08	63.23	69.3
600 ms	64	17.28	18.41	19.54	20.67	21.79	22.91	24.03	25.14
	128	18.79	21.04	23.28	25.51	27.73	29.94	32.13	34.32
	256	21.79	26.25	30.67	35.04	39.37	43.66	47.9	52.11
800 ms	64	16.84	17.69	18.53	19.38	20.23	21.07	21.91	22.75
	128	17.97	19.66	21.35	23.03	24.7	26.37	28.03	29.69
	256	20.23	23.59	26.93	30.24	33.53	36.79	40.03	43.24

MAXIMUM AVERAGE CURRENT IN LOW POWER MODE

V_{CC} = 3.6 V, load of 50 pF, unless otherwise noted.

Table 3.

		Current Values of Conversion Stages (µA)							
Low Power Mode Delay	**Decimation Rate**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
200 ms	64	27.71	31.65	35.56	39.44	43.28	47.1	50.89	54.64
	128	32.96	40.72	48.37	55.89	63.3	70.59	77.77	84.84
	256	43.28	58.37	72.99	87.17	100.92	114.26	127.22	139.8
400 ms	64	24.61	26.6	28.58	30.55	32.51	34.47	36.42	38.36
	128	27.26	31.21	35.12	39	42.85	46.67	50.46	54.22
	256	32.51	40.29	47.94	55.47	62.88	70.18	77.36	84.44
600 ms	64	23.58	24.91	26.23	27.55	28.87	30.18	31.5	32.8
	128	25.35	27.99	30.62	33.24	35.84	38.43	41	43.56
	256	28.87	34.11	39.29	44.41	49.48	54.5	59.46	64.38
800 ms	64	23.06	24.06	25.05	26.05	27.04	28.03	29.02	30
	128	24.39	26.38	28.36	30.33	32.29	34.25	36.2	38.14
	256	27.04	30.98	34.9	38.78	42.64	46.46	50.25	54.01

I²C TIMING SPECIFICATIONS (AD7148-1)

T_A = −40°C to +85°C, V_{DRIVE} = 1.65 V to 3.6 V, V_{CC} = 2.6 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals timed from a voltage level of 1.6 V.

Table 4.

Parameter[1]	Limit	Unit	Description
f_{SCLK}	400	kHz max	
t_1	0.6	µs min	Start condition hold time, $t_{HD; STA}$
t_2	1.3	µs min	Clock low period, t_{LOW}
t_3	0.6	µs min	Clock high period, t_{HIGH}
t_4	100	ns min	Data setup time, $t_{SU; DAT}$
t_5	300	ns min	Data hold time, $t_{HD; DAT}$
t_6	0.6	µs min	Stop condition setup time, $t_{SU; STO}$
t_7	0.6	µs min	Start condition setup time, $t_{SU; STA}$
t_8	1.3	µs min	Bus free time between stop and start conditions, t_{BUF}
t_R	300	ns max	Clock/data rise time
t_F	300	ns max	Clock/data fall time

[1] Guaranteed by design, not production tested.

I²C Timing Diagram

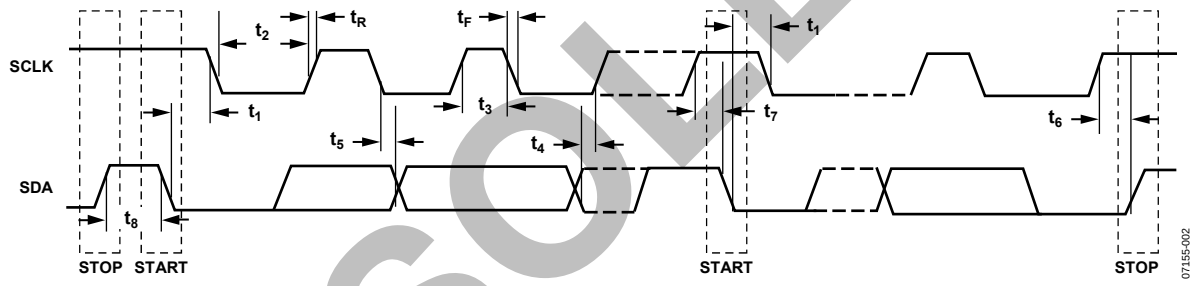


Figure 2. I²C Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{CC} to GND	−0.3 V to +3.6 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating (Human Body Model)	2.5 kV
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP	
Power Dissipation	450 mW
θ_{JA} Thermal Impedance	135.7°C/W
IR Reflow Peak Temperature	260°C ± 0.5°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

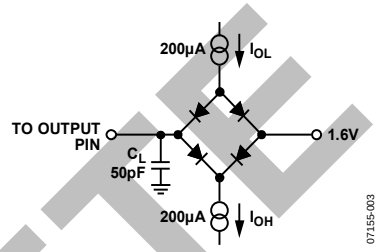
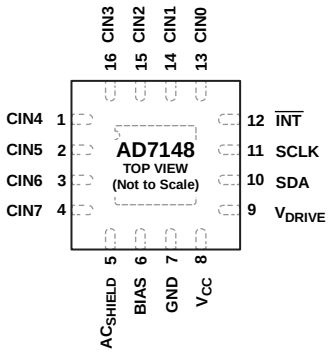


Figure 3. Load Circuit for Digital Output Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINT AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

07155-004

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CIN4	Capacitance Sensor Input.
2	CIN5	Capacitance Sensor Input.
3	CIN6	Capacitance Sensor Input.
4	CIN7	Capacitance Sensor Input.
5	AC_{SHIELD}	CDC Active Shield Output. Connect to external shield.
6	BIAS	Bias Node for Internal Circuitry. Requires 100 nF capacitor to ground.
7	GND	Ground Reference Point for All Circuitry.
8	V_{CC}	Supply Voltage.
9	V_{DRIVE}	Serial Interface Operating Voltage Supply.
10	SDA	I^2C Serial Data Input/Output. SDA requires pull-up resistor.
11	SCLK	Clock Input for Serial Interface.
12	$\overline{INT}$	General-Purpose Open-Drain Interrupt Output. Programmable polarity; requires pull-up resistor.
13	CIN0	Capacitance Sensor Input.
14	CIN1	Capacitance Sensor Input.
15	CIN2	Capacitance Sensor Input.
16	CIN3	Capacitance Sensor Input.
17	EPAD	The exposed pad is not connected internally. For increased reliability of the solder joint and maximum thermal capability, it is recommended that the pad be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

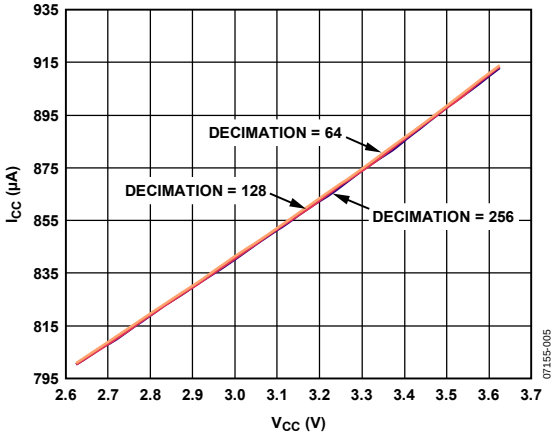


Figure 5. Supply Current vs. Supply Voltage

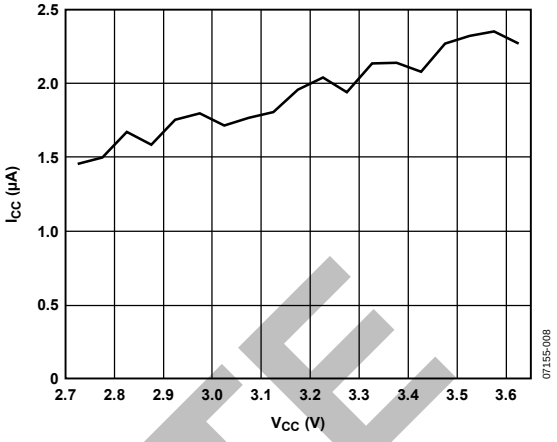


Figure 8. Shutdown Supply Current vs. Supply Voltage

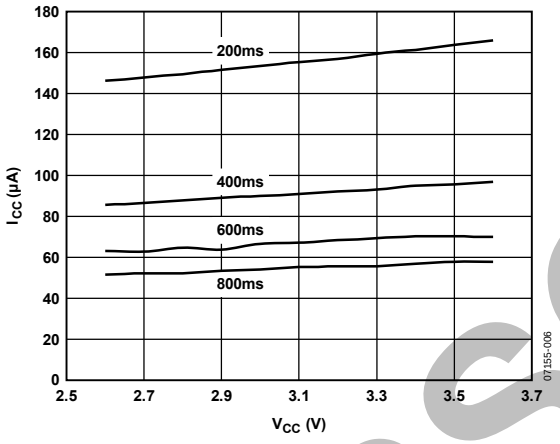


Figure 6. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 256

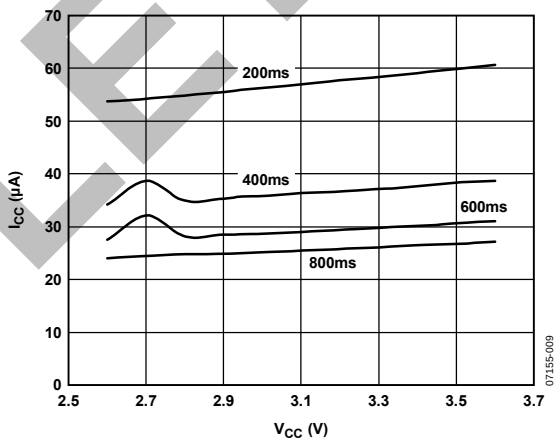


Figure 9. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 64

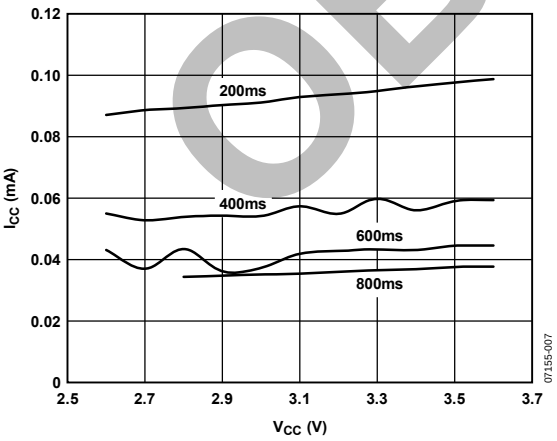


Figure 7. Low Power Supply Current vs. Supply Voltage Decimation Rate = 128

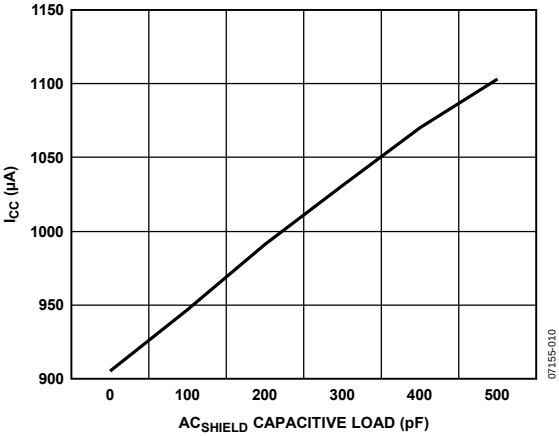


Figure 10. Supply Current vs. Capacitive Load on CIN

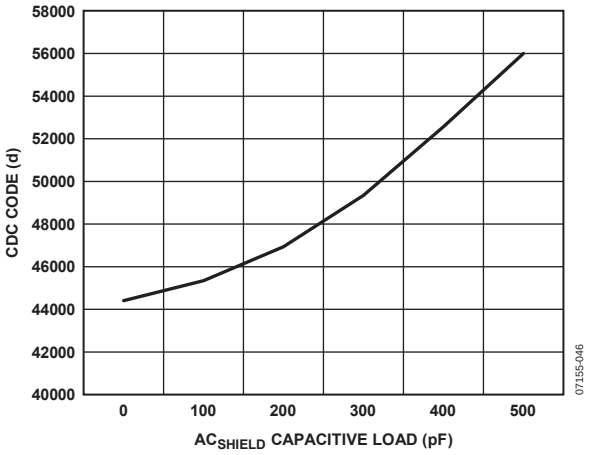


Figure 11. CDC Output Code vs. Capacitive Load on AC_{SHIELD}

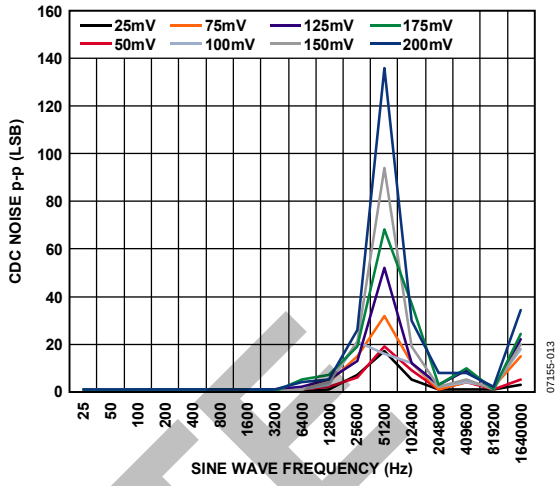


Figure 14. Power Supply Sine Wave Rejection, V_{CC} = 3.6 V

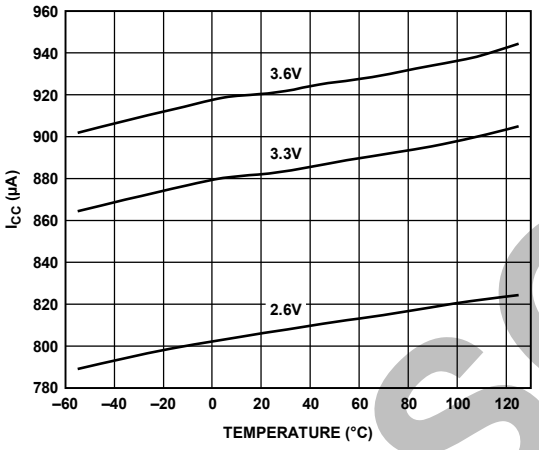


Figure 12. Supply Current vs. Temperature

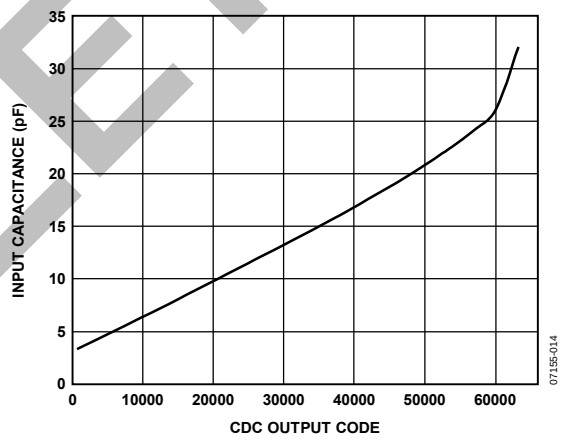


Figure 15. CDC Linearity, V_{CC} = 3.3 V

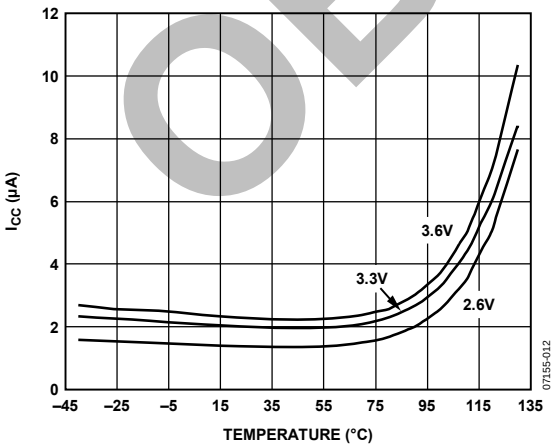


Figure 13. Shutdown Supply Current vs. Temperature

THEORY OF OPERATION

The AD7148 is a capacitance-to-digital converter (CDC) with on-chip environmental compensation, intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit, Σ-Δ converter that converts a capacitive input signal into a digital value. There are eight input pins on the AD7148: CIN0 to CIN7. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7148 has an I^2C interface, ensuring that the part is compatible with a wide range of host processors.

The AD7148 interfaces with up to eight external capacitance sensors. These sensors can be arranged as buttons, scroll bars, wheels, or as a combination of sensor types. The external sensors consist of an electrode on a single or multiple layer PCB that interfaces directly to the AD7148.

The AD7148 can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is an on-chip sequencer to control how each of the capacitance inputs is polled.

The AD7148 has on-chip digital logic and 528 words of RAM that are used for environmental compensation. The effects of humidity, temperature, and other environmental factors can affect the operation of capacitance sensors. Transparent to the user, the AD7148 performs continuous calibration to compensate for these effects, allowing the AD7148 to give error-free results at all times.

The AD7148 requires minimal companion software that runs on the host or other microcontroller to implement high resolution sensor functions, such as scroll bars or wheels. However, no companion software is required to implement buttons. Button sensors are implemented on chip, entirely in digital logic.

The AD7148 can be programmed to operate in either full power mode or low power, automatic wake-up mode. The automatic wake-up mode is particularly suited for portable devices that require low power operation, providing the user with significant power savings and full functionality.

The AD7148 has an interrupt output, $\overline{\text{INT}}$, to indicate when new data has been placed into the registers. $\overline{\text{INT}}$ is used to interrupt the host on sensor activation. The AD7148 operates from a 2.6 V to 3.6 V supply and is available in a 16-lead, 4 mm × 4 mm LFCSP.

CAPACITANCE SENSING THEORY

The AD7148 measures capacitance changes from sensors where one plate is connected to ground. The sensor electrode on the PCB makes up one plate of a virtual capacitor. The other plate of the capacitor is the user's finger, which is grounded with respect to the sensor input.

The AD7148 first outputs an excitation signal to charge the plate of the capacitor. When the user comes close to the sensor, the virtual capacitor is formed, with the user acting as the second capacitor plate.

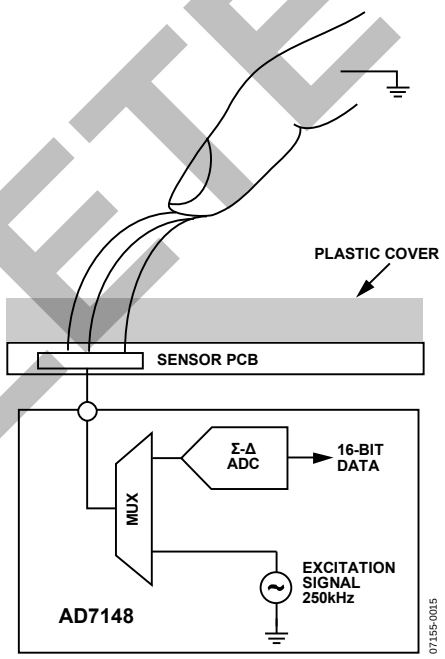


Figure 16. Capacitance Sensing Method

A square wave excitation signal is applied to the CINx input during the conversion, and the modulator continuously samples the charge going through the CINx pin. The output of the modulator is processed via a digital filter, and the resulting digital data is stored in the CDC_RESULT_Sx registers for each conversion stage, located at Address 0x00B to Address 0x012.

Registering a Sensor Activation

When a user approaches a sensor, the total capacitance associated with that sensor changes and is measured by the AD7148. When the capacitance changes to such an extent that a set threshold is exceeded, the AD7148 registers this as a sensor activation.

On-chip threshold limits are used to determine when sensor activation occurs. Figure 17 shows the change in CDC_RESULT_Sx that occurs when a user activates a sensor. The sensor is deemed to be active only when the value of CDC_RESULT_Sx is either greater than the value of STAGEx_HIGH_THRESHOLD or less than the value of STAGEx_LOW_THRESHOLD.

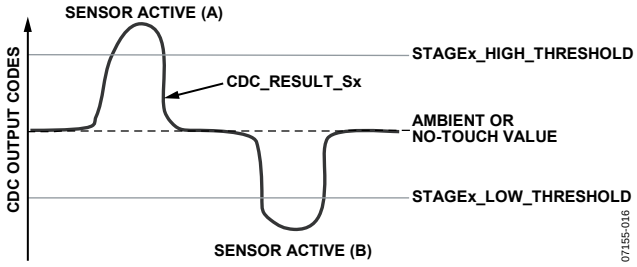


Figure 17. Sensor Activation Thresholds

In Figure 17, two different sensor activations are shown. Sensor Activate (A) occurs when a sensor is connected to the positive input of the converter. In this case, when a user activates the sensor, there is an increase in the CDC code, and the value of CDC_RESULT_Sx exceeds the value of STAGEx_HIGH_THRESHOLD. Sensor Active (B) occurs when the sensor is connected to the negative input of the converter. In this case, when a user activates the sensor, there is a decrease in the CDC code, and the value of CDC_RESULT_Sx becomes less than the value of STAGEx_LOW_THRESHOLD.

For each conversion stage, the STAGEx_HIGH_THRESHOLD and the STAGEx_LOW_THRESHOLD registers are in Register Bank 3. The values in these registers are updated automatically by the AD7148 due to its environmental calibration and adaptive threshold logic.

At power-up, the values in the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD registers are the same as those in the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers in Register Bank 2. The user must program the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers on device power-up. See the Environmental Calibration section for more information.

Complete Solution for Capacitance Sensing

Analog Devices, Inc., provides a complete solution for capacitance sensing. The two main elements of the solution are the sensor PCB and the AD7148.

If the application requires high resolution sensors such as scroll bars or wheels, software is required that runs on the host processor. No position algorithm is required for button sensors.

The memory requirements for the host depend on the sensor and are typically 10 kB of code and 600 bytes of data memory, depending on the sensor type.

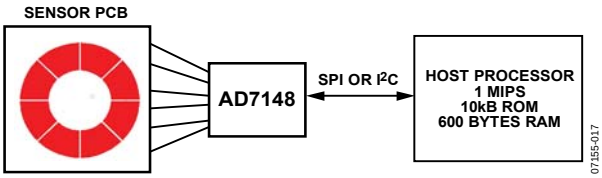


Figure 18. Three-Part Capacitance Sensing Solution

Analog Devices supplies the sensor PCB footprint design libraries to the customer and supplies any necessary software on an open-source basis.

BIAS PIN

The BIAS pin (Pin 6) is connected internally to the bias node in the AD7148. To ensure correct operation of the AD7148, connect a 100 nF capacitor between the BIAS pin and ground. The voltage at the BIAS pin is $V_{CC}/2$.

OPERATING MODES

The AD7148 has three operating modes. Full power mode, in which the device is always fully powered, is suited for applications where power is not a concern (for example, game consoles that have an ac power supply). Low power mode, in which the part automatically powers down, is tailored to give significant power savings over full power mode and is suited for mobile applications where power must be conserved. In shutdown mode, the part shuts down completely.

The POWER_MODE bits of the PWR_CONTROL register (Address 0x000[1:0]) set the operating mode on the AD7148. Table 7 shows the POWER_MODE settings for each operating mode. To put the AD7148 into shutdown mode, set the POWER_MODE bits to either 01 or 11.

Table 7. POWER_MODE Settings

POWER_MODE Bits	Operating Mode
00	Full power mode
01	Shutdown mode
10	Low power mode
11	Shutdown mode

The power-on default setting of the POWER_MODE bits is 00, full power mode.

Full Power Mode

In full power mode, all sections of the AD7148 remain fully powered and converting at all times. While a sensor is being touched, the AD7148 processes the sensor data. If no sensor is touched, the AD7148 measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7148 converts at a constant rate. See the CDC Conversion Sequence Time section for more information.

Low Power Mode

When in low power mode, the POWER_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7148 reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a reduced power state while the sensors are not touched. After a delay defined by the LP_CONV_DELAY bits (200 ms, 400 ms, 600 ms or 800 ms), the AD7148 performs a conversion and uses this data to update the compensation logic.

When an external sensor is touched, the AD7148 begins a conversion sequence every 25 ms to read back data from the sensors.

In low power mode, total current consumption is an average of the current used during a conversion and the current used while the AD7148 is waiting for the next conversion to begin. For example, when LP_CONV_DELAY is 400 ms, the AD7148 typically uses 0.85 mA current for 25 ms and 14 µA for 400 ms during the conversion interval. Note that these conversion timings can be altered through the register settings. See the CDC Conversion Sequence Time section for more information.

The time required for the AD7148 to transition from a full power state to a reduced power state after the user stops touching the external sensors is configurable. The PWR_DOWN_TIMEOUT bits in the AMB_COMP_CTRL0 register (Address 0x002[13:12]) control the time delay before the AD7148 transitions to the reduced power state after the user stops touching the sensors.

Low Latency from Touch to Response

In low power mode, the AD7148 remains in a low power state until proximity is detected on any one of the external sensors. When proximity is detected, the AD7148 is automatically configured into the full power mode operation, thus converting each sequence every 36 ms. Using this method, the latency delay is minimized because the AD7148 is operating in full power mode by the time the user physically makes contact with a sensor.

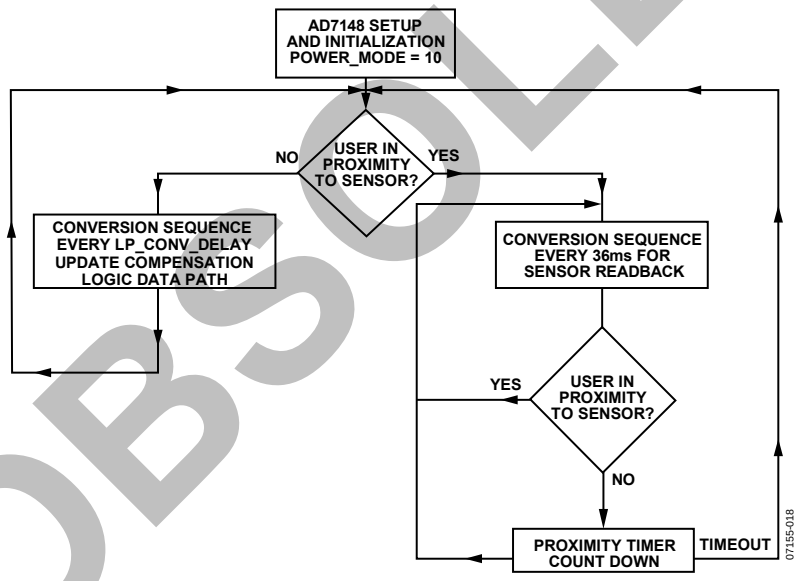


Figure 19. Low Power Mode Operation

CAPACITANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7148 has a Σ-Δ architecture with 16-bit resolution. There are eight possible inputs to the CDC that are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 250 kHz.

OVERSAMPLING THE CDC OUTPUT

The decimation rate, or oversampling ratio, is determined by the DECIMATION bits of the PWR_CONTROL register (Address 0x000[9:8]), as listed in Table 8.

Table 8. CDC Decimation Rate

DECIMATION Bits	Decimation Rate	CDC Output Rate per Stage (ms)
00	256	3.072
01	128	1.536
10	64	0.768
11	64	0.768

The decimation process on the AD7148 is an averaging process, during which a number of samples are taken, and the averaged result is output. Due to the architecture of the digital filter used, the number of samples taken (per stage) is equal to 3× the decimation rate. That is, 3 × 256 samples or 3 × 128 samples are averaged to obtain each stage result.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the output rate per stage; thus, a trade-off is possible between a noise-free signal and speed of sampling.

CAPACITANCE SENSOR OFFSET CONTROL

There are two programmable DACs on board the AD7148 to null the effect of any stray capacitances on the CDC measurement. These offsets are due to stray capacitance to ground. Best practice is to ensure that the CDC output for any stage is approximately equal to midscale (~32,700) when no sensor is active.

The simplified block diagram in Figure 20 shows how to apply the STAGEx_OFFSET registers to null the offsets. The 6-bit POS_AFE_OFFSET and NEG_AFE_OFFSET bits program the offset DAC to provide 0.32 pF resolution offset adjustment over a range of 20 pF. Apply the positive and negative offsets to either the positive or the negative CDC input using the NEG_AFE_OFFSET and POS_AFE_OFFSET bits.

This process is required only once during the initial capacitance sensor characterization.

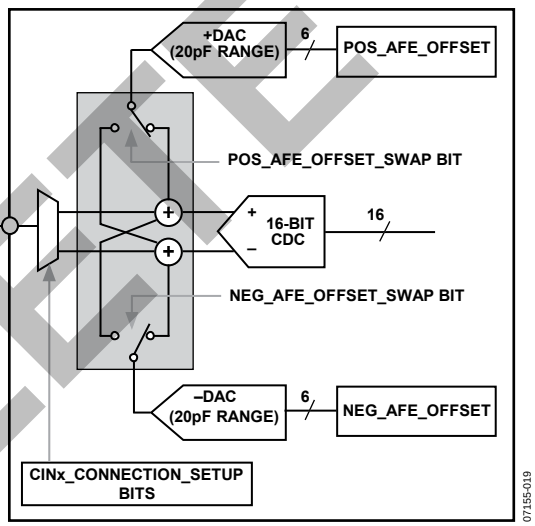


Figure 20. Analog Front-End Offset Control

CONVERSION SEQUENCER

The AD7148 has an on-chip sequencer to implement conversion control for the input channels. Up to eight conversion stages can be performed in one sequence. Each of the eight conversion stages can measure the input from a different sensor. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a slider sensor can be assigned to STAGE0 through STAGE7, or a button sensor can be assigned to STAGE0. For each conversion stage, the input mux that connects the CINx inputs to the converter can have a unique setting.

The AD7148 on-chip sequence controller provides conversion control, beginning with STAGE0. Figure 21 shows a block diagram of the CDC conversion stages and CINx inputs. A conversion sequence is defined as a sequence of CDC conversions starting at STAGE0 and ending at the stage determined by the value that is programmed using the SEQUENCE_STAGE_NUM bits in the PWR_CONTROL register (Address 0x000[7:4]). Depending on the number and type of capacitance sensors that are used, not all conversion stages are required. Use the SEQUENCE_STAGE_NUM bits to set the number of conversions in one sequence, depending on the sensor interface requirements. For example, these bits are set to 0005 if the CINx inputs are mapped to only six stages. In addition, set the STAGEx_CAL_EN register according to the number of stages that are used.

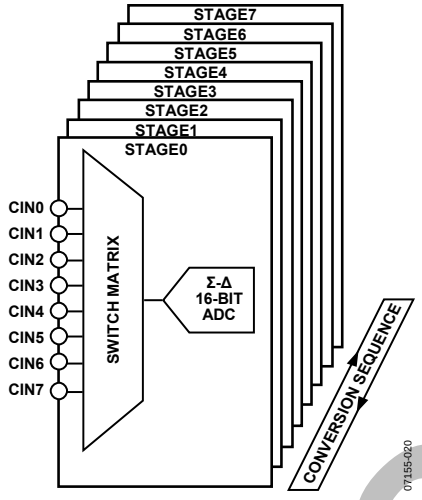


Figure 21. CDC Conversion Stages

The number of required conversion stages depends completely on the number of sensors attached to the AD7148. Figure 22 shows how many conversion stages are required for each sensor and how many inputs to the AD7148 each sensor requires.

A button sensor generally requires one sequencer stage; however, it is possible to configure two button sensors to operate differentially. Only one button from the pair can be activated at a time; pressing both buttons together results in neither button being activated. This configuration requires one conversion stage (see Figure 22, B2 and B3).

A wheel sensor requires eight stages, and a slider requires two stages. The result from each stage is used by the host software to determine user position on the slider or wheel. The algorithms that perform this process are available from Analog Devices, free of charge, on signing a software license.

CDC CONVERSION SEQUENCE TIME

The time required for one complete measurement for all eight stages by the CDC is defined as the CDC conversion sequence time. The SEQUENCE_STAGE_NUM and DECIMATION bits determine the conversion time, as shown in Table 9.

For example, while operating with a decimation rate of 128, if the SEQUENCE_STAGE_NUM bits are set to 0005 for the conversion of six stages in a sequence, the conversion sequence time is 9.216 ms.

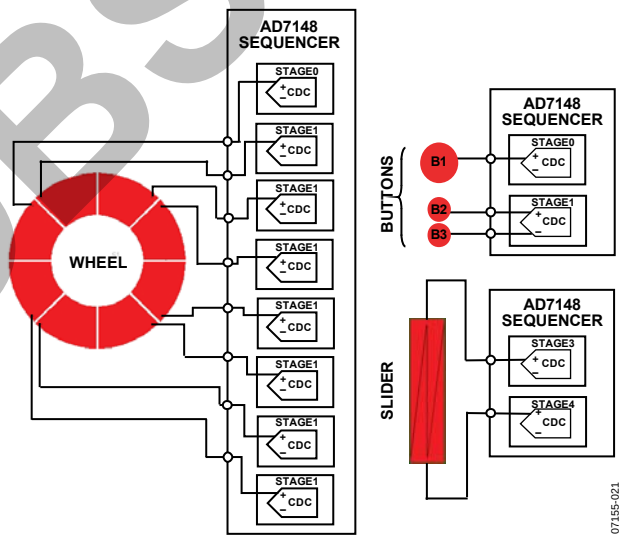


Figure 22. Sequencer Setup for Sensors

Table 9. CDC Conversion Times for Full Power Mode

	Conversion Time (ms)		
SEQUENCE_STAGE_NUM	Decimation = 64	Decimation = 128	Decimation = 256
0	0.768	1.536	3.072
1	1.536	3.072	6.144
2	2.304	4.608	9.216
3	3.072	6.144	12.288
4	3.84	7.68	15.36
5	4.608	9.216	18.432
6	5.376	10.752	21.504
7	6.144	12.288	24.576

Full Power Mode CDC Conversion Sequence Time

The full power mode CDC conversion sequence time for all eight stages is set by configuring the SEQUENCE_STAGE_NUM and DECIMATION bits, as outlined in Table 9.

Figure 23 shows a simplified timing diagram of the full power CDC conversion time. The full power mode CDC conversion time, t_{CONV_FP}, is set using Table 9.

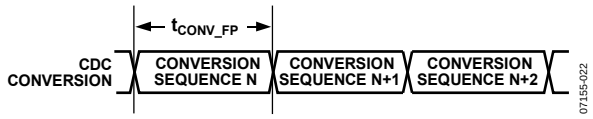


Figure 23. Full Power Mode CDC Conversion Sequence Time

Low Power Mode CDC Conversion Sequence Time with Delay

The frequency of each CDC conversion, while operating in the low power automatic wake-up mode, is controlled by using the LP_CONV_DELAY bits located at Address 0x000[3:2], in addition to the registers listed in Table 9. This feature provides some flexibility for optimizing the conversion time to meet system requirements vs. AD7148 power consumption.

For example, maximum power savings is achieved when the LP_CONV_DELAY bits (Address 0x000[3:2] are set to 11. With a setting of 11, the AD7148 automatically wakes up, performing a conversion every 800 ms.

Table 10. LP_CONV_DELAY Settings

LP_CONV_DELAY Bits	Delay Between Conversions (ms)
00	200
01	400
10	600
11	800

Figure 24 shows a simplified timing example of the low power CDC conversion time. As shown, the low power CDC conversion time is set by t_{CONV_FP} and the LP_CONV_DELAY bits.

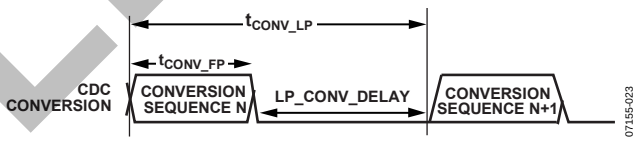


Figure 24. Low Power Mode CDC Conversion Sequence Time

CDC CONVERSION RESULTS

Certain high resolution sensors require the host to read back the CDC conversion results for processing. The registers required for host processing are located in the Bank 3 registers. The host processes the data readback from these registers using a software algorithm to determine position information.

In addition to the results registers found in the Bank 3 registers, the AD7148 provides the 16-bit CDC output data directly, starting at Address 0x00B of the Bank 1 registers. Reading back the CDC 16-bit conversion data register allows for customer-specific application data processing.

CAPACITANCE SENSOR INPUT CONFIGURATION

Each input connection from the external capacitance sensors to the AD7148 converter can be uniquely configured by using the registers in Bank 2 (see Table 39 through Table 42). These registers are used to configure input pin connection setups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Each sensor can be individually optimized. For example, a button sensor connected to STAGE0 can have different sensitivity and offset values from those of a button with a different function that is connected to a different stage.

CINx INPUT MULTIPLEXER SETUP

The CINx_CONNECTION_SETUP register bits provide options for connecting the sensor input pins to the CDC (see Table 39 and Table 40).

The AD7148 has an on-chip multiplexer to route the input signals from each pin to the input of the converter. Each input pin can be tied to either the negative or the positive input of the CDC, or it can be left floating. Each input can also be internally connected to the BIAS signal to help prevent cross coupling. If an input is not used, always connect it to BIAS.

Connecting a CINx input pin to the positive CDC input results in an increase in CDC output code when the corresponding sensor is activated. Connecting a CINx input pin to the negative CDC input results in a decrease in CDC output code when the corresponding sensor is activated.

The AD7148 performs a sequence of eight conversions. The multiplexer can have different connection settings for each of the eight conversions by using the CINx_CONNECTION_SETUP bits. For example, CIN0 can be connected to the negative CDC input or left floating. The same holds true for all eight conversion stages.

Two bits in each sequence stage register control the mux setting for the input pin, as shown in Figure 25.

SINGLE-ENDED CONNECTIONS TO THE CDC

A single-ended connection to the CDC is defined as having one CINx input connected to either the positive or the negative CDC input. A differential connection to the CDC is defined as having one CINx input connected to the positive CDC input and a second CINx input connected to the negative input of the CDC.

When a single-ended connection to the CDC is made in any stage, the SE_CONNECTION_SETUP bits in the STAGEx_CONNECTION_SETUP registers should be applied. These bits ensure that, during a single-ended connection to the CDC, the input paths to both terminals are matched. This matching of input paths, in turn, improves the power supply rejection of the converter measurement.

Table 11. Application of SE_CONNECTION_SETUP Bits

Bit Values	Description
00	Do not use.
01	Single-ended connection. For this stage, there is one CINx connected to the positive CDC input.
10	Single-ended connection. For this stage, there is one CINx connected to the negative CDC input.
11	Differential connection. For this stage, there is one CINx connected to the negative CDC input and one CINx connected to the positive CDC input.

If more than one CINx input is connected to either the positive or negative input of the converter for the same conversion, set SE_CONNECTION_SETUP = 11. For example, if CIN0 and CIN3 are connected to the positive input of the CDC, SE_CONNECTION_SETUP = 11.

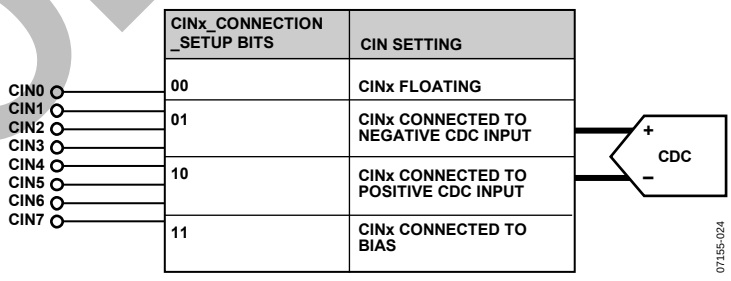


Figure 25. Input Mux Configuration Options

NONCONTACT PROXIMITY DETECTION

The AD7148 internal signal processing continuously monitors all capacitance sensors for noncontact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, at which time all internal calibration is immediately disabled while the AD7148 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 12. The FP_PROXIMITY_CNT and LP_PROXIMITY_CNT register bits (Address 0x002[11:4]) control the length of the calibration disable period after the user leaves the sensor and proximity is no longer active in full and low power modes.

The calibration is disabled during this time and is enabled again at the end of this period, provided that the user is no longer approaching, or in contact with, the sensor. Figure 26 and Figure 27 show examples of how these registers are used to set the full and low power mode calibration disable periods.

The calibration disable period in full power mode is equal to FP_PROXIMITY_CNT × 16 × time taken for one conversion sequence in full power mode.

The calibration disable period in low power mode is equal to LP_PROXIMITY_CNT × 4 × time taken for one conversion sequence in low power mode.

Table 12. Proximity Control Registers (See Figure 30)

Bits	Length	Register Address	Description
FP_PROXIMITY_CNT	4 bits	0x002[7:4]	Calibration disable time in full power mode.
LP_PROXIMITY_CNT	4 bits	0x002[11:8]	Calibration disable time in low power mode.
FP_PROXIMITY_RECAL	10 bits	0x004[9:0]	Full power mode proximity recalibration time.
LP_PROXIMITY_RECAL	6 bits	0x004[15:10]	Low power mode proximity recalibration time.
PROXIMITY_RECAL_LVL	8 bits	0x003[7:0]	Proximity recalibration level. This value, multiplied by 16, controls the sensitivity of Comparator 2 in Figure 30.
PROXIMITY_DETECTION_RATE	6 bits	0x003[13:8]	Proximity detection rate. This value, multiplied by 16, controls the sensitivity of Comparator 1 in Figure 30.

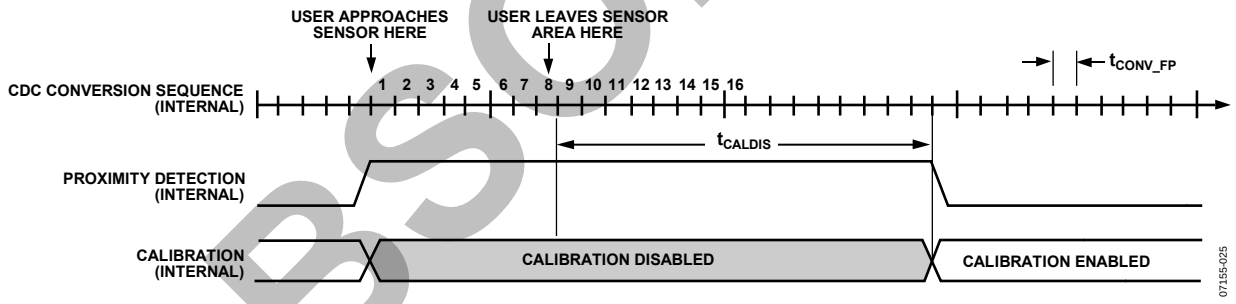


Figure 26. Full Power Mode Proximity Detection Example with FP_PROXIMITY_CNT = 1

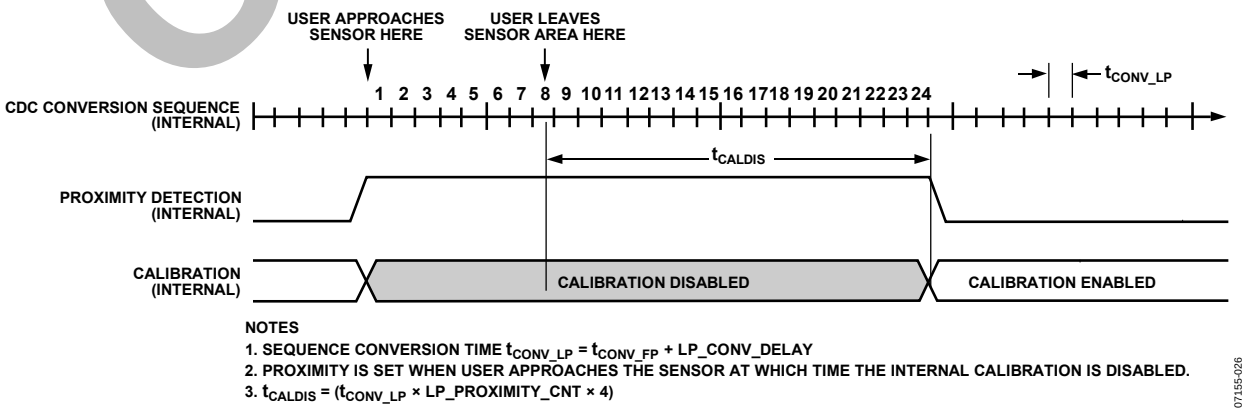


Figure 27. Low Power Mode Proximity Detection with LP_PROXIMITY_CNT = 4

RECALIBRATION

In certain situations, the proximity flag can be set for a long period: for example, when a user hovers over a sensor for a long time. The environmental calibration on the AD7148 is suspended while proximity is detected, but changes may occur to the ambient capacitance level during the proximity event. This means that the ambient value stored on the AD7148 no longer represents the actual ambient value. In this case, even when the user has left the sensor, the proximity flag may still be set. This situation could occur if user interaction creates some moisture on the sensor, causing the new sensor ambient value to be different from the expected value. In this situation, the AD7148 automatically forces an internal recalibration, ensuring that the ambient values are recalibrated, regardless of how long the user hovers over a sensor. The recalibration ensures maximum sensor performance.

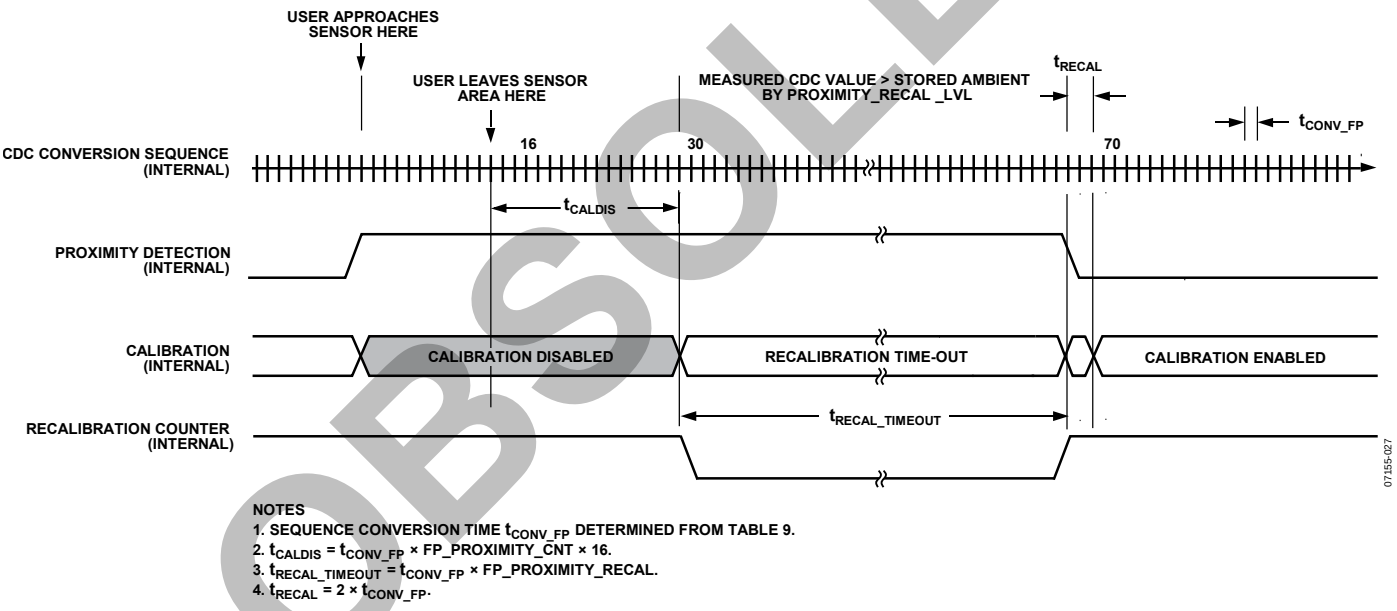
The AD7148 recalibrates automatically when the measured CDC value exceeds the stored ambient value by an amount determined by the PROXIMITY_RECAL_LVL bits (Address 0x003[7:0]) for a set period of time, known as the recalibration timeout.

In full power mode, the recalibration timeout is controlled by FP_PROXIMITY_RECAL; in low power mode, the timeout is controlled by LP_PROXIMTY_RECAL.

The recalibration timeout in full power mode is the value of the FP_PROXIMITY_RECAL multiplied by the time taken for one conversion sequence in full power mode.

The recalibration timeout in low power mode is the value of the LP_PROXIMITY_RECAL multiplied by the time taken for one conversion sequence in low power mode.

Figure 28 and Figure 29 show examples of how the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL register bits (Address 0x004[15:0]) control the timeout period before a recalibration while operating in the full power and low power modes. These figures show a user approaching a sensor, followed by the user leaving the sensor while the proximity detection remains active after the user leaves the sensor. The measured CDC value exceeds the stored ambient value by the amount set in the PROXIMITY_RECAL_LVL bits for the entire timeout period. The sensor is automatically recalibrated at the end of the timeout period.



NOTES
1. SEQUENCE CONVERSION TIME t_{CONV_FP} DETERMINED FROM TABLE 9.
2. $t_{CALDIS} = t_{CONV\_FP} \times FP\_PROXIMITY\_CNT \times 16$.
3. $t_{RECAL\_TIMEOUT} = t_{CONV\_FP} \times FP\_PROXIMITY\_RECAL$.
4. $t_{RECAL} = 2 \times t_{CONV\_FP}$.

Figure 28. Full Power Mode Proximity Detection with Forced Recalibration Example with FP_PROXIMITY_CNT = 1 and FP_PROXIMITY_RECAL = 40

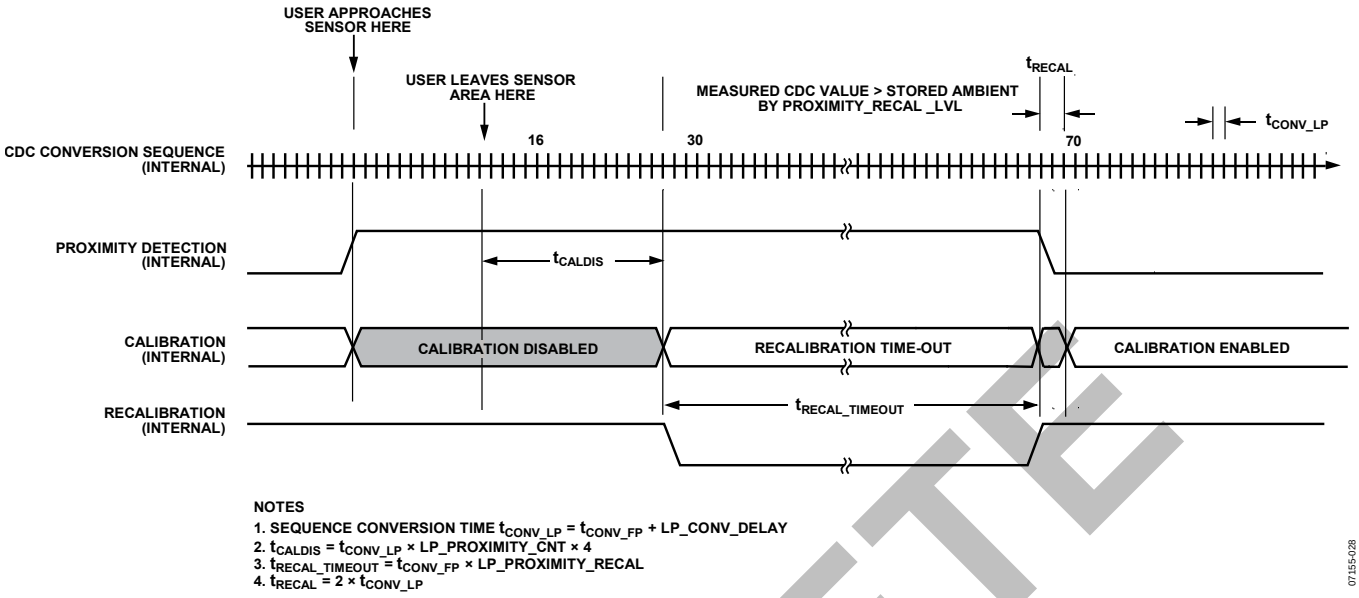


Figure 29. Low Power Mode Proximity Detection with Forced Recalibration Example with LP_PROXIMITY_CNT = 4 and LP_PROXIMITY_RECAL = 40

PROXIMITY SENSITIVITY

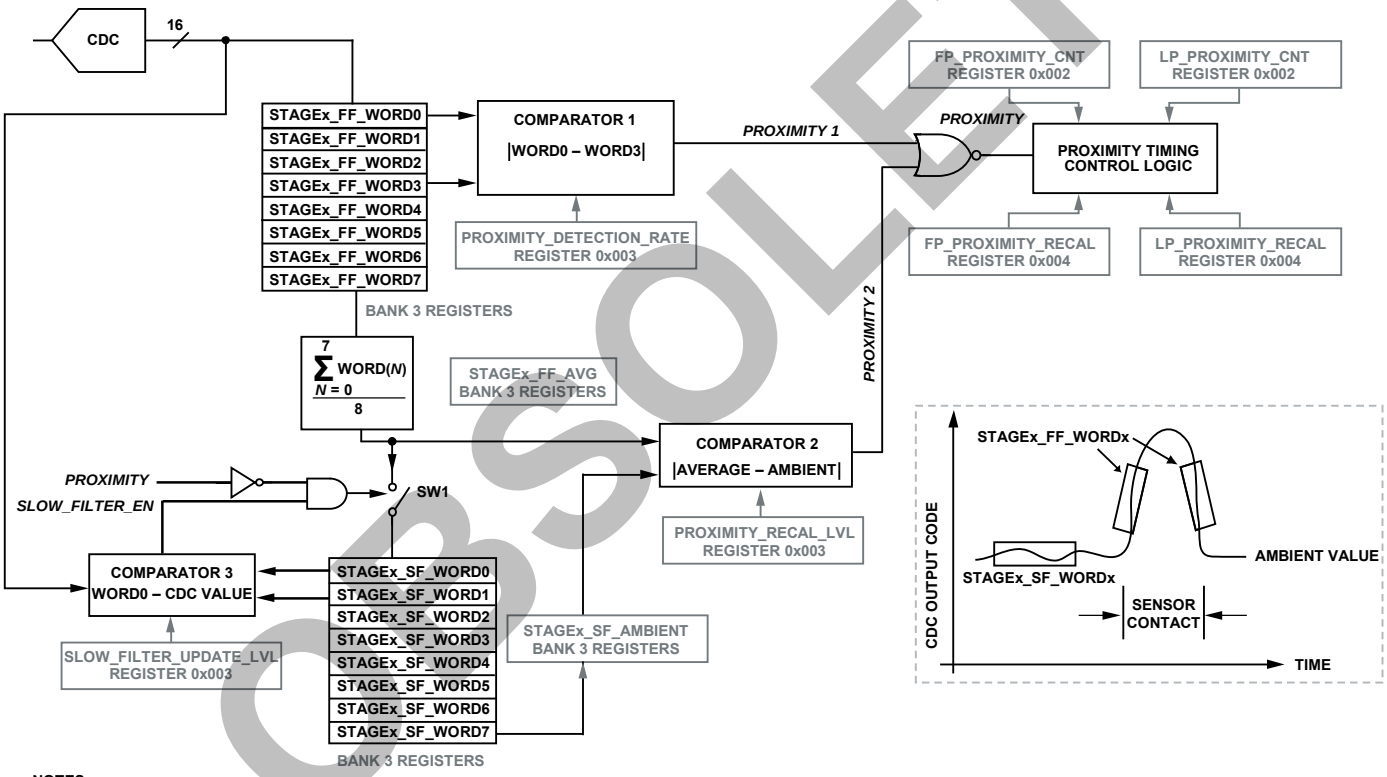
The fast filter in Figure 30 is used to detect when someone is close to the sensor (proximity). Two conditions set the internal proximity detection signal, using Comparator 1 and Comparator 2. Comparator 1 detects when a user is approaching a sensor. The PROXIMITY_DETECTION_RATE bits (Address0x003[13:8]) controls the sensitivity of Comparator 1. For example, if PROXIMITY_DETECTION_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceeds (4 × 16) LSB codes. Comparator 2 detects when a user hovers over a sensor or approaches a sensor very slowly. The PROXIMITY_RECAL_LVL bits (Address 0x003[7:0]) control the sensitivity of Comparator 2. For example, if PROXIMITY_RECAL_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds (75 × 16) LSB codes.

FF_SKIP_CNT

The proximity detection fast FIFO is used by the on-chip logic to determine if proximity is detected . The fast FIFO expects to receive samples from the converter at a set rate. FF_SKIP_CNT (Register 0x002[3:0]) is the fast filter skip control, which used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence. This value determines which CDC samples are not used (skipped) in the proximity detection fast FIFO.

Determining the FF_SKIP_CNT value is required only once during the initial setup of the capacitance sensor interface. Table 13 shows how FF_SKIP_CNT controls the update rate to the fast FIFO. Recommended value for this setting, when using all eight conversion stages on the AD7148, is

FF_SKIP_CNT = 0000 = no samples skipped.



NOTES
1. *SLOW_FILTER_EN* IS SET AND SW1 IS CLOSED WHEN |STAGEx_SF_WORD0–STAGEx_SF_WORD 1| EXCEEDS THE VALUE PROGRAMMED IN THE SLOW_FILTER_UPDATE_LVL BITS PROVIDING *PROXIMITY* IS NOT SET.
2. *PROXIMITY 1* IS SET WHEN |STAGEx_FF_WORD0– STAGEx_FF_WORD3| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_DETECTION_RATE BITS.
3. *PROXIMITY 2* IS SET WHEN |AVERAGE–AMBIENT| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_RECAL_LVL BITS.
4. DESCRIPTION OF COMPARATOR FUNCTIONS:
   COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.
   COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR OR APPROACHING A SENSOR VERY SLOWLY.
   ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF USER INTERACTION.
   FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.
   COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN*SLOW_FILTER_EN* IS SET AND *PROXIMITY* IS NOT SET.

Figure 30. Proximity Detection Logic

Table 13. FF_SKIP_CNT Settings

FF_SKIP_CNT	Fast FIFO Update Rate		
	Decimation = 64	**Decimation = 128**	**Decimation = 256**
0	0.768 × (SEQUENCE_STAGE_NUM + 1) ms	1.536 × (SEQUENCE_STAGE_NUM + 1) ms	3.072 × (SEQUENCE_STAGE_NUM + 1) ms
1	1.536 × (SEQUENCE_STAGE_NUM + 1) ms	3.072 × (SEQUENCE_STAGE_NUM + 1) ms	6.144 × (SEQUENCE_STAGE_NUM + 1) ms
2	2.3 × (SEQUENCE_STAGE_NUM + 1) ms	4.608 × (SEQUENCE_STAGE_NUM + 1) ms	9.216 × (SEQUENCE_STAGE_NUM + 1) ms
3	3.072 × (SEQUENCE_STAGE_NUM + 1) ms	6.144 × (SEQUENCE_STAGE_NUM + 1) ms	12.288 × (SEQUENCE_STAGE_NUM + 1) ms
4	3.84 × (SEQUENCE_STAGE_NUM + 1) ms	7.68 × (SEQUENCE_STAGE_NUM + 1) ms	15.36 × (SEQUENCE_STAGE_NUM + 1) ms
5	4.6 × (SEQUENCE_STAGE_NUM + 1) ms	9.216 × (SEQUENCE_STAGE_NUM + 1) ms	18.432 × (SEQUENCE_STAGE_NUM + 1) ms
6	5.376 × (SEQUENCE_STAGE_NUM + 1) ms	10.752 × (SEQUENCE_STAGE_NUM + 1) ms	21.504 × (SEQUENCE_STAGE_NUM + 1) ms
7	6.144 × (SEQUENCE_STAGE_NUM + 1) ms	12.288 × (SEQUENCE_STAGE_NUM + 1) ms	24.576 × (SEQUENCE_STAGE_NUM + 1) ms
8	6.912× (SEQUENCE_STAGE_NUM + 1) ms	13.824 × (SEQUENCE_STAGE_NUM + 1) ms	27.648 × (SEQUENCE_STAGE_NUM + 1) ms
9	7.68 × (SEQUENCE_STAGE_NUM + 1) ms	15.36 × (SEQUENCE_STAGE_NUM + 1) ms	30.72 × (SEQUENCE_STAGE_NUM + 1) ms
10	8.448× (SEQUENCE_STAGE_NUM + 1) ms	16.896 × (SEQUENCE_STAGE_NUM + 1) ms	33.792 × (SEQUENCE_STAGE_NUM + 1) ms
11	9.216 × (SEQUENCE_STAGE_NUM + 1) ms	18.432 × (SEQUENCE_STAGE_NUM + 1) ms	36.864 × (SEQUENCE_STAGE_NUM + 1) ms
12	9.984 × (SEQUENCE_STAGE_NUM + 1) ms	19.968 × (SEQUENCE_STAGE_NUM + 1) ms	39.936 × (SEQUENCE_STAGE_NUM + 1) ms
13	10.752 × (SEQUENCE_STAGE_NUM + 1) ms	21.504 × (SEQUENCE_STAGE_NUM + 1) ms	43.008 × (SEQUENCE_STAGE_NUM + 1) ms
14	11.52 × (SEQUENCE_STAGE_NUM + 1) ms	23.04 × (SEQUENCE_STAGE_NUM + 1) ms	46.08 × (SEQUENCE_STAGE_NUM + 1) ms
15	12.288 × (SEQUENCE_STAGE_NUM + 1) ms	24.576 × (SEQUENCE_STAGE_NUM + 1) ms	49.152 × (SEQUENCE_STAGE_NUM + 1) ms

ENVIRONMENTAL CALIBRATION

The AD7148 provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the capacitance sensor ambient levels. Capacitance sensor output levels are sensitive to temperature, humidity, and in some cases, dirt. The AD7148 achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and correcting for any changes by adjusting the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD register values, as described in Equation 1 and Equation 2. The CDC ambient level is defined as the capacitance sensor output level during periods when the user is not approaching or in contact with the sensor.

The compensation logic runs automatically on every conversion after configuration when the AD7148 is not being touched, which allows the AD7148 to account for rapidly changing environmental conditions.

The ambient compensation control registers give the host access to general setup and controls for the compensation algorithm. On-chip RAM stores the compensation data for each conversion stage, as well as setup information specific to each stage.

Figure 31 shows an example of an ideal capacitance sensor behavior where the CDC ambient level remains constant, regardless of the environmental conditions. The CDC output shown is for a pair of differential button sensors, where one sensor caused an increase and the other caused a decrease in measured capacitance when activated. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values based on the threshold sensitivity settings and the ambient value. These values are sufficient to detect a sensor contact, resulting in the AD7148 asserting the $\overline{\text{INT}}$ output when threshold levels are exceeded.

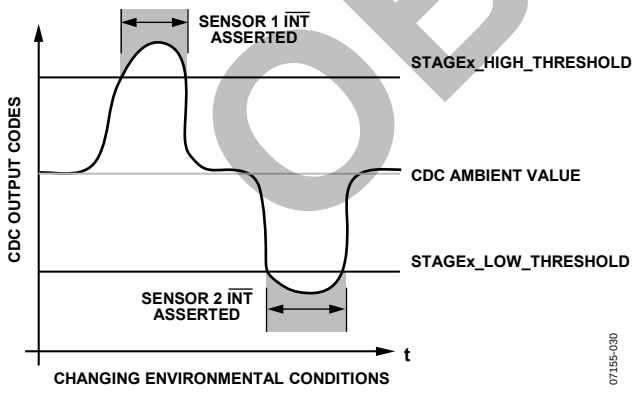


Figure 31. Ideal Sensor Behavior with a Constant Ambient Level

CAPACITANCE SENSOR BEHAVIOR WITHOUT CALIBRATION

Figure 32 shows the typical behavior of a capacitance sensor with no applied calibration. This figure shows ambient levels drifting over time as environmental conditions change. The ambient level drift results in the detection of a missed user contact on Sensor 2. This is a result of the initial low offset level remaining constant while the ambient levels drifted upward beyond the detection range.

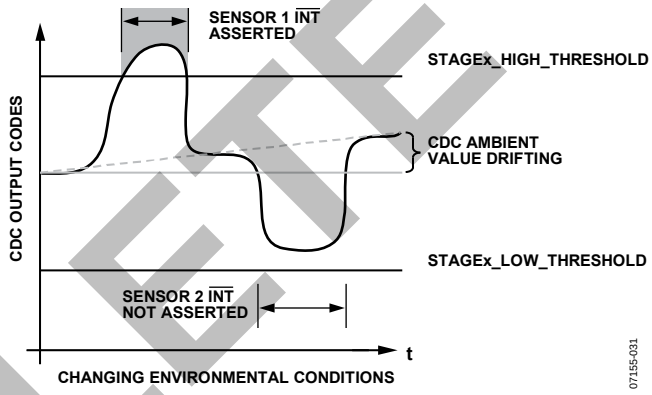


Figure 32. Typical Sensor Behavior Without Calibration Applied

The Capacitance Sensor Behavior with Calibration section describes how the AD7148 adaptive calibration algorithm prevents errors such as this from occurring.

CAPACITANCE SENSOR BEHAVIOR WITH CALIBRATION

The AD7148 on-chip adaptive calibration algorithm prevents sensor detection errors such as the one shown in Figure 32. Error prevention is accomplished by monitoring CDC ambient levels and readjusting the initial STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values according to the amount of ambient drift measured on each sensor. The internal STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values described in Equation 1 and Equation 2 are automatically updated based on the new values of STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW. This closed-loop routine ensures the reliability and repeatable operation of every sensor connected to the AD7148 under dynamic environmental conditions. Figure 33 shows a simplified example of how the AD7148 applies the adaptive calibration process resulting in no interrupt errors under changing CDC ambient levels due to environmental conditions.

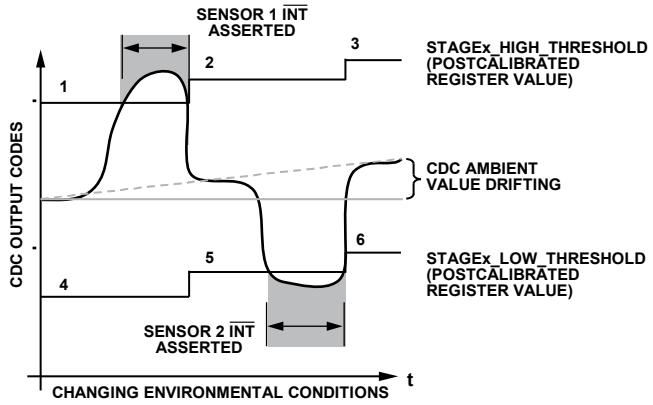


Figure 33. Typical Sensor Behavior with Calibration Applied on the Data Path

SLOW FIFO

As shown in Figure 30, there are a number of FIFOs implemented on the AD7148. These FIFOs are located in Bank 3 of the on-chip memory. The slow FIFOs are used by on-chip logic to monitor the ambient capacitance level from each sensor.

AVG_FP_SKIP and AVG_LP_SKIP

In Register 0x001, Bits[13:12]are the slow FIFO skip control for full power mode, AVG_FP_SKIP. Bits[15:14] in the same register are the slow FIFO skip control for low power mode, AVG_LP_SKIP. These values determine which CDC samples are not used (skipped) in the slow FIFO. Changing theses values slows down or speeds up the rate at which the ambient capacitance value tracks the measured capacitance value read by the converter.

Slow FIFO update rate in full power mode is equal to

AVG_FP_SKIP × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM +1) × (FF_SKIP_CNT +1) × 4x10^{-7}]

Slow FIFO update rate in low power mode is equal to

(AVG_LP_SKIP +1) × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM +1) × (FF_SKIP_CNT +1) × 4x10^{-7}]/[(FF_SKIP_CNT +1) + LP_CONV_DELAY]

The slow FIFO is used by the on-chip logic to track the ambient capacitance value. The slow FIFO expects to receive samples from the converter at a rate of 25 ms. AVG_FP_SKIP and AVG_LP_SKIP are used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence.

Determining the AVG_FP_SKIP and AVG_LP_SKIP values is required only once during the initial setup of the capacitance sensor interface. When using all eight conversion stages, recommended values for these settings are

AVG_FP_SKIP = 00 = skip 3 samples

AVG_LP_SKIP = 00 = skip 0 samples

SLOW_FILTER_UPDATE_LVL

The SLOW_FILTER_UPDATE_LVL (Address 0x003[15:14]) controls whether the most recent CDC measurement goes into the slow FIFO (slow filter) or not. The slow filter is updated when the difference between the current CDC value and last value pushed into the slow FIFO is greater than SLOW_FILTER_UPDATE_LVL.

Equations for On-Chip Logic Stage High and Logic Stage Low Threshold Calculation

$$STAGEx\_HIGH\_THRESHOLD = STAGE\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_HIGH}{4}\right) + \left(\frac{STAGEx\_OFFSET\_HIGH - \frac{STAGEx\_OFFSET\_HIGH}{4}}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY \quad (1)$$

$$STAGEx\_LOW\_THRESHOLD = STAGE\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_LOW}{4}\right) + \left(\frac{STAGEx\_OFFSET\_LOW - \frac{STAGEx\_OFFSET\_LOW}{4}}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY \quad (2)$$

ADAPTIVE THRESHOLD AND SENSITIVITY

The AD7148 provides an on-chip self-learning adaptive threshold and sensitivity algorithm. This algorithm continuously monitors the output levels of each sensor and automatically rescales the threshold levels proportionally to the sensor area covered by the user. As a result, the AD7148 maintains optimal threshold and sensitivity levels for all types of users, regardless of finger size.

The threshold level is always referenced from the ambient level and is defined as the CDC converter output level that must be exceeded for a valid sensor contact. The sensitivity level is defined as how sensitive the sensor is before a valid contact is registered.

Figure 34 provides an example of how the adaptive threshold and sensitivity algorithm works. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values, based on the threshold sensitivity settings and the ambient value. On configuration, initial estimates are supplied for both STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW, after which the calibration engine automatically adjusts the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values for sensor response.

The AD7148 tracks the average maximum and minimum values measured from each sensor. These values give an indication of how the user is interacting with the sensor. A large finger gives a large average maximum or minimum value, and a small finger gives smaller values. When the average maximum or minimum value changes, the threshold levels are rescaled to ensure that the threshold levels are appropriate for the current user. Figure 35 shows how the minimum and maximum sensor responses are tracked by the on-chip logic.

Reference A in Figure 34 shows an undersensitive threshold level for a small finger user, demonstrating the disadvantages of a fixed threshold level.

By enabling the adaptive threshold and sensitivity algorithm, the positive and negative threshold levels are determined by the POS_THRESHOLD_SENSITIVITY and NEG_THRESHOLD_SENSITIVITY values and the most recent average maximum sensor output value. These bits can be used to select 16 different positive and negative sensitivity levels ranging between 25% and 95.32% of the most recent average maximum output level referenced from the ambient value. The smaller the sensitivity percentage setting, the easier it is to trigger a sensor activation. Reference B shows that the positive adaptive threshold level is set at almost mid-sensitivity with a 62.51% threshold level by setting POS_THRESHOLD_SENSITIVITY = 1000. Figure 34 also provides a similar example for the negative threshold level with NEG_THRESHOLD_SENSITIVITY = 0011.

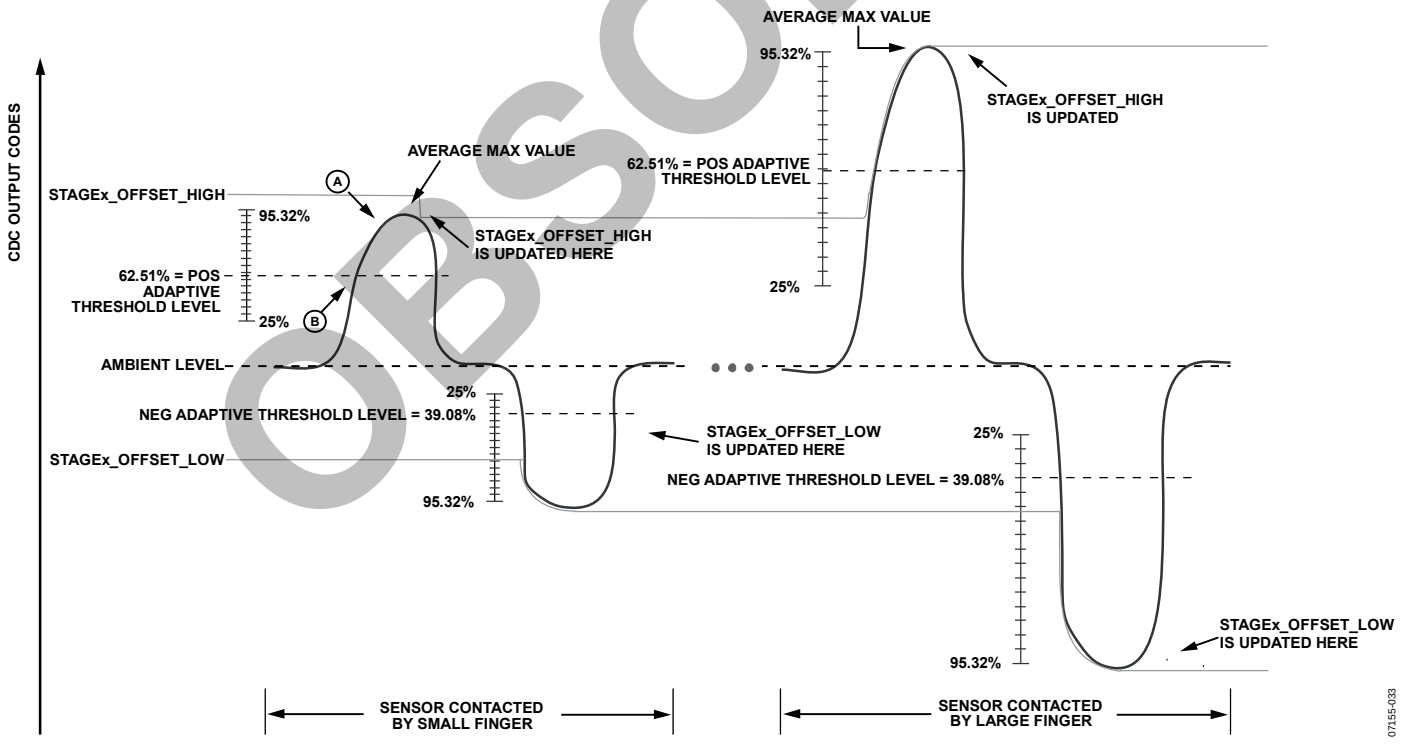


Figure 34. Threshold Sensitivity Example with POS_THRESHOLD_SENSITIVITY = 1000 and NEG_THRESHOLD_SENSITIVITY = 0011

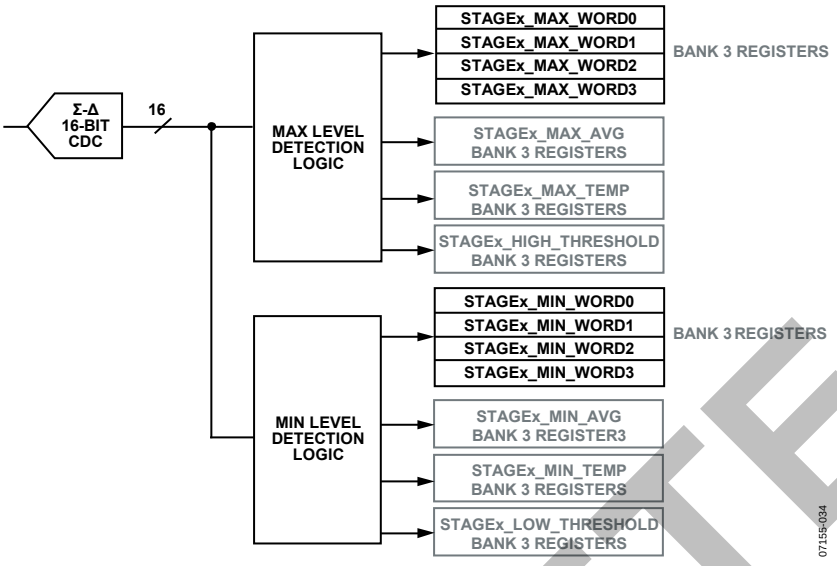


Figure 35. Tracking the Minimum and Maximum Average Sensor Values

Table 14. Additional Information About Environmental Calibration and Adaptive Threshold Registers

Bit	Register Location	Description
NEG_THRESHOLD_SENSITIVITY	Bank 2	Used in Equation 2. This value is programmed once at startup.
NEG_PEAK_DETECT	Bank 2	Used by internal adaptive threshold logic only. The NEG_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the minimum average CDC value. If the output of the CDC gets within the NEG_PEAK_DETECT percentage of the minimum average, only then is the minimum average value updated.
POS_THRESHOLD_SENSITIVITY	Bank 2	Used in Equation 1. This value is programmed once at startup.
POS_PEAK_DETECT	Bank 2	Used by internal adaptive threshold logic only. The POS_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the maximum average CDC value. If the output of the CDC gets within the POS_PEAK_DETECT percentage of the maximum average, only then is the maximum average value updated.
STAGEx_OFFSET_LOW	Bank 2	Used in Equation 2. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7148 on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set to 80% of the STAGEx_OFFSET_LOW_CLAMP value.
STAGEx_OFFSET_HIGH	Bank 2	Used in Equation 1. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7148 on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set to 80% of the STAGEx_OFFSET_HIGH_CLAMP value.
STAGEx_OFFSET_HIGH_CLAMP	Bank 2	Used by internal environmental calibration and adaptive threshold algorithms only. An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing sensor output value to exceed the expected nominal value. Set to the maximum expected sensor response, maximum change in CDC output code.
STAGEx_OFFSET_LOW_CLAMP	Bank 2	Used by internal environmental calibration and adaptive threshold algorithms only. An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing sensor output value to exceed the expected nominal value. Set to the minimum expected sensor response, minimum change in CDC output code .
STAGEx_SF_AMBIENT	Bank 3	Used in Equation 1 and Equation 2. This is the ambient sensor output, when the sensor is not touched, as calculated using the slow FIFO.
STAGEx_HIGH_THRESHOLD	Bank 3	Equation 1 value.
STAGEx_LOW_THRESHOLD	Bank 3	Equation 2 value.

INTERRUPT OUTPUT

The AD7148 has an interrupt output that triggers an interrupt service routine on the host processor. The $\overline{\text{INT}}$ signal is on Pin 12 and is an open-drain output. There are two types of interrupt events on the AD7148: a CDC conversion complete interrupt and a sensor threshold interrupt. Each interrupt has enable and status registers. The conversion complete and sensor threshold interrupts can be enabled on a per conversion stage basis. The status registers indicate what type of interrupt triggered the $\overline{\text{INT}}$ pin. Status registers are cleared, and the $\overline{\text{INT}}$ signal is reset high during a read operation. The signal returns high as soon as the read address is set up.

CDC CONVERSION-COMPLETE INTERRUPT

The AD7148 interrupt signal asserts low to indicate the completion of a conversion stage, and new conversion result data is available in the registers.

The interrupt can be independently enabled for each conversion stage. Each conversion-stage-complete interrupt can be enabled via the STAGEx_COMPLETE_INT_EN register (Address 0x007). This register has a bit that corresponds to each conversion stage. Setting this bit to 1 enables the interrupt for that stage. Clearing this bit to 0 disables the conversion complete interrupt for that stage.

In normal operation, the interrupt is enabled only for the last stage in a conversion sequence. For example, if there are five conversion stages, the conversion-complete interrupt for STAGE4 is enabled. $\overline{\text{INT}}$ asserts only when all five conversion stages are complete, and the host can read new data from all five results registers. The interrupt is cleared by reading the STAGEx_COMPLETE_INT_STATUS register located at Address 0x00A.

Register 0x00A is the conversion-complete interrupt status register. Each bit in this register corresponds to a conversion stage. If a bit is set, it means that the conversion-complete interrupt for the corresponding stage has been triggered. This register is cleared on a read, provided that the underlying condition that triggered the interrupt has gone away.

SENSOR TOUCH INTERRUPT

The sensor touch interrupt mode is implemented when the host processor requires an interrupt only when a sensor is contacted. Configuring the AD7148 into this mode results in the interrupt being asserted when the user makes contact with the sensor and again when the user lifts off the sensor. The second interrupt is required to alert the host processor that the user is no longer contacting the sensor.

The registers located at Address 0x005 (STAGEx_LOW_INT_EN) and Address 0x006 (STAGEx_HIGH_INT_EN) are used to enable the interrupt output for each stage. The registers located at Address 0x008 (STAGEx_LOW_LIMIT_INT) and Address 0x009 (STAGEx_HIGH_LIMIT_INT) are used to read back the interrupt status for each stage.

Figure 36 shows the interrupt output timing during contact with one of the sensors connected to STAGE0 while operating in the sensor touch interrupt mode. For a low limit configuration, the interrupt output is asserted as soon as the sensor is contacted and again after the user has stopped contacting the sensor.

Note that the interrupt output remains low until the host processor reads back the interrupt status registers located at Address 0x008 and Address 0x009.

The interrupt output is asserted when there is a change in the threshold status bits. This change indicates that a user is now touching the sensor(s) for the first time, the number of sensors being touched has changed, or the user is no longer touching the sensor(s). Reading the status bits in the interrupt status register shows the current sensor activations.

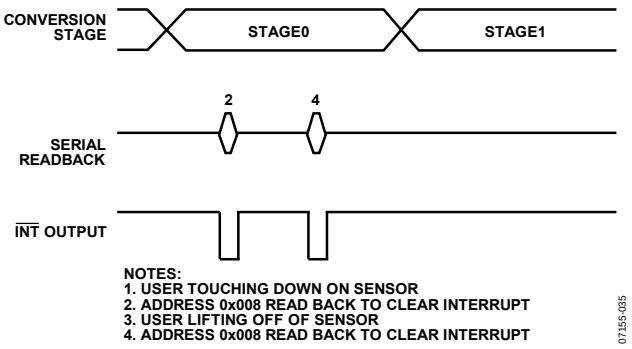


Figure 36. Example of Sensor Touch Interrupt

AC_{SHIELD} OUTPUT

The AD7148 measures capacitance between CINx and ground. Any capacitance to ground on the signal path between the CINx pins and the sensor is included in the conversion result.

To eliminate the stray capacitance to ground, the AC_{SHIELD} signal should be used to shield the connection between the sensor and CINx, as shown in Figure 37. The plane around the sensors should also be connected to AC_{SHIELD}.

The AC_{SHIELD} output is the same signal waveform as the excitation signal on CINx. Therefore, there is no ac current between CINx and AC_{SHIELD}, and any capacitance between these pins does not affect the CINx charge transfer.

Using AC_{SHIELD} eliminates capacitance-to-ground pick-up, which means that the AD7148 can be placed up to 60 cm away from the sensors. This allows the AD7148 to be placed on a separate PCB from the sensors, provided that the connections between the sensors and the CINx inputs are correctly shielded, using AC_{SHIELD}.

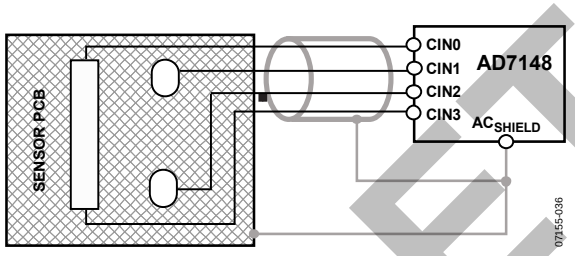


Figure 37. AC_{SHIELD}

I²C-COMPATIBLE SERIAL INTERFACE

The AD7148 supports the industry standard 2-wire I²C serial interface protocol. The two wires associated with the I²C timing are the SCLK and the SDA inputs. The SDA is an I/O pin that allows both register write and register readback operations. The AD7148 is always a slave device on the I²C serial interface bus.

It has a single fixed 7-bit device address, Address 0101 110. The AD7148 responds when the master device sends its device address over the bus. The AD7148 cannot initiate data transfers on the bus.

Table 15. AD7148 I²C Device Address

DEV A6	DEV A5	DEV A4	DEV A3	DEV A2	DEV A1	DEV A0
0	1	0	1	1	1	0

Data Transfer

Data is transferred over the I²C serial interface in 8-bit bytes. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCLK, remains high. This indicates that an address/data stream follows.

All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from, or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

Data is sent over the serial bus in a sequence of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes are read or written, a stop condition is established. A stop condition is defined by a low-to-high transition on SDA, while SCLK remains high. If the AD7148 encounters a stop condition, it returns to its idle condition, and the address pointer register resets to Address 0x00.

Writing Data over the I²C Bus

The process for writing to the AD7148 over the I²C bus is shown in Figure 38 and Figure 40. The device address is sent over the bus followed by the R/$\overline{W}$ bit set to 0. This is followed by two bytes of data that contain the 10-bit address of the internal data register to be written. The following bit map shows the upper register address bytes. Note that Bit 7 to Bit 2 in the upper address byte are don't care bits. The address is contained in the 10 LSBs of the register address bytes.

MSB **LSB**

7	6	5	4	3	2	1	0
X	X	X	X	X	X	Register Address Bit 9	Register Address Bit 8

The following bit map shows the lower register address bytes.

MSB **LSB**

7	6	5	4	3	2	1	0
Reg Add Bit 7	Reg Add Bit 6	Reg Add Bit 5	Reg Add Bit 4	Reg Add Bit 3	Reg Add Bit 2	Reg Add Bit 1	Reg Add Bit 0

The third data byte contains the eight MSBs of the data to be written to the internal register. The fourth data byte contains the eight LSBs of data to be written to the internal register.

The AD7148 address pointer register automatically increments after each write, allowing the master to sequentially write to all registers on the AD7148-1 in the same write transaction. However, the address pointer register does not wrap around after the last address.

Any data written to the AD7148 after the address pointer has reached its maximum value is discarded.

All registers on the AD7148 have 16 bits. Two consecutive 8-bit data bytes are combined and written to the 16-bit registers. To avoid errors, all writes to the device must contain an even number of data bytes.

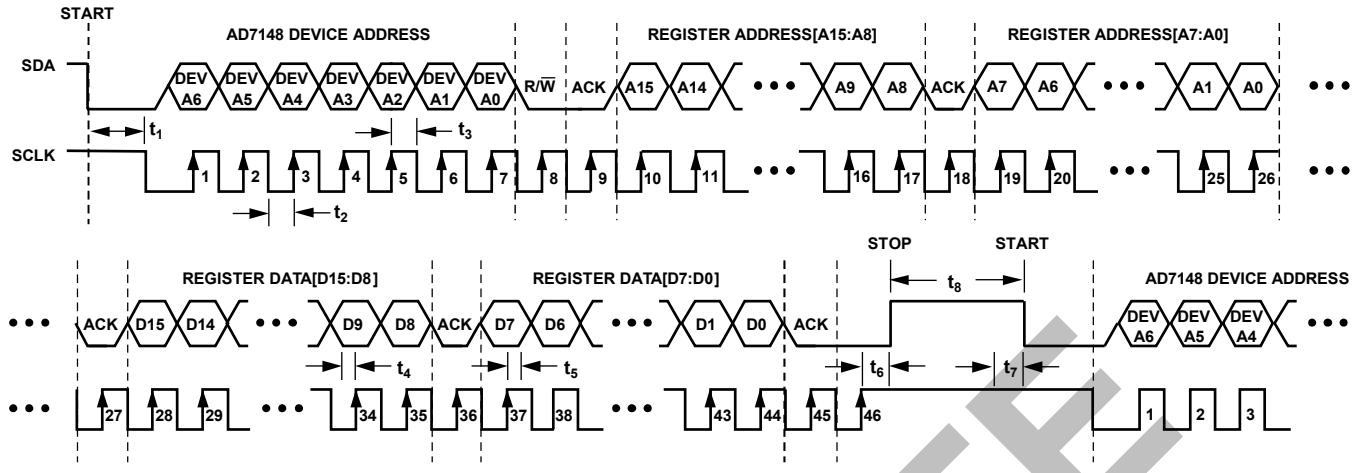
To finish the transaction, the master generates a stop condition on SDO or generates a repeat start condition if the master is to maintain control of the bus.

Reading Data over the I²C Bus

To read from the AD7148, the address pointer register must first be set to the address of the required internal register. The master performs a write transaction and writes to the AD7148 to set the address pointer. The master then outputs a repeat start condition to keep control of the bus or, if this is not possible, ends the write transaction with a stop condition. A read transaction is initiated, with the R/$\overline{W}$ bit set to 1.

The AD7148 supplies the upper eight bits of data from the addressed register in the first readback byte, followed by the lower eight bits in the next byte. This operation is shown in Figure 39 and Figure 40.

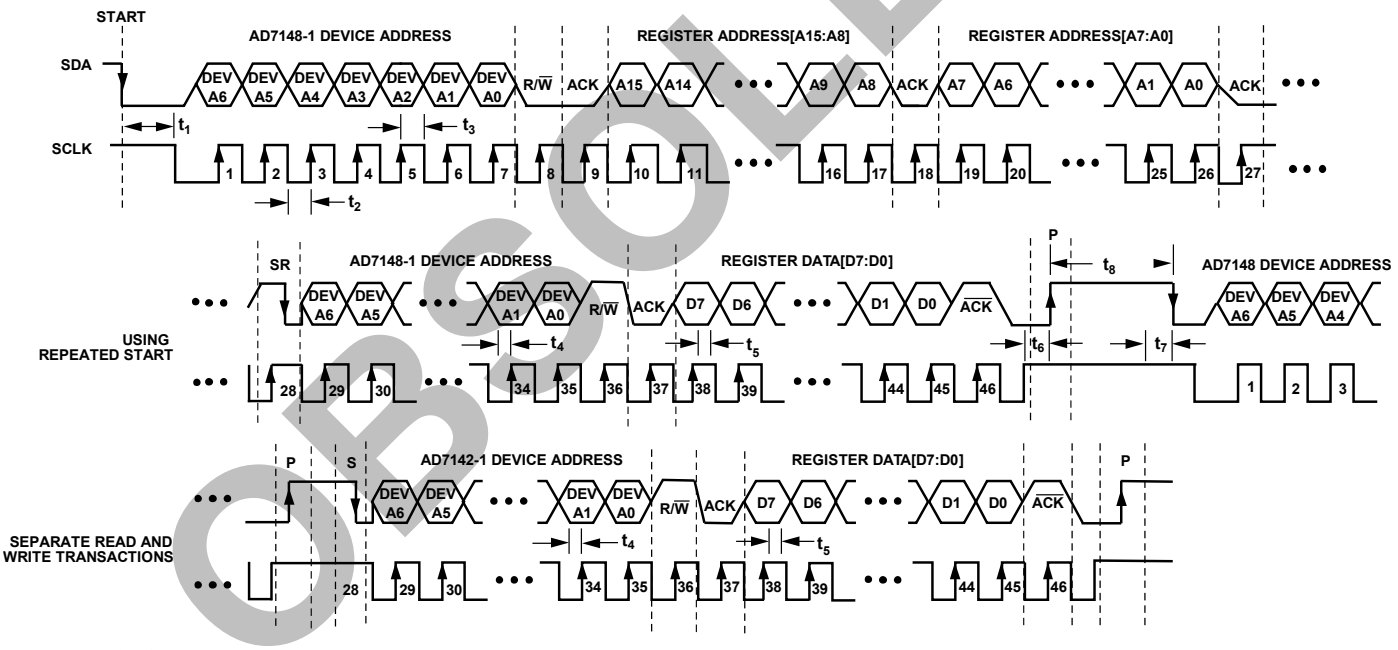
Because the address pointer automatically increases after each read, the AD7148 continues to output readback data until the master puts a no acknowledge and a stop condition on the bus. If the address pointer reaches its maximum value, and the master continues to read from the part, the AD7148 repeatedly sends data from the last register addressed.



NOTES
1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
3. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 X X], WHERE X ARE DON'T CARE BITS.
4. 16-BIT REGISTER ADDRESS[A15:A0] = [X, X, X, X, X, X, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0], WHERE X ARE DON'T CARE BITS.
5. REGISTER ADDRESS [A15:A8] AND REGISTER ADDRESS [A7:A0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
6. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.

07155-037

Figure 38. Example of I²C Timing for Single Register Write Operation



NOTES
1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
3. THE MASTER GENERATES THE $\overline{\text{ACK}}$ AT THE END OF THE READBACK TO SIGNAL THAT IT DOES NOT WANT ADDITIONAL DATA.
4. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 X X], WHERE THE TWO LSB X's ARE DON'T CARE BITS.
5. 16-BIT REGISTER ADDRESS[A15:A0] = [X, X, X, X, X, X, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0], WHERE THE UPPER LSB X's ARE DON'T CARE BITS.
6. REGISTER ADDRESS [A15:A8] AND REGISTER ADDRESS [A7:A0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
7. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
8. THE R/$\overline{\text{W}}$ BIT IS SET TO A1 TO INDICATE A READBACK OPERATION.

07155-038

Figure 39. Example of I²C Timing for Single Register Readback Operation

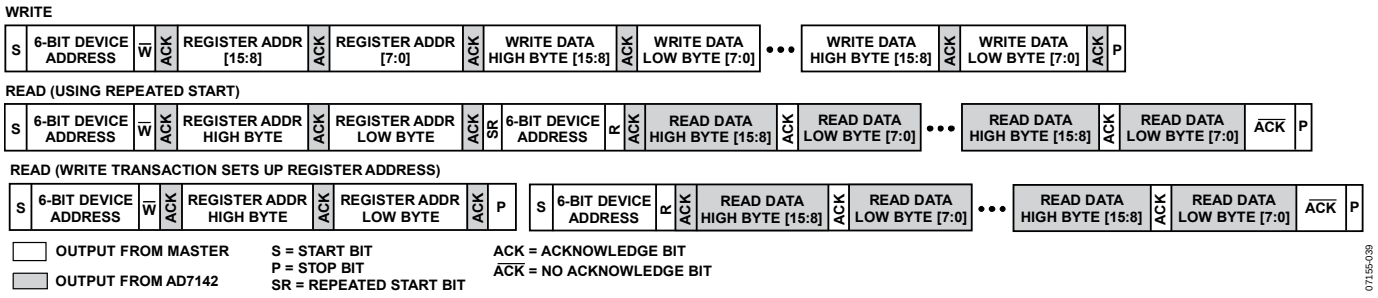


Figure 40. Example of Sequential I²C Write and Readback Operation

V_{DRIVE} INPUT

The supply voltage to all pins associated with the I²C serial interface (SCLK, SDA) is separate from the main V_{CC} supplies and is connected to the V_{DRIVE} pin.

This arrangement allows the AD7148 to be connected directly to processors whose supply voltage is less than the minimum operating voltage of the AD7148 without the need for external level-shifters. The V_{DRIVE} pin can be connected to voltage supplies as low as 1.65 V and as high as V_{CC}.

PCB DESIGN GUIDELINES

CAPACITIVE SENSOR BOARD MECHANICAL SPECIFICATIONS

Table 16.

Parameter	Symbol	Min	Typ	Max	Unit
Distance from Edge of Any Sensor to Edge of Grounded Metal Object	D_1	0.1			mm
Distance Between Sensor Edges[1]	$D_2 = D_3 = D_4$	0			mm
Distance Between Bottom of Sensor Board and Controller Board or Grounded Metal Casing[2]	D_5		1.0		mm

[1] The distance is dependent on the application and the positioning of the switches relative to each other and with respect to the user's finger positioning and handling. Adjacent sensors, with 0 minimum space between them, are implemented differentially.

[2] The 1.0 mm specification is meant to prevent direct sensor board contact with any conductive material. This specification does not guarantee no EMI coupling from the controller board to the sensors. Address potential EMI coupling issues by placing a grounded metal shield between the capacitive sensor board and the main controller board, as shown in Figure 43.

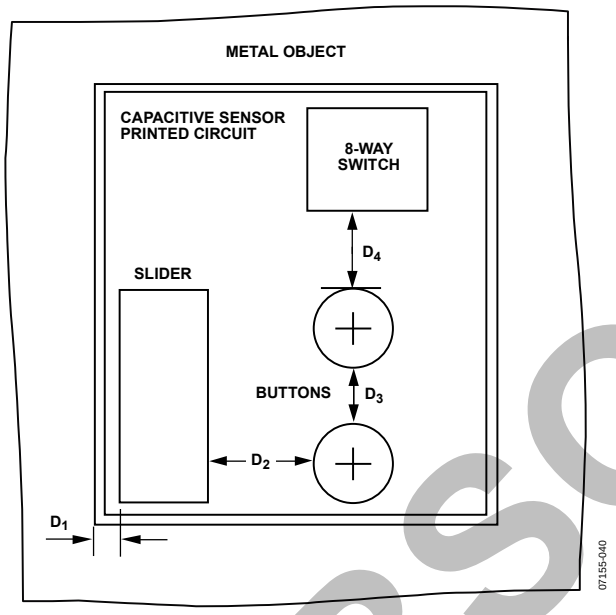


Figure 41. Capacitive Sensor Board Mechanicals Top View

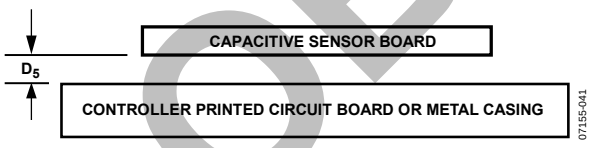


Figure 42. Capacitive Sensor Board Mechanicals Side View

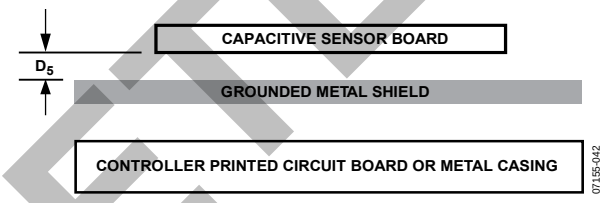


Figure 43. Capacitive Sensor Board with Grounded Shield

CHIP SCALE PACKAGES

The lands on the chip scale package (CP-16-13) are rectangular. The printed circuit board pad for this package should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center the land on the pad to maximize the solder joint size.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. To avoid shorting, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the land pattern on the printed circuit board.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

Connect the printed circuit board thermal pad to GND.

POWER-UP SEQUENCE

When the AD7148 is powered up, the following sequence is recommended when initially developing the AD7148 and host microprocessor serial interface:

1. Turn on the power supplies to the AD7148.
2. Write to the Bank 2 registers at Address 0x080 through Address 0x0BF. These registers are contiguous, so a sequential register write sequence can be applied. Note that the Bank 2 register values are unique for each application. Register values come from characterization of the sensor in the application and may be provided by Analog Devices after the sensor board has been developed.
3. Write to the Bank 1 registers at Address 0x000 through Address 0x007, as outlined in the following list.

   Caution

   At this time, Address 0x001 must remain set to Default Value 0x0000 during this contiguous write operation.

   Register values:
   Address 0x000 = 0x0B2
   Address 0x001 = 0x000
   Address 0x002 = 0x3230 (depends on number of conversion stages used)
   Address 0x003 = 0x0419
   Address 0x004 = 0x0832
   Address 0x005 = interrupt enable register; depends on required interrupt behavior
   Address 0x006 = interrupt enable register; depends on required interrupt behavior
   Address 0x007 = interrupt enable register; depends on required interrupt behavior
4. Write to the Bank 1 register, Address 0x001 = 0x00FF; depends on number of conversion stages used.
5. Read back the corresponding interrupt status register at Address 0x008, Address 0x009, or Address 0x00A. The address to be read back is determined by the interrupt output configuration, as explained in the Interrupt Output section.
6. Note that the specific registers required to be read back depend on each application. For buttons, the interrupt status registers are read back, while other sensors read data back according to the requirements of the slider or wheel algorithm. Analog Devices provides this information after the sensor board has been developed.
7. Repeat Step 5 every time $\overline{\text{INT}}$ is asserted.

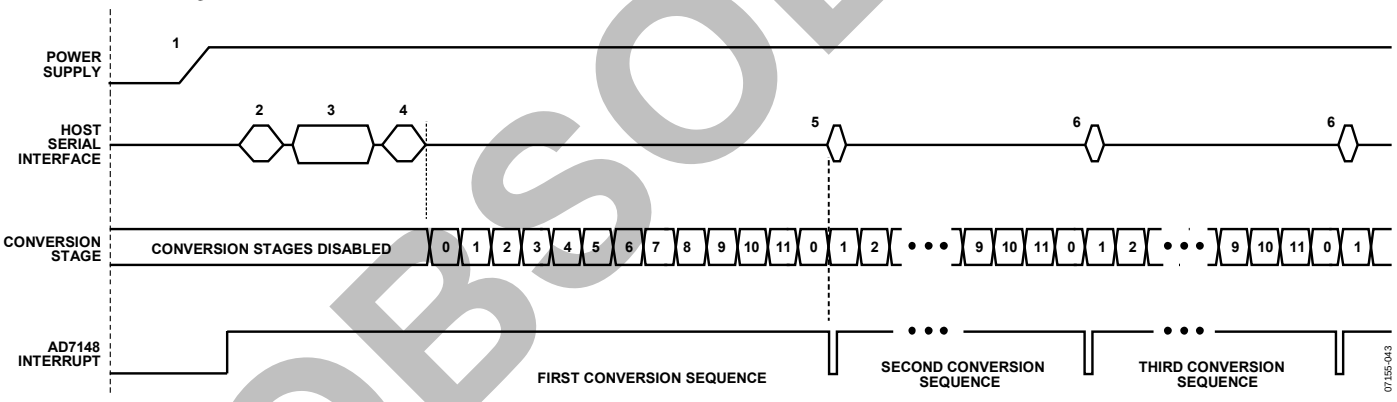


Figure 44. Recommended Start-Up Sequence

TYPICAL APPLICATION CIRCUIT

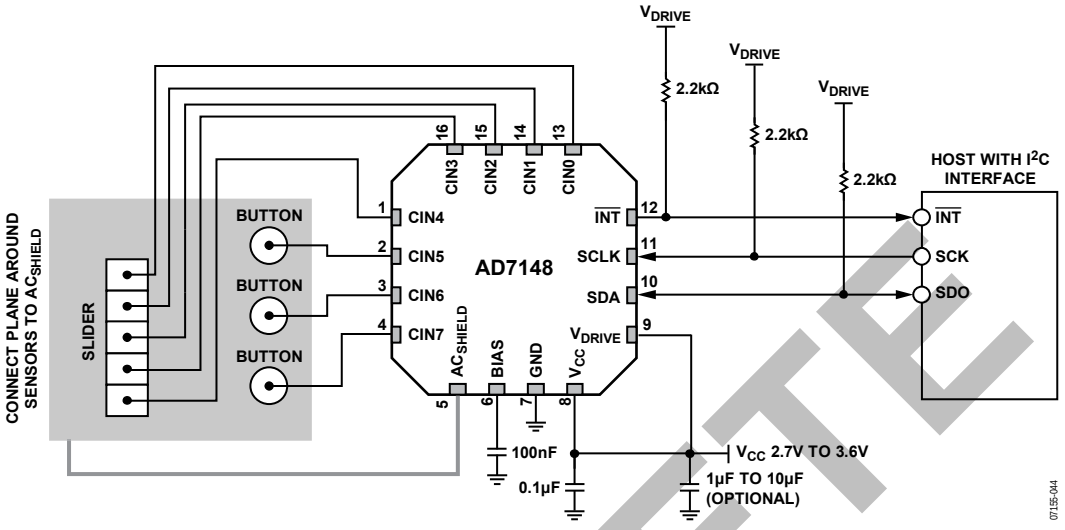


Figure 45. Typical Application Circuit

REGISTER MAP

The AD7148 address space is divided into three different register banks, referred to as Register Bank 1, Register Bank 2, and Register Bank 3. Figure 46 illustrates the division of these three banks.

Bank 1 registers contain control registers, CDC conversion control registers, interrupt enable registers, interrupt status registers, CDC 16-bit conversion data registers, device ID registers, and proximity status registers.

Bank 2 registers contain the configuration registers used for uniquely configuring the CINx inputs for each conversion stage. Initialize the Bank 2 configuration registers immediately after power-up to obtain valid CDC conversion result data.

Bank 3 registers contain the results of each conversion stage. These registers automatically update at the end of each conversion sequence. Although these registers are primarily used by the AD7148 internal data processing, they are accessible by the host processor for additional external data processing, if desired.

Default values are undefined for Bank 2 registers and Bank 3 registers until after power-up and configuration of the Bank 2 registers.

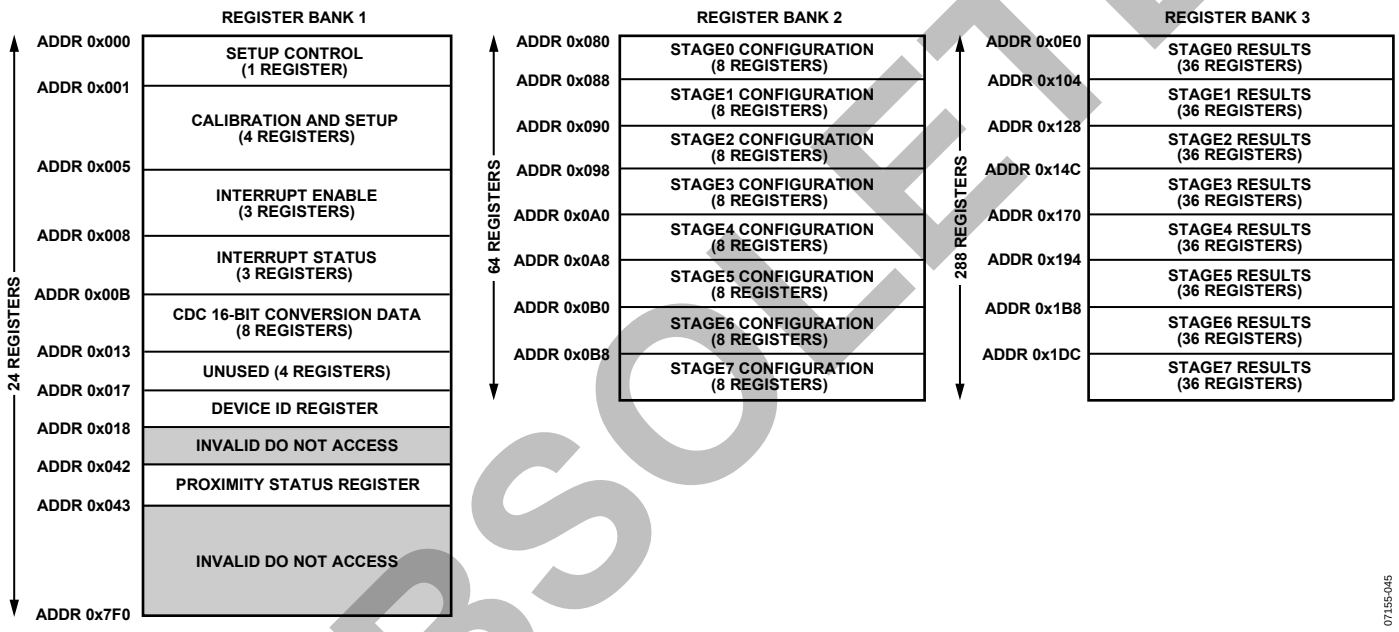


Figure 46. Layout of Bank 1 Registers, Bank 2 Registers, and Bank 3 Registers

DETAILED REGISTER DESCRIPTIONS

BANK 1 REGISTERS

All addresses and default values are expressed in hexadecimal format.

Table 17. PWR_CONTROL Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x000	[1:0]	0	R/$\overline{W}$	POWER_MODE	Operating modes 00 = full power mode (normal operation, CDC conversions approximately every 36 ms) 01 = full shutdown mode (no CDC conversions) 10 = low power mode (automatic wake up operation) 11 = full shutdown mode (no CDC conversions)
	[3:2]	0	R/$\overline{W}$	LP_CONV_DELAY	Low power mode conversion delay 00 = 200 ms 01 = 400 ms 10 = 600 ms 11 = 800 ms
	[7:4]	0	R/$\overline{W}$	SEQUENCE_STAGE_NUM	Number of stages in sequence (N + 1) 0000 = 1 conversion stage in sequence 0001 = 2 conversion stages in sequence … Maximum value = 1011 = 12 conversion stages per sequence
	[9:8]	0	R/$\overline{W}$	DECIMATION	ADC decimation factor 00 = decimate by 256 01 = decimate by 128 10 = decimate by 64 11 = decimate by 64
	[10]	0	R/$\overline{W}$	SW_RESET	Software reset control (self-clearing) 1 = resets all registers to default values
	[11]	0	R/$\overline{W}$	INT_POL	Interrupt polarity control 0 = active low 1 = active high
	[12]	0	R/$\overline{W}$		Excitation source control 0 = enable excitation source to CINx pins 1 = disable excitation source to CINx pins
	[13]	0		Unused	Set to 0
	[15:14]	0	R/$\overline{W}$	CDC_BIAS	CDC bias current control 00 = normal operation 01 = normal operation + 20% 10 = normal operation + 35% 11 = normal operation + 50%

Table 18. STAGEx_CAL_EN Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x001	[0]	0	R/$\overline{W}$	STAGE0_CAL_EN	STAGE0 calibration enable 0 = disable 1 = enable
	[1]	0	R/$\overline{W}$	STAGE1_CAL_EN	STAGE1 calibration enable 0 = disable 1 = enable
	[2]	0	R/$\overline{W}$	STAGE2_CAL_EN	STAGE2 calibration enable 0 = disable 1 = enable
	[3]	0	R/$\overline{W}$	STAGE3_CAL_EN	STAGE3 calibration enable 0 = disable 1 = enable
	[4]	0	R/$\overline{W}$	STAGE4_CAL_EN	STAGE4 calibration enable 0 = disable 1 = enable
	[5]	0	R/$\overline{W}$	STAGE5_CAL_EN	STAGE5 calibration enable 0 = disable 1 = enable
	[6]	0	R/$\overline{W}$	STAGE6_CAL_EN	STAGE6 calibration enable 0 = disable 1 = enable
	[7]	0	R/$\overline{W}$	STAGE7_CAL_EN	STAGE7 calibration enable 0 = disable 1 = enable
	[11:8]	0	R/$\overline{W}$	Unused	Set unused register bits to 0
	[13:12]	0	R/$\overline{W}$	AVG_FP_SKIP	Full power mode skip control 00 = skip 3 samples 01 = skip 7 samples 10 = skip 15 samples 11 = skip 31 samples
	[15:14]	0	R/$\overline{W}$	AVG_LP_SKIP	Low power mode skip control 00 = use all samples 01 = skip 1 sample 10 = skip 2 samples 11 = skip 3 samples

Table 19. AMB_COMP_CTRL0 Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x002	[3:0]	0	R/$\overline{W}$	FF_SKIP_CNT	Fast filter skip control (N+1) 0000 = no sequence of results is skipped 0001 = one sequence of results is skipped for every one allowed into fast FIFO 0010 = two sequences of results are skipped for every one allowed into fast FIFO 1011 = maximum value = 8 sequences of results are skipped for every one allowed into fast FIFO
	[7:4]	F	R/$\overline{W}$	FP_PROXIMITY_CNT	Calibration disable period in full power mode = FP_PROXIMITY_CNT × 16 × time taken for one conversion sequence in full power mode
	[11:8]	F	R/$\overline{W}$	LP_PROXIMITY_CNT	Calibration disable period in low power mode = LP_PROXIMITY_CNT × 4 × time taken for one conversion sequence in low power mode
	[13:12]	0	R/$\overline{W}$	PWR_DOWN_TIMEOUT	Full power to low power mode time out control 00 = 1.25 × (FP_PROXIMITY_CNT) 01 = 1.50 × (FP_PROXIMITY_CNT) 10 = 1.75 × (FP_PROXIMITY_CNT) 11 = 2.00 × (FP_PROXIMITY_CNT)
	[14]	0	R/$\overline{W}$	FORCED_CAL	Forced calibration control 0 = normal operation 1 = forces all conversion stages to recalibrate
	[15]	0	R/$\overline{W}$	CONV_RESET	Conversion reset control (self-clearing) 0 = normal operation 1 = resets the conversion sequence back to STAGE0.

Table 20. AMB_COMP_CTRL1 Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x003	[7:0]	64	R/$\overline{W}$	PROXIMITY_RECAL_LVL	Proximity recalibration level; value is multiplied by 16 to get actual recalibration level
	[13:8]	1	R/$\overline{W}$	PROXIMITY_DETECTION_RATE	Proximity detection rate; value is multiplied by 16 to get actual detection rate
	[15:14]	0	R/$\overline{W}$	SLOW_FILTER_UPDATE_LVL	Slow filter update level

Table 21. AMB_COMP_CTRL2 Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x004	[9:0]	3FF	R/$\overline{W}$	FP_PROXIMITY_RECAL	Full power mode proximity recalibration time control
	[15:10]	3F	R/$\overline{W}$	LP_PROXIMITY_RECAL	Low power mode proximity recalibration time control

Table 22. STAGEx_LOW_INT_EN Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x005	[0]	0	R/$\overline{W}$	STAGE0_LOW_INT_EN	STAGE0 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 low threshold is exceeded
	[1]	0	R/$\overline{W}$	STAGE1_LOW_INT_EN	STAGE1 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE1 low threshold is exceeded
	[2]	0	R/$\overline{W}$	STAGE2_LOW_INT_EN	STAGE2 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE2 low threshold is exceeded
	[3]	0	R/$\overline{W}$	STAGE3_LOW_INT_EN	STAGE3 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE3 low threshold is exceeded
	[4]	0	R/$\overline{W}$	STAGE4_LOW_INT_EN	STAGE4 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE4 low threshold is exceeded
	[5]	0	R/$\overline{W}$	STAGE5_LOW_INT_EN	STAGE5 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE5 low threshold is exceeded
	[6]	0	R/$\overline{W}$	STAGE6_LOW_INT_EN	STAGE6 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE6 low threshold is exceeded
	[7]	0	R/$\overline{W}$	STAGE7_LOW_INT_EN	STAGE7 low interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE7 low threshold is exceeded
	[11:8]	0		Unused	Set unused register bits to 0
	[13:12]	0	R/$\overline{W}$	GPIO_SETUP	GPIO setup 00 = disable GPIO pin 01 = configure GPIO as an input 10 = configure GPIO as an active low output 11 = configure GPIO as an active high output
	[15:14]	0	R/$\overline{W}$	GPIO_INPUT_CONFIG	GPIO input configuration 00 = triggered on negative level 01 = triggered on positive edge 10 = triggered on negative edge 11 = triggered on positive level

Table 23. STAGEx_HIGH_INT_EN Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x006	[0]	0	R/$\overline{W}$	STAGE0_HIGH_INT_EN	STAGE0 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE0 high threshold is exceeded
	[1]	0	R/$\overline{W}$	STAGE1_HIGH_INT_EN	STAGE1 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE1 high threshold is exceeded
	[2]	0	R/$\overline{W}$	STAGE2_HIGH_INT_EN	STAGE2 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE2 high threshold is exceeded
	[3]	0	R/$\overline{W}$	STAGE3_HIGH_INT_EN	STAGE3 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE3 high threshold is exceeded
	[4]	0	R/$\overline{W}$	STAGE4_HIGH_INT_EN	STAGE4 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE4 high threshold is exceeded
	[5]	0	R/$\overline{W}$	STAGE5_HIGH_INT_EN	STAGE5 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE5 high threshold is exceeded
	[6]	0	R/$\overline{W}$	STAGE6_HIGH_INT_EN	STAGE6 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE6 high threshold is exceeded
	[7]	0	R/$\overline{W}$	STAGE7_HIGH_INT_EN	STAGE7 high interrupt enable 0 = interrupt source disabled 1 = $\overline{INT}$ asserted if STAGE7 high threshold is exceeded
	[15:8]			Unused	Set unused register bits to 0

Table 24. STAGEx_COMPLETE_INT_EN Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x007	[0]	0	R/$\overline{W}$	STAGE0_COMPLETE_INT_EN	STAGE0 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE0 conversion
	[1]	0	R/$\overline{W}$	STAGE1_COMPLETE_INT_EN	STAGE1 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE1 conversion
	[2]	0	R/$\overline{W}$	STAGE2_COMPLETE_INT_EN	STAGE2 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE2 conversion
	[3]	0	R/$\overline{W}$	STAGE3_COMPLETE_INT_EN	STAGE3 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE3 conversion
	[4]	0	R/$\overline{W}$	STAGE4_COMPLETE_INT_EN	STAGE4 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE4 conversion
	[5]	0	R/$\overline{W}$	STAGE5_COMPLETE_INT_EN	STAGE5 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE5 conversion
	[6]	0	R/$\overline{W}$	STAGE6_COMPLETE_INT_EN	STAGE6 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE6 conversion
	[7]	0	R/$\overline{W}$	STAGE7_COMPLETE_INT_EN	STAGE7 conversion interrupt control 0 = interrupt source disabled 1 = $\overline{INT}$ asserted at completion of STAGE7 conversion
	[15:8]			Unused	Set unused register bits to 0

Table 25. STAGEx_LOW_LIMIT_INT Register[1]

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x008	[0]	0	R	STAGE0_LOW_LIMIT_INT	STAGE0 CDC conversion low limit interrupt result 1 = indicates STAGE0_LOW_THRESHOLD value exceeded
	[1]	0	R	STAGE1_LOW_LIMIT_INT	STAGE1 CDC conversion low limit interrupt result 1 = indicates STAGE1_LOW_THRESHOLD value exceeded
	[2]	0	R	STAGE2_LOW_LIMIT_INT	STAGE2 CDC conversion low limit interrupt result 1 = indicates STAGE2_LOW_THRESHOLD value exceeded
	[3]	0	R	STAGE3_LOW_LIMIT_INT	STAGE3 CDC conversion low limit interrupt result 1 = indicates STAGE3_LOW_THRESHOLD value exceeded
	[4]	0	R	STAGE4_LOW_LIMIT_INT	STAGE4 CDC conversion low limit interrupt result 1 = indicates STAGE4_LOW_THRESHOLD value exceeded
	[5]	0	R	STAGE5_LOW_LIMIT_INT	STAGE5 CDC conversion low limit interrupt result 1 = indicates STAGE5_LOW_THRESHOLD value exceeded
	[6]	0	R	STAGE6_LOW_LIMIT_INT	STAGE6 CDC conversion low limit interrupt result 1 = indicates STAGE6_LOW_THRESHOLD value exceeded
	[7]	0	R	STAGE7_LOW_LIMIT_INT	STAGE7 CDC conversion low limit interrupt result 1 = indicates STAGE7_LOW_THRESHOLD value exceeded
	[15:8]			Unused	Set unused register bits to 0

[1] Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 26. STAGEx_HIGH_LIMIT_INT Register[1]

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x009	[0]	0	R	STAGE0_HIGH_LIMIT_INT	STAGE0 CDC conversion high limit interrupt result 1 = indicates STAGE0_HIGH_THRESHOLD value exceeded
	[1]	0	R	STAGE1_HIGH_LIMIT_INT	STAGE1 CDC conversion high limit interrupt result 1 = indicates STAGE1_HIGH_THRESHOLD value exceeded
	[2]	0	R	STAGE2_HIGH_LIMIT_INT	Stage2 CDC conversion high limit interrupt result 1 = indicates STAGE2_HIGH_THRESHOLD value exceeded
	[3]	0	R	STAGE3_HIGH_LIMIT_INT	STAGE3 CDC conversion high limit interrupt result 1 = indicates STAGE3_HIGH_THRESHOLD value exceeded
	[4]	0	R	STAGE4_HIGH_LIMIT_INT	STAGE4 CDC conversion high limit interrupt result 1 = indicates STAGE4_HIGH_THRESHOLD value exceeded
	[5]	0	R	STAGE5_HIGH_LIMIT_INT	STAGE5 CDC conversion high limit interrupt result 1 = indicates STAGE5_HIGH_THRESHOLD value exceeded
	[6]	0	R	STAGE6_HIGH_LIMIT_INT	STAGE6 CDC conversion high limit interrupt result 1 = indicates STAGE6_HIGH_THRESHOLD value exceeded
	[7]	0	R	STAGE7_HIGH_LIMIT_INT	STAGE7 CDC conversion high limit interrupt result 1 = indicates STAGE7_HIGH_THRESHOLD value exceeded
	[15:8]			Unused	Set unused register bits to 0

[1] Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 27. STAGEx_COMPLETE_INT_STATUS Register[1]

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x00A	[0]	0	R	STAGE0_COMPLETE_INT_STATUS	STAGE0 conversion complete register interrupt status 1 = indicates STAGE0 conversion completed
	[1]	0	R	STAGE1_COMPLETE_INT_STATUS	STAGE1 conversion complete register interrupt status 1 = indicates STAGE1 conversion completed
	[2]	0	R	STAGE2_COMPLETE_INT_STATUS	STAGE2 conversion complete register interrupt status 1 = indicates STAGE2 conversion completed
	[3]	0	R	STAGE3_COMPLETE_INT_STATUS	STAGE3 conversion complete register interrupt status 1 = indicates STAGE3 conversion completed
	[4]	0	R	STAGE4_COMPLETE_INT_STATUS	STAGE4 conversion complete register interrupt status 1 = indicates STAGE4 conversion completed
	[5]	0	R	STAGE5_COMPLETE_INT_STATUS	STAGE5 conversion complete register interrupt status 1 = indicates STAGE5 conversion completed
	[6]	0	R	STAGE6_COMPLETE_INT_STATUS	STAGE6 conversion complete register interrupt status 1 = indicates STAGE6 conversion completed
	[7]	0	R	STAGE7_COMPLETE_INT_STATUS	STAGE7 conversion complete register interrupt status 1 = indicates STAGE7 conversion completed
	[15:8]			Unused	Set unused register bits to 0

[1] Registers self-clear to 0 after readback, provided that the limits are not exceeded.

Table 28. CDC 16-Bit Conversion Data Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x00B	[15:0]	0	R	CDC_RESULT_S0	STAGE0 CDC 16-bit conversion data
0x00C	[15:0]	0	R	CDC_RESULT_S1	STAGE1 CDC 16-bit conversion data
0x00D	[15:0]	0	R	CDC_RESULT_S2	STAGE2 CDC 16-bit conversion data
0x00E	[15:0]	0	R	CDC_RESULT_S3	STAGE3 CDC 16-bit conversion data
0x00F	[15:0]	0	R	CDC_RESULT_S4	STAGE4 CDC 16-bit conversion data
0x010	[15:0]	0	R	CDC_RESULT_S5	STAGE5 CDC 16-bit conversion data
0x011	[15:0]	0	R	CDC_RESULT_S6	STAGE6 CDC 16-bit conversion data
0x012	[15:0]	0	R	CDC_RESULT_S7	STAGE7 CDC 16-bit conversion data

Table 29. Device ID Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x017	[3:0]	0	R	REVISION_CODE	AD7148 revision code
	[15:4]	148	R	DEVID	AD7148 device ID = 0x148

Table 30. Proximity Status Register

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x042	[0]	0	R	STAGE0_PROXIMITY_STATUS	STAGE0 proximity status register 1 = indicates proximity has been detected on STAGE0
	[1]	0	R	STAGE1_PROXIMITY_STATUS	STAGE1 proximity status register 1 = indicates proximity has been detected on STAGE1
	[2]	0	R	STAGE2_PROXIMITY_STATUS	STAGE2 proximity status register 1 = indicates proximity has been detected on STAGE2
	[3]	0	R	STAGE3_PROXIMITY_STATUS	STAGE3 proximity status register 1 = indicates proximity has been detected on STAGE3
	[4]	0	R	STAGE4_PROXIMITY_STATUS	STAGE4 proximity status register 1 = indicates proximity has been detected on STAGE4
	[5]	0	R	STAGE5_PROXIMITY_STATUS	STAGE5 proximity status register 1 = indicates proximity has been detected on STAGE5
	[6]	0	R	STAGE6_PROXIMITY_STATUS	STAGE6 proximity status register 1 = indicates proximity has been detected on STAGE6
	[7]	0	R	STAGE7_PROXIMITY_STATUS	STAGE7 proximity status register 1 = indicates proximity has been detected on STAGE7
	[15:8]			Unused	Set unused register bits to 0

BANK 2 REGISTERS

All address values are expressed in hexadecimal format.

Table 31. STAGE0 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x080	[15:0]	X	R/$\overline{W}$	STAGE0_CONNECTION_SETUP[6:0]	STAGE0 CIN[6:0] connection setup (see Table 39)
0x081	[15:0]	X	R/$\overline{W}$	STAGE0_CONNECTION_SETUP[7]	STAGE0 CIN7 connection setup (see Table 40)
0x082	[15:0]	X	R/$\overline{W}$	STAGE0_AFE_OFFSET	STAGE0 AFE offset control (see Table 41)
0x083	[15:0]	X	R/$\overline{W}$	STAGE0_SENSITIVITY	STAGE0 sensitivity control (see Table 42)
0x084	[15:0]	X	R/$\overline{W}$	STAGE0_OFFSET_LOW	STAGE0 initial offset low value
0x085	[15:0]	X	R/$\overline{W}$	STAGE0_OFFSET_HIGH	STAGE0 initial offset high value
0x086	[15:0]	X	R/$\overline{W}$	STAGE0_OFFSET_HIGH_CLAMP	STAGE0 offset high clamp value
0x087	[15:0]	X	R/$\overline{W}$	STAGE0_ OFFSET_LOW_CLAMP	STAGE0 offset low clamp value

Table 32. STAGE1 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x088	[15:0]	X	R/$\overline{W}$	STAGE1_CONNECTION_SETUP[6:0]	STAGE1 CIN[6:0] connection setup (see Table 39)
0x089	[15:0]	X	R/$\overline{W}$	STAGE1_CONNECTION_SETUP[7]	STAGE1 CIN7 connection setup (see Table 40)
0x08A	[15:0]	X	R/$\overline{W}$	STAGE1_AFE_OFFSET	STAGE1 AFE offset control (see Table 41)
0x08B	[15:0]	X	R/$\overline{W}$	STAGE1_SENSITIVITY	STAGE1 sensitivity control (see Table 42)
0x08C	[15:0]	X	R/$\overline{W}$	STAGE1_OFFSET_LOW	STAGE1 initial offset low value
0x08D	[15:0]	X	R/$\overline{W}$	STAGE1_OFFSET_HIGH	STAGE1 initial offset high value
0x08E	[15:0]	X	R/$\overline{W}$	STAGE1_OFFSET_HIGH_CLAMP	STAGE1 offset high clamp value
0x08F	[15:0]	X	R/$\overline{W}$	STAGE1_OFFSET_LOW_CLAMP	STAGE1 offset low clamp value

Table 33. STAGE2 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x090	[15:0]	X	R/$\overline{W}$	STAGE2_CONNECTION_SETUP[6:0]	STAGE2 CIN[6:0] connection setup (see Table 39)
0x091	[15:0]	X	R/$\overline{W}$	STAGE2_CONNECTION_SETUP[7]	STAGE2 CIN7 connection setup (see Table 40)
0x092	[15:0]	X	R/$\overline{W}$	STAGE2_AFE_OFFSET	STAGE2 AFE offset control (see Table 41)
0x093	[15:0]	X	R/$\overline{W}$	STAGE2_SENSITIVITY	STAGE2 sensitivity control (see Table 42)
0x094	[15:0]	X	R/$\overline{W}$	STAGE2_OFFSET_LOW	STAGE2 initial offset low value
0x095	[15:0]	X	R/$\overline{W}$	STAGE2_OFFSET_HIGH	STAGE2 initial offset high value
0x096	[15:0]	X	R/$\overline{W}$	STAGE2_OFFSET_HIGH_CLAMP	STAGE2 offset high clamp value
0x097	[15:0]	X	R/$\overline{W}$	STAGE2_OFFSET_LOW_CLAMP	STAGE2 offset low clamp value

Table 34. STAGE3 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x098	[15:0]	X	R/$\overline{W}$	STAGE3_CONNECTION_SETUP[6:0]	STAGE3 CIN[6:0] connection setup (see Table 39
0x099	[15:0]	X	R/$\overline{W}$	STAGE3_CONNECTION_SETUP[7]	STAGE3 CIN7 connection setup (see Table 40)
0x09A	[15:0]	X	R/$\overline{W}$	STAGE3_AFE_OFFSET	STAGE3 AFE offset control (see Table 41)
0x09B	[15:0]	X	R/$\overline{W}$	STAGE3_SENSITIVITY	STAGE3 sensitivity control (see Table 42)
0x09C	[15:0]	X	R/$\overline{W}$	STAGE3_OFFSET_LOW	STAGE3 initial offset low value
0x09D	[15:0]	X	R/$\overline{W}$	STAGE3_OFFSET_HIGH	STAGE3 initial offset high value
0x09E	[15:0]	X	R/$\overline{W}$	STAGE3_OFFSET_HIGH_CLAMP	STAGE3 offset high clamp value
0x09F	[15:0]	X	R/$\overline{W}$	STAGE3_OFFSET_LOW_CLAMP	STAGE3 offset low clamp value

Table 35. STAGE4 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x0A0	[15:0]	X	R/$\overline{W}$	STAGE4_CONNECTION_SETUP[6:0]	STAGE4 CIN[6:0] connection setup (see Table 39)
0x0A1	[15:0]	X	R/$\overline{W}$	STAGE4_CONNECTION_SETUP[7]	STAGE4 CIN7 connection setup (see Table 40)
0x0A2	[15:0]	X	R/$\overline{W}$	STAGE4_AFE_OFFSET	STAGE4 AFE offset control (see Table 41)
0x0A3	[15:0]	X	R/$\overline{W}$	STAGE4_SENSITIVITY	STAGE4 sensitivity control (see Table 42)
0x0A4	[15:0]	X	R/$\overline{W}$	STAGE4_OFFSET_LOW	STAGE4 initial offset low value
0x0A5	[15:0]	X	R/$\overline{W}$	STAGE4_OFFSET_HIGH	STAGE4 initial offset high value
0x0A6	[15:0]	X	R/$\overline{W}$	STAGE4_OFFSET_HIGH_CLAMP	STAGE4 offset high clamp value
0x0A7	[15:0]	X	R/$\overline{W}$	STAGE4_OFFSET_LOW_CLAMP	STAGE4 offset low clamp value

Table 36. STAGE5 Configuration Registers

Address	Data Bit	Default Value	Type	Name	Description
0x0A8	[15:0]	X	R/$\overline{W}$	STAGE5_CONNECTION_SETUP[6:0]	STAGE5 CIN[6:0] connection setup (see Table 39)
0x0A9	[15:0]	X	R/$\overline{W}$	STAGE5_CONNECTION_SETUP[7]	STAGE5 CIN7 connection setup (see Table 40)
0x0AA	[15:0]	X	R/$\overline{W}$	STAGE5_AFE_OFFSET	STAGE5 AFE offset control (see Table 41)
0x0AB	[15:0]	X	R/$\overline{W}$	STAGE5_SENSITIVITY	STAGE5 sensitivity control (see Table 42)
0x0AC	[15:0]	X	R/$\overline{W}$	STAGE5_OFFSET_LOW	STAGE5 initial offset low value
0x0AD	[15:0]	X	R/$\overline{W}$	STAGE5_OFFSET_HIGH	STAGE5 initial offset high value
0x0AE	[15:0]	X	R/$\overline{W}$	STAGE5_OFFSET_HIGH_CLAMP	STAGE5 offset high clamp value
0x0AF	[15:0]	X	R/$\overline{W}$	STAGE5_OFFSET_LOW_CLAMP	STAGE5 offset low clamp value

Table 37. STAGE6 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x0B0	[15:0]	X	R/$\overline{W}$	STAGE6_CONNECTION_SETUP[6:0]	STAGE6 CIN[6:0] connection setup (see Table 39)
0x0B1	[15:0]	X	R/$\overline{W}$	STAGE6_CONNECTION_SETUP[7]	STAGE6 CIN7 connection setup (see Table 40)
0x0B2	[15:0]	X	R/$\overline{W}$	STAGE6_AFE_OFFSET	STAGE6 AFE offset control (see Table 41)
0x0B3	[15:0]	X	R/$\overline{W}$	STAGE6_SENSITIVITY	STAGE6 sensitivity control (see Table 42)
0x0B4	[15:0]	X	R/$\overline{W}$	STAGE6_OFFSET_LOW	STAGE6 initial offset low value
0x0B5	[15:0]	X	R/$\overline{W}$	STAGE6_OFFSET_HIGH	STAGE6 initial offset high value
0x0B6	[15:0]	X	R/$\overline{W}$	STAGE6_OFFSET_HIGH_CLAMP	STAGE6 offset high clamp value
0x0B7	[15:0]	X	R/$\overline{W}$	STAGE6_OFFSET_LOW_CLAMP	STAGE6 offset low clamp value

Table 38. STAGE7 Configuration Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x0B8	[15:0]	X	R/W	STAGE7_CONNECTION_SETUP[6:0]	STAGE7 CIN[6:0] connection setup (see Table 39)
0x0B9	[15:0]	X	R/$\overline{W}$	STAGE7_CONNECTION_SETUP[7]	STAGE7 CIN7 connection setup (see Table 40)
0x0BA	[15:0]	X	R/$\overline{W}$	STAGE7_AFE_OFFSET	STAGE7 AFE offset control (see Table 41)
0x0BB	[15:0]	X	R/$\overline{W}$	STAGE7_SENSITIVITY	STAGE7 sensitivity control (see Table 42)
0x0BC	[15:0]	X	R/$\overline{W}$	STAGE7_OFFSET_LOW	STAGE7 initial offset low value
0x0BD	[15:0]	X	R/$\overline{W}$	STAGE7_OFFSET_HIGH	STAGE7 initial offset high value
0x0BE	[15:0]	X	R/$\overline{W}$	STAGE7_OFFSET_HIGH_CLAMP	STAGE7 offset high clamp value
0x0BF	[15:0]	X	R/$\overline{W}$	STAGE7_OFFSET_LOW_CLAMP	STAGE7 offset low clamp value

Table 39. STAGEx Detailed CIN[0:6] Connection Setup Description (x = 0 to 7)

Data Bit	Default Value	Type	Mnemonic	Description
[1:0]	X	R/$\overline{W}$	CIN0_CONNECTION_SETUP	CIN0 connection setup 00 = CIN0 not connected to CDC inputs 01 = CIN0 connected to CDC negative input 10 = CIN0 connected to CDC positive input 11 = CIN0 connected to BIAS (connect unused CINx inputs)
[3:2]	X	R/$\overline{W}$	CIN1_CONNECTION_SETUP	CIN1 connection setup 00 = CIN1 not connected to CDC inputs 01 = CIN1 connected to CDC negative input 10 = CIN1 connected to CDC positive input 11 = CIN1 connected to BIAS (connect unused CINx inputs)
[5:4]	X	R/$\overline{W}$	CIN2_CONNECTION_SETUP	CIN2 connection setup 00 = CIN2 not connected to CDC inputs 01 = CIN2 connected to CDC negative input 10 = CIN2 connected to CDC positive input 11 = CIN2 connected to BIAS (connect unused CINx inputs)
[7:6]	X	R/$\overline{W}$	CIN3_CONNECTION_SETUP	CIN3 connection setup 00 = CIN3 not connected to CDC inputs 01 = CIN3 connected to CDC negative input 10 = CIN3 connected to CDC positive input 11 = CIN3 connected to BIAS (connect unused CINx inputs)
[9:8]	X	R/$\overline{W}$	CIN4_CONNECTION_SETUP	CIN4 connection setup 00 = CIN4 not connected to CDC inputs 01 = CIN4 connected to CDC negative input 10 = CIN4 connected to CDC positive input 11 = CIN4 connected to BIAS (connect unused CINx inputs)
[11:10]	X	R/$\overline{W}$	CIN5_CONNECTION_SETUP	CIN5 connection setup 00 = CIN5 not connected to CDC inputs 01 = CIN5 connected to CDC negative input 10 = CIN5 connected to CDC positive input 11 = CIN5 connected to BIAS (connect unused CINx inputs)
[13:12]	X	R/$\overline{W}$	CIN6_CONNECTION_SETUP	CIN6 connection setup 00 = CIN6 not connected to CDC inputs 01 = CIN6 connected to CDC negative input 10 = CIN6 connected to CDC positive input 11 = CIN6 connected to BIAS (connect unused CINx inputs)
[15:14]	X		Unused	Set unused register bits to 0

Table 40. STAGEx Detailed CIN7 Connection Setup Description (x = 0 to 7)

Data Bit	Default Value	Type	Mnemonic	Description
[1:0]	X	R/$\overline{W}$	CIN7_CONNECTION_SETUP	CIN7 connection setup 00 = CIN7 not connected to CDC inputs 01 = CIN7 connected to CDC negative input 10 = CIN7 connected to CDC positive input 11 = CIN7 connected to BIAS (connect unused CINx inputs)
[12:2]	X		Unused	Set unused register bits to 0
[13:12]	X	R/$\overline{W}$	SE_CONNECTION_SETUP	Single-ended measurement connection setup 00 = do not use 01 = use when one CIN is connected to CDC positive input, single-ended measurements only 10 = use when one CIN is connected to CDC negative input, single-ended measurements only 11 = differential connection to CDC
[14]	X	R/$\overline{W}$	NEG_AFE_OFFSET_DISABLE	Negative AFE offset enable control 0 = enable 1 = disable
[15]	X	R/$\overline{W}$	POS_AFE_OFFSET_DISABLE	Positive AFE offset enable control 0 = enable 1 = disable

Table 41. STAGEx Detailed Offset Control Description (x = 0 to 7)

Data Bit	Default Value	Type	Mnemonic	Description
[5:0]	X	R/$\overline{W}$	NEG_AFE_OFFSET	Negative AFE offset setting (20 pF range) 1 LSB value = 0.32 pF of offset
[6]	X		Unused	Set to 0
[7]	X	R/$\overline{W}$	NEG_AFE_OFFSET_SWAP	Negative AFE offset swap control 0 = NEG_AFE_OFFSET applied to CDC negative input 1 = NEG_AFE_OFFSET applied to CDC positive input
[13:8]	X	R/$\overline{W}$	POS_AFE_OFFSET	Positive AFE offset setting (20 pF range) 1 LSB value = 0.32 pF of offset
[14]	X		Unused	Set to 0
[15]	X	R/$\overline{W}$	POS_AFE_OFFSET_SWAP	Positive AFE offset swap control 0 = POS_AFE_OFFSET applied to CDC positive input 1 = POS_AFE_OFFSET applied to CDC negative input

Table 42. STAGEx Detailed Sensitivity Control Description (x = 0 to 7)

Data Bit	Default Value	Type	Mnemonic	Description
[3:0]	X	R/$\overline{W}$	NEG_THRESHOLD_SENSITIVITY	Negative threshold sensitivity control 0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08% 0100 = 43.79%, 0101 = 48.48%, 0110 = 53.15% 0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22% 1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28% 1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32%
[6:4]	X	R/$\overline{W}$	NEG_PEAK_DETECT	Negative peak detect setting 000 = 40% level, 001 = 50% level, 010 = 60% level 011 = 70% level, 100 = 80% level, 101 = 90% level
[7]	X		Unused	Set to 0
[11:8]	X	R/$\overline{W}$	POS_THRESHOLD_SENSITIVITY	Positive threshold sensitivity control 0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08% 0100 = 43.79%, 0101 = 48.48%, 0110 = 53.15% 0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22% 1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28% 1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32%
[14:12]	X	R/$\overline{W}$	POS_PEAK_DETECT	Positive peak detect setting 000 = 40% level, 001 = 50% level, 010 = 60% level 011 = 70% level, 100 = 80% level, 101 = 90% level
[15]	X		Unused	Set to 0

BANK 3 REGISTERS

All address values are expressed in hexadecimal format.

Table 43. STAGE0 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x0E0	[15:0]	X	R/$\overline{W}$	STAGE0_CONV_DATA	STAGE0 CDC 16-bit conversion data (copy of data in CDC_RESULT_S0 register)
0x0E1	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD0	STAGE0 fast FIFO WORD0
0x0E2	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD1	STAGE0 fast FIFO WORD1
0x0E3	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD2	STAGE0 fast FIFO WORD2
0x0E4	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD3	STAGE0 fast FIFO WORD3
0x0E5	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD4	STAGE0 fast FIFO WORD4
0x0E6	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD5	STAGE0 fast FIFO WORD5
0x0E7	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD6	STAGE0 fast FIFO WORD6
0x0E8	[15:0]	X	R/$\overline{W}$	STAGE0_FF_WORD7	STAGE0 fast FIFO WORD7
0x0E9	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD0	STAGE0 slow FIFO WORD0
0x0EA	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD1	STAGE0 slow FIFO WORD1
0x0EB	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD2	STAGE0 slow FIFO WORD2
0x0EC	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD3	STAGE0 slow FIFO WORD3
0x0ED	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD4	STAGE0 slow FIFO WORD4
0x0EE	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD5	STAGE0 slow FIFO WORD5
0x0EF	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD6	STAGE0 slow FIFO WORD6
0x0F0	[15:0]	X	R/$\overline{W}$	STAGE0_SF_WORD7	STAGE0 slow FIFO WORD7
0x0F1	[15:0]	X	R/$\overline{W}$	STAGE0_SF_AMBIENT	STAGE0 slow FIFO ambient value
0x0F2	[15:0]	X	R/$\overline{W}$	STAGE0_FF_AVG	STAGE0 fast FIFO average value
0x0F3	[15:0]	X	R/$\overline{W}$	STAGE0_PEAK_DETECT_WORD0	STAGE0 peak FIFO WORD0 value
0x0F4	[15:0]	X	R/$\overline{W}$	STAGE0_PEAK_DETECT_WORD1	STAGE0 peak FIFO WORD1 value
0x0F5	[15:0]	X	R/$\overline{W}$	STAGE0_MAX_WORD0	STAGE0 maximum value FIFO WORD0
0x0F6	[15:0]	X	R/$\overline{W}$	STAGE0_MAX_WORD1	STAGE0 maximum value FIFO WORD1
0x0F7	[15:0]	X	R/$\overline{W}$	STAGE0_MAX_WORD2	STAGE0 maximum value FIFO WORD2
0x0F8	[15:0]	X	R/$\overline{W}$	STAGE0_MAX_WORD3	STAGE0 maximum value FIFO WORD3
0x0F9	[15:0]	X	R/$\overline{W}$	STAGE0_MAX_AVG	STAGE0 average maximum FIFO value
0x0FA	[15:0]	X	R/$\overline{W}$	STAGE0_HIGH_THRESHOLD	STAGE0 high threshold value
0x0FB	[15:0]	X	R/$\overline{W}$	STAGE0_MAX_TEMP	STAGE0 temporary maximum value
0x0FC	[15:0]	X	R/$\overline{W}$	STAGE0_MIN_WORD0	STAGE0 minimum value FIFO WORD0
0x0FD	[15:0]	X	R/$\overline{W}$	STAGE0_MIN_WORD1	STAGE0 minimum value FIFO WORD1
0x0FE	[15:0]	X	R/$\overline{W}$	STAGE0_MIN_WORD2	STAGE0 minimum value FIFO WORD2
0x0FF	[15:0]	X	R/$\overline{W}$	STAGE0_MIN_WORD3	STAGE0 minimum value FIFO WORD3
0x100	[15:0]	X	R/$\overline{W}$	STAGE0_MIN_AVG	STAGE0 average minimum FIFO value
0x101	[15:0]	X	R/$\overline{W}$	STAGE0_LOW_THRESHOLD	STAGE0 low threshold value
0x102	[15:0]	X	R/$\overline{W}$	STAGE0_MIN_TEMP	STAGE0 temporary minimum value
0x103	[15:0]	X		Unused	Set unused register bits to 0

Table 44. STAGE1 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x104	[15:0]	X	R/W	STAGE1_CONV_DATA	STAGE1 CDC 16-bit conversion data (copy of data in CDC_RESULT_S1 register)
0x105	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD0	STAGE1 fast FIFO WORD0
0x106	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD1	STAGE1 fast FIFO WORD1
0x107	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD2	STAGE1 fast FIFO WORD2
0x108	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD3	STAGE1 fast FIFO WORD3
0x109	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD4	STAGE1 fast FIFO WORD4
0x10A	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD5	STAGE1 fast FIFO WORD5
0x10B	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD6	STAGE1 fast FIFO WORD6
0x10C	[15:0]	X	R/$\overline{W}$	STAGE1_FF_WORD7	STAGE1 fast FIFO WORD7
0x10D	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD0	STAGE1 slow FIFO WORD0
0x10E	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD1	STAGE1 slow FIFO WORD1
0x10F	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD2	STAGE1 slow FIFO WORD2
0x110	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD3	STAGE1 slow FIFO WORD3
0x111	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD4	STAGE1 slow FIFO WORD4
0x112	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD5	STAGE1 slow FIFO WORD5
0x113	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD6	STAGE1 slow FIFO WORD6
0x114	[15:0]	X	R/$\overline{W}$	STAGE1_SF_WORD7	STAGE1 slow FIFO WORD7
0x115	[15:0]	X	R/$\overline{W}$	STAGE1_SF_AMBIENT	STAGE1 slow FIFO ambient value
0x116	[15:0]	X	R/$\overline{W}$	STAGE1_FF_AVG	STAGE1 fast FIFO average value
0x117	[15:0]	X	R/$\overline{W}$	STAGE1_CDC_WORD0	STAGE1 CDC FIFO WORD0
0x118	[15:0]	X	R/$\overline{W}$	STAGE1_CDC_WORD1	STAGE1 CDC FIFO WORD1
0x119	[15:0]	X	R/$\overline{W}$	STAGE1_MAX_WORD0	STAGE1 maximum value FIFO WORD0
0x11A	[15:0]	X	R/$\overline{W}$	STAGE1_MAX_WORD1	STAGE1 maximum value FIFO WORD1
0x11B	[15:0]	X	R/$\overline{W}$	STAGE1_MAX_WORD2	STAGE1 maximum value FIFO WORD2
0x11C	[15:0]	X	R/$\overline{W}$	STAGE1_MAX_WORD3	STAGE1 maximum value FIFO WORD3
0x11D	[15:0]	X	R/$\overline{W}$	STAGE1_MAX_AVG	STAGE1 average maximum FIFO value
0x11E	[15:0]	X	R/$\overline{W}$	STAGE1_HIGH_THRESHOLD	STAGE1 high threshold value
0x11F	[15:0]	X	R/$\overline{W}$	STAGE1_MAX_TEMP	STAGE1 temporary maximum value
0x120	[15:0]	X	R/$\overline{W}$	STAGE1_MIN_WORD0	STAGE1 minimum value FIFO WORD0
0x121	[15:0]	X	R/$\overline{W}$	STAGE1_MIN_WORD1	STAGE1 minimum value FIFO WORD1
0x122	[15:0]	X	R/$\overline{W}$	STAGE1_MIN_WORD2	STAGE1 minimum value FIFO WORD2
0x123	[15:0]	X	R/$\overline{W}$	STAGE1_MIN_WORD3	STAGE1 minimum value FIFO WORD3
0x124	[15:0]	X	R/$\overline{W}$	STAGE1_MIN_AVG	STAGE1 average minimum FIFO value
0x125	[15:0]	X	R/$\overline{W}$	STAGE1_LOW_THRESHOLD	STAGE1 low threshold value
0x126	[15:0]	X	R/$\overline{W}$	STAGE1_MIN_TEMP	STAGE1 temporary minimum value
0x127	[15:0]	X		Unused	Set unused register bits to 0

Table 45. STAGE2 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x128	[15:0]	X	R/$\overline{W}$	STAGE2_CONV_DATA	STAGE2 CDC 16-bit conversion data (copy of data in CDC_RESULT_S2 register)
0x129	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD0	STAGE2 fast FIFO WORD0
0x12A	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD1	STAGE2 fast FIFO WORD1
0x12B	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD2	STAGE2 fast FIFO WORD2
0x12C	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD3	STAGE2 fast FIFO WORD3
0x12D	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD4	STAGE2 fast FIFO WORD4
0x12E	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD5	STAGE2 fast FIFO WORD5
0x12F	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD6	STAGE2 fast FIFO WORD6
0x130	[15:0]	X	R/$\overline{W}$	STAGE2_FF_WORD7	STAGE2 fast FIFO WORD7
0x131	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD0	STAGE2 slow FIFO WORD0
0x132	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD1	STAGE2 slow FIFO WORD1
0x133	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD2	STAGE2 slow FIFO WORD2
0x134	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD3	STAGE2 slow FIFO WORD3
0x135	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD4	STAGE2 slow FIFO WORD4
0x136	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD5	STAGE2 slow FIFO WORD5
0x137	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD6	STAGE2 slow FIFO WORD6
0x138	[15:0]	X	R/$\overline{W}$	STAGE2_SF_WORD7	STAGE2 slow FIFO WORD7
0x139	[15:0]	X	R/$\overline{W}$	STAGE2_SF_AMBIENT	STAGE2 slow FIFO ambient value
0x13A	[15:0]	X	R/$\overline{W}$	STAGE2_FF_AVG	STAGE2 fast FIFO average value
0x13B	[15:0]	X	R/$\overline{W}$	STAGE2_CDC_WORD0	STAGE2 CDC FIFO WORD0
0x13C	[15:0]	X	R/$\overline{W}$	STAGE2_CDC_WORD1	STAGE2 CDC FIFO WORD1
0x13D	[15:0]	X	R/$\overline{W}$	STAGE2_MAX_WORD0	STAGE2 maximum value FIFO WORD0
0x13E	[15:0]	X	R/$\overline{W}$	STAGE2_MAX_WORD1	STAGE2 maximum value FIFO WORD1
0x13F	[15:0]	X	R/$\overline{W}$	STAGE2_MAX_WORD2	STAGE2 maximum value FIFO WORD2
0x140	[15:0]	X	R/$\overline{W}$	STAGE2_MAX_WORD3	STAGE2 maximum value FIFO WORD3
0x141	[15:0]	X	R/$\overline{W}$	STAGE2_MAX_AVG	STAGE2 average maximum FIFO value
0x142	[15:0]	X	R/$\overline{W}$	STAGE2_HIGH_THRESHOLD	STAGE2 high threshold value
0x143	[15:0]	X	R/$\overline{W}$	STAGE2_MAX_TEMP	STAGE2 temporary maximum value
0x144	[15:0]	X	R/$\overline{W}$	STAGE2_MIN_WORD0	STAGE2 minimum value FIFO WORD0
0x145	[15:0]	X	R/$\overline{W}$	STAGE2_MIN_WORD1	STAGE2 minimum value FIFO WORD1
0x146	[15:0]	X	R/$\overline{W}$	STAGE2_MIN_WORD2	STAGE2 minimum value FIFO WORD2
0x148	[15:0]	X	R/$\overline{W}$	STAGE2_MIN_WORD3	STAGE2 minimum value FIFO WORD3
0x148	[15:0]	X	R/$\overline{W}$	STAGE2_MIN_AVG	STAGE2 average minimum FIFO value
0x149	[15:0]	X	R/$\overline{W}$	STAGE2_LOW_THRESHOLD	STAGE2 low threshold value
0x14A	[15:0]	X	R/$\overline{W}$	STAGE2_MIN_TEMP	STAGE2 temporary minimum value
0x14B	[15:0]	X		Unused	Set unused register bits to 0

Table 46. STAGE3 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x14C	[15:0]	X	R/$\overline{W}$	STAGE3_CONV_DATA	STAGE3 CDC 16-bit conversion data (copy of data in CDC_RESULT_S3 register)
0x14D	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD0	STAGE3 fast FIFO WORD0
0x14E	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD1	STAGE3 fast FIFO WORD1
0x14F	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD2	STAGE3 fast FIFO WORD2
0x150	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD3	STAGE3 fast FIFO WORD3
0x151	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD4	STAGE3 fast FIFO WORD4
0x152	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD5	STAGE3 fast FIFO WORD5
0x153	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD6	STAGE3 fast FIFO WORD6
0x154	[15:0]	X	R/$\overline{W}$	STAGE3_FF_WORD7	STAGE3 fast FIFO WORD7
0x155	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD0	STAGE3 slow FIFO WORD0
0x156	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD1	STAGE3 slow FIFO WORD1
0x157	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD2	STAGE3 slow FIFO WORD2
0x158	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD3	STAGE3 slow FIFO WORD3
0x159	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD4	STAGE3 slow FIFO WORD4
0x15A	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD5	STAGE3 slow FIFO WORD5
0x15B	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD6	STAGE3 slow FIFO WORD6
0x15C	[15:0]	X	R/$\overline{W}$	STAGE3_SF_WORD7	STAGE3 slow FIFO WORD7
0x15D	[15:0]	X	R/$\overline{W}$	STAGE3_SF_AMBIENT	STAGE3 slow FIFO ambient value
0x15E	[15:0]	X	R/$\overline{W}$	STAGE3_FF_AVG	STAGE3 fast FIFO average value
0x15F	[15:0]	X	R/$\overline{W}$	STAGE3_CDC_WORD0	STAGE3 CDC FIFO WORD0
0x160	[15:0]	X	R/$\overline{W}$	STAGE3_CDC_WORD1	STAGE3 CDC FIFO WORD1
0x161	[15:0]	X	R/$\overline{W}$	STAGE3_MAX_WORD0	STAGE3 maximum value FIFO WORD0
0x162	[15:0]	X	R/$\overline{W}$	STAGE3_MAX_WORD1	STAGE3 maximum value FIFO WORD1
0x163	[15:0]	X	R/$\overline{W}$	STAGE3_MAX_WORD2	STAGE3 maximum value FIFO WORD2
0x164	[15:0]	X	R/$\overline{W}$	STAGE3_MAX_WORD3	STAGE3 maximum value FIFO WORD3
0x165	[15:0]	X	R/$\overline{W}$	STAGE3_MAX_AVG	STAGE3 average maximum FIFO value
0x166	[15:0]	X	R/$\overline{W}$	STAGE3_HIGH_THRESHOLD	STAGE3 high threshold value
0x167	[15:0]	X	R/$\overline{W}$	STAGE3_MAX_TEMP	STAGE3 temporary maximum value
0x168	[15:0]	X	R/$\overline{W}$	STAGE3_MIN_WORD0	STAGE3 minimum value FIFO WORD0
0x169	[15:0]	X	R/$\overline{W}$	STAGE3_MIN_WORD1	STAGE3 minimum value FIFO WORD1
0x16A	[15:0]	X	R/$\overline{W}$	STAGE3_MIN_WORD2	STAGE3 minimum value FIFO WORD2
0x16B	[15:0]	X	R/$\overline{W}$	STAGE3_MIN_WORD3	STAGE3 minimum value FIFO WORD3
0x16C	[15:0]	X	R/$\overline{W}$	STAGE3_MIN_AVG	STAGE3 average minimum FIFO value
0x16D	[15:0]	X	R/$\overline{W}$	STAGE3_LOW_THRESHOLD	STAGE3 low threshold value
0x16E	[15:0]	X	R/$\overline{W}$	STAGE3_MIN_TEMP	STAGE3 temporary minimum value
0x16F	[15:0]	X		Unused	Set unused register bits to 0

Table 47. STAGE4 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x170	[15:0]	X	R/$\overline{W}$	STAGE4_CONV_DATA	STAGE4 CDC 16-bit conversion data (copy of data in CDC_RESULT_S4 register)
0x171	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD0	STAGE4 fast FIFO WORD0
0x172	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD1	STAGE4 fast FIFO WORD1
0x173	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD2	STAGE4 fast FIFO WORD2
0x174	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD3	STAGE4 fast FIFO WORD3
0x175	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD4	STAGE4 fast FIFO WORD4
0x176	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD5	STAGE4 fast FIFO WORD5
0x177	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD6	STAGE4 fast FIFO WORD6
0x178	[15:0]	X	R/$\overline{W}$	STAGE4_FF_WORD7	STAGE4 fast FIFO WORD7
0x179	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD0	STAGE4 slow FIFO WORD0
0x17A	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD1	STAGE4 slow FIFO WORD1
0x17B	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD2	STAGE4 slow FIFO WORD2
0x17C	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD3	STAGE4 slow FIFO WORD3
0x17D	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD4	STAGE4 slow FIFO WORD4
0x17E	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD5	STAGE4 slow FIFO WORD5
0x17F	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD6	STAGE4 slow FIFO WORD6
0x180	[15:0]	X	R/$\overline{W}$	STAGE4_SF_WORD7	STAGE4 slow FIFO WORD7
0x181	[15:0]	X	R/$\overline{W}$	STAGE4_SF_AMBIENT	STAGE4 slow FIFO ambient value
0x182	[15:0]	X	R/$\overline{W}$	STAGE4_FF_AVG	STAGE4 fast FIFO average value
0x183	[15:0]	X	R/$\overline{W}$	STAGE4_CDC_WORD0	STAGE4 CDC FIFO WORD0
0x184	[15:0]	X	R/$\overline{W}$	STAGE4_CDC_WORD1	STAGE4 CDC FIFO WORD1
0x185	[15:0]	X	R/$\overline{W}$	STAGE4_MAX_WORD0	STAGE4 maximum value FIFO WORD0
0x186	[15:0]	X	R/$\overline{W}$	STAGE4_MAX_WORD1	STAGE4 maximum value FIFO WORD1
0x187	[15:0]	X	R/$\overline{W}$	STAGE4_MAX_WORD2	STAGE4 maximum value FIFO WORD2
0x188	[15:0]	X	R/$\overline{W}$	STAGE4_MAX_WORD3	STAGE4 maximum value FIFO WORD3
0x189	[15:0]	X	R/$\overline{W}$	STAGE4_MAX_AVG	STAGE4 average maximum FIFO value
0x18A	[15:0]	X	R/$\overline{W}$	STAGE4_HIGH_THRESHOLD	STAGE4 high threshold value
0x18B	[15:0]	X	R/$\overline{W}$	STAGE4_MAX_TEMP	STAGE4 temporary maximum value
0x18C	[15:0]	X	R/$\overline{W}$	STAGE4_MIN_WORD0	STAGE4 minimum value FIFO WORD0
0x18D	[15:0]	X	R/$\overline{W}$	STAGE4_MIN_WORD1	STAGE4 minimum value FIFO WORD1
0x18E	[15:0]	X	R/$\overline{W}$	STAGE4_MIN_WORD2	STAGE4 minimum value FIFO WORD2
0x18F	[15:0]	X	R/$\overline{W}$	STAGE4_MIN_WORD3	STAGE4 minimum value FIFO WORD3
0x190	[15:0]	X	R/$\overline{W}$	STAGE4_MIN_AVG	STAGE4 average minimum FIFO value
0x191	[15:0]	X	R/$\overline{W}$	STAGE4_LOW_THRESHOLD	STAGE4 low threshold value
0x192	[15:0]	X	R/$\overline{W}$	STAGE4_MIN_TEMP	STAGE4 temporary minimum value
0x193	[15:0]	X		Unused	Set unused register bits to 0

Table 48. STAGE5 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x194	[15:0]	X	R/W	STAGE5_CONV_DATA	STAGE5 CDC 16-bit conversion data (copy of data in CDC_RESULT_S5 register)
0x195	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD0	STAGE5 fast FIFO WORD0
0x196	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD1	STAGE5 fast FIFO WORD1
0x197	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD2	STAGE5 fast FIFO WORD2
0x198	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD3	STAGE5 fast FIFO WORD3
0x199	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD4	STAGE5 fast FIFO WORD4
0x19A	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD5	STAGE5 fast FIFO WORD5
0x19B	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD6	STAGE5 fast FIFO WORD6
0x19C	[15:0]	X	R/$\overline{W}$	STAGE5_FF_WORD7	STAGE5 fast FIFO WORD7
0x19D	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD0	STAGE5 slow FIFO WORD0
0x19E	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD1	STAGE5 slow FIFO WORD1
0x19F	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD2	STAGE5 slow FIFO WORD2
0x1A0	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD3	STAGE5 slow FIFO WORD3
0x1A1	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD4	STAGE5 slow FIFO WORD4
0x1A2	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD5	STAGE5 slow FIFO WORD5
0x1A3	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD6	STAGE5 slow FIFO WORD6
0x1A4	[15:0]	X	R/$\overline{W}$	STAGE5_SF_WORD7	STAGE5 slow FIFO WORD7
0x1A5	[15:0]	X	R/$\overline{W}$	STAGE5_SF_AMBIENT	STAGE5 slow FIFO ambient value
0x1A6	[15:0]	X	R/$\overline{W}$	STAGE5_FF_AVG	STAGE5 fast FIFO average value
0x1A7	[15:0]	X	R/$\overline{W}$	STAGE5_CDC_WORD0	STAGE5 CDC FIFO WORD0
0x1A8	[15:0]	X	R/$\overline{W}$	STAGE5_CDC_WORD1	STAGE5 CDC FIFO WORD1
0x1A9	[15:0]	X	R/$\overline{W}$	STAGE5_MAX_WORD0	STAGE5 maximum value FIFO WORD0
0x1AA	[15:0]	X	R/$\overline{W}$	STAGE5_MAX_WORD1	STAGE5 maximum value FIFO WORD1
0x1AB	[15:0]	X	R/$\overline{W}$	STAGE5_MAX_WORD2	STAGE5 maximum value FIFO WORD2
0x1AC	[15:0]	X	R/$\overline{W}$	STAGE5_MAX_WORD3	STAGE5 maximum value FIFO WORD3
0x1AD	[15:0]	X	R/$\overline{W}$	STAGE5_MAX_AVG	STAGE5 average maximum FIFO value
0x1AE	[15:0]	X	R/$\overline{W}$	STAGE5_HIGH_THRESHOLD	STAGE5 high threshold value
0x1AF	[15:0]	X	R/$\overline{W}$	STAGE5_MAX_TEMP	STAGE5 temporary maximum value
0x1B0	[15:0]	X	R/$\overline{W}$	STAGE5_MIN_WORD0	STAGE5 minimum value FIFO WORD0
0x1B1	[15:0]	X	R/$\overline{W}$	STAGE5_MIN_WORD1	STAGE5 minimum value FIFO WORD1
0x1B2	[15:0]	X	R/$\overline{W}$	STAGE5_MIN_WORD2	STAGE5 minimum value FIFO WORD2
0x1B3	[15:0]	X	R/$\overline{W}$	STAGE5_MIN_WORD3	STAGE5 minimum value FIFO WORD3
0x1B4	[15:0]	X	R/$\overline{W}$	STAGE5_MIN_AVG	STAGE5 average minimum FIFO value
0x1B5	[15:0]	X	R/$\overline{W}$	STAGE5_LOW_THRESHOLD	STAGE5 low threshold value
0x1B6	[15:0]	X	R/$\overline{W}$	STAGE5_MIN_TEMP	STAGE5 temporary minimum value
0x1B7	[15:0]	X		Unused	Set unused register bits to 0

Table 49. STAGE6 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x1B8	[15:0]	X	R/$\overline{W}$	STAGE6_CONV_DATA	STAGE6 CDC 16-bit conversion data (copy of data in CDC_RESULT_S6 register)
0x1B9	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD0	STAGE6 fast FIFO WORD0
0x1BA	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD1	STAGE6 fast FIFO WORD1
0x1BB	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD2	STAGE6 fast FIFO WORD2
0x1BC	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD3	STAGE6 fast FIFO WORD3
0x1BD	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD4	STAGE6 fast FIFO WORD4
0x1BE	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD5	STAGE6 fast FIFO WORD5
0x1BF	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD6	STAGE6 fast FIFO WORD6
0x1C0	[15:0]	X	R/$\overline{W}$	STAGE6_FF_WORD7	STAGE6 fast FIFO WORD7
0x1C1	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD0	STAGE6 slow FIFO WORD0
0x1C2	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD1	STAGE6 slow FIFO WORD1
0x1C3	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD2	STAGE6 slow FIFO WORD2
0x1C4	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD3	STAGE6 slow FIFO WORD3
0x1C5	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD4	STAGE6 slow FIFO WORD4
0x1C6	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD5	STAGE6 slow FIFO WORD5
0x1C7	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD6	STAGE6 slow FIFO WORD6
0x1C8	[15:0]	X	R/$\overline{W}$	STAGE6_SF_WORD7	STAGE6 slow FIFO WORD7
0x1C9	[15:0]	X	R/$\overline{W}$	STAGE6_SF_AMBIENT	STAGE6 slow FIFO ambient value
0x1CA	[15:0]	X	R/$\overline{W}$	STAGE6_FF_AVG	STAGE6 fast FIFO average value
0x1CB	[15:0]	X	R/$\overline{W}$	STAGE6_CDC_WORD0	STAGE0 CDC FIFO WORD0
0x1CC	[15:0]	X	R/$\overline{W}$	STAGE6_CDC_WORD1	STAGE6 CDC FIFO WORD1
0x1CD	[15:0]	X	R/$\overline{W}$	STAGE6_MAX_WORD0	STAGE6 maximum value FIFO WORD0
0x1CE	[15:0]	X	R/$\overline{W}$	STAGE6_MAX_WORD1	STAGE6 maximum value FIFO WORD1
0x1CF	[15:0]	X	R/$\overline{W}$	STAGE6_MAX_WORD2	STAGE6 maximum value FIFO WORD2
0x1D0	[15:0]	X	R/$\overline{W}$	STAGE6_MAX_WORD3	STAGE6 maximum value FIFO WORD3
0x1D1	[15:0]	X	R/$\overline{W}$	STAGE6_MAX_AVG	STAGE6 average maximum FIFO value
0x1D2	[15:0]	X	R/$\overline{W}$	STAGE6_HIGH_THRESHOLD	STAGE6 high threshold value
0x1D3	[15:0]	X	R/$\overline{W}$	STAGE6_MAX_TEMP	STAGE6 temporary maximum value
0x1D4	[15:0]	X	R/$\overline{W}$	STAGE6_MIN_WORD0	STAGE6 minimum value FIFO WORD0
0x1D5	[15:0]	X	R/$\overline{W}$	STAGE6_MIN_WORD1	STAGE6 minimum value FIFO WORD1
0x1D6	[15:0]	X	R/$\overline{W}$	STAGE6_MIN_WORD2	STAGE6 minimum value FIFO WORD2
0x1D7	[15:0]	X	R/$\overline{W}$	STAGE6_MIN_WORD3	STAGE6 minimum value FIFO WORD3
0x1D8	[15:0]	X	R/$\overline{W}$	STAGE6_MIN_AVG	STAGE6 average minimum FIFO value
0x1D9	[15:0]	X	R/$\overline{W}$	STAGE6_LOW_THRESHOLD	STAGE6 low threshold value
0x1DA	[15:0]	X	R/$\overline{W}$	STAGE6_MIN_TEMP	STAGE6 temporary minimum value
0x1DB	[15:0]	X		Unused	Set unused register bits to 0

Table 50. STAGE7 Results Registers

Address	Data Bit	Default Value	Type	Mnemonic	Description
0x1DC	[15:0]	X	R/W	STAGE7_CONV_DATA	STAGE7 CDC 16-bit conversion data (copy of data in CDC_RESULT_S7 register)
0x1DD	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD0	STAGE7 fast FIFO WORD0
0x1DE	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD1	STAGE7 fast FIFO WORD1
0x1DF	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD2	STAGE7 fast FIFO WORD2
0x1E0	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD3	STAGE7 fast FIFO WORD3
0x1E1	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD4	STAGE7 fast FIFO WORD4
0x1E2	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD5	STAGE7 fast FIFO WORD5
0x1E3	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD6	STAGE7 fast FIFO WORD6
0x1E4	[15:0]	X	R/$\overline{W}$	STAGE7_FF_WORD7	STAGE7 fast FIFO WORD7
0x1E5	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD0	STAGE7 slow FIFO WORD0
0x1E6	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD1	STAGE7 slow FIFO WORD1
0x1E7	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD2	STAGE7 slow FIFO WORD2
0x1E8	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD3	STAGE7 slow FIFO WORD3
0x1E9	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD4	STAGE7 slow FIFO WORD4
0x1EA	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD5	STAGE7 slow FIFO WORD5
0x1EB	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD6	STAGE7 slow FIFO WORD6
0x1EC	[15:0]	X	R/$\overline{W}$	STAGE7_SF_WORD7	STAGE7 slow FIFO WORD7
0x1ED	[15:0]	X	R/$\overline{W}$	STAGE7_SF_AMBIENT	STAGE7 slow FIFO ambient value
0x1EE	[15:0]	X	R/$\overline{W}$	STAGE7_FF_AVG	STAGE7 fast FIFO average value
0x1EF	[15:0]	X	R/$\overline{W}$	STAGE7_CDC_WORD0	STAGE7 CDC FIFO WORD0
0x1F0	[15:0]	X	R/$\overline{W}$	STAGE7_CDC_WORD1	STAGE7 CDC FIFO WORD1
0x1F1	[15:0]	X	R/$\overline{W}$	STAGE7_MAX_WORD0	STAGE7 maximum value FIFO WORD0
0x1F2	[15:0]	X	R/$\overline{W}$	STAGE7_MAX_WORD1	STAGE7 maximum value FIFO WORD1
0x1F3	[15:0]	X	R/$\overline{W}$	STAGE7_MAX_WORD2	STAGE7 maximum value FIFO WORD2
0x1F4	[15:0]	X	R/$\overline{W}$	STAGE7_MAX_WORD3	STAGE7 maximum value FIFO WORD3
0x1F5	[15:0]	X	R/$\overline{W}$	STAGE7_MAX_AVG	STAGE7 average maximum FIFO value
0x1F6	[15:0]	X	R/$\overline{W}$	STAGE7_HIGH_THRESHOLD	STAGE7 high threshold value
0x1F7	[15:0]	X	R/$\overline{W}$	STAGE7_MAX_TEMP	STAGE7 temporary maximum value
0x1F8	[15:0]	X	R/$\overline{W}$	STAGE7_MIN_WORD0	STAGE7 minimum value FIFO WORD0
0x1F9	[15:0]	X	R/$\overline{W}$	STAGE7_MIN_WORD1	STAGE7 minimum value FIFO WORD1
0x1FA	[15:0]	X	R/$\overline{W}$	STAGE7_MIN_WORD2	STAGE7 minimum value FIFO WORD2
0x1FB	[15:0]	X	R/$\overline{W}$	STAGE7_MIN_WORD3	STAGE7 minimum value FIFO WORD3
0x1FC	[15:0]	X	R/$\overline{W}$	STAGE7_MIN_AVG	STAGE7 average minimum FIFO value
0x1FD	[15:0]	X	R/$\overline{W}$	STAGE7_LOW_THRESHOLD	STAGE7 low threshold value
0x1FE	[15:0]	X	R/$\overline{W}$	STAGE7_MIN_TEMP	STAGE7 temporary minimum value
0x1FF	[15:0]	X		Unused	Set unused register bits to 0

OUTLINE DIMENSIONS

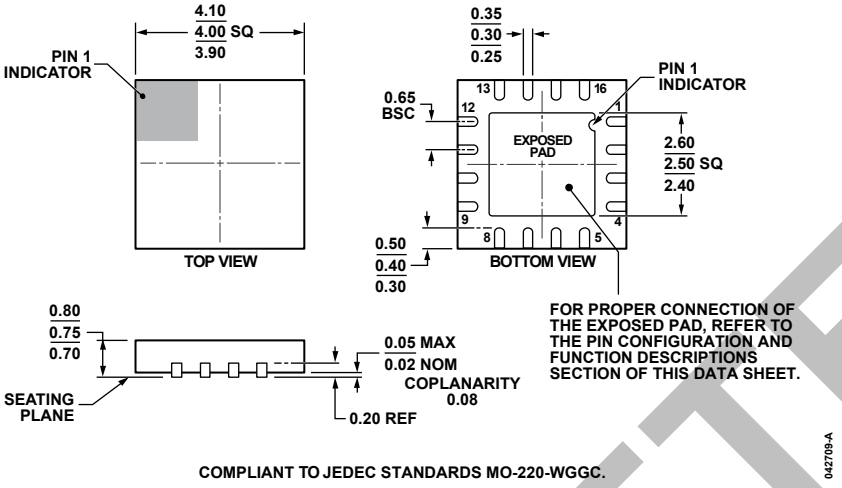


Figure 47. 16-Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Very Very Thin Quad
(CP-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Serial Interface Description	Package Description	Package Option
AD7148ACPZ-1REEL	–40°C to +85°C	I²C Interface	16-Lead LFCSP_WQ	CP-16-26
AD7148ACPZ-1500RL7	–40°C to +85°C	I²C Interface	16-Lead LFCSP_WQ	CP-16-26

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D07155-0-5/15(B)