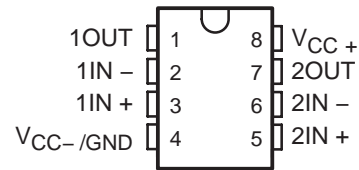


TL322C, TL322I DUAL LOW-POWER OPERATIONAL AMPLIFIERS

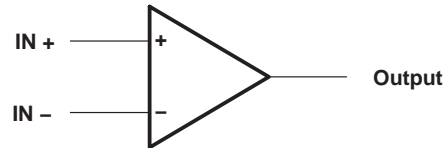
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- **Wide Range of Supply Voltages**
Single Supply . . . 5 V to 30 V
Dual Supplies . . . ± 2.5 V to ± 15 V
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TL322C and the TL322I are dual operational amplifiers similar in performance to the μ A741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 5 V to 30 V. Operation from split supplies is also possible provided the difference between the two supplies is 5 V to 30 V. The common-mode input range includes the negative supply. Output range is from the negative supply to $V_{CC} - 1.5$ V. Quiescent supply currents per amplifier are typically less than one-half those of the μ A741.

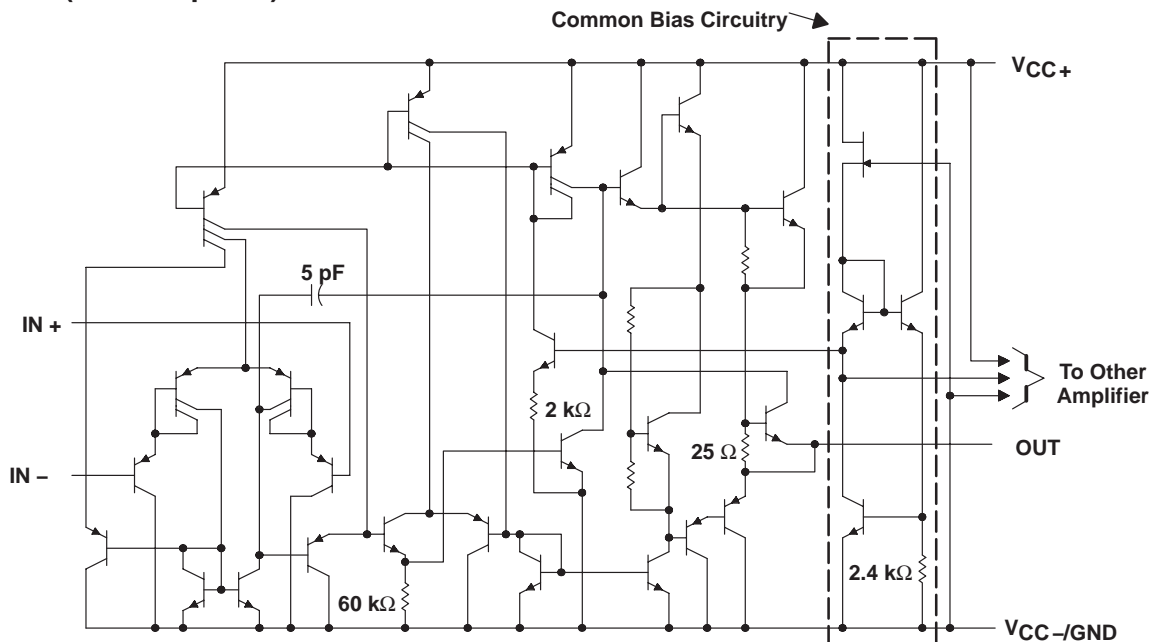
The TL322C is characterized for operation from 0°C to 70°C. The TL322I is characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

TA	V _{IO} MAX AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	10 mV	TL322CD	TL322CP
0°C to 70°C	8 mV	TL322ID	TL322IP

D packages are available taped and reeled. Add R suffix to device type, (e.g., TL322CDR).

schematic (each amplifier)



All component values shown are nominal.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TL322C, TL322I

DUAL LOW-POWER OPERATIONAL AMPLIFIERS

SLOS086 – D2567, OCTOBER 1979 – REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL322C	TL322I	UNIT
Supply voltage V_{CC+} (see Note 1)	18	18	V
Supply voltage V_{CC-} (see Note 1)	–18	–18	V
Supply voltage V_{CC+} (with respect to V_{CC-})	36	36	V
Differential input voltage (see Note 2)	± 36	± 36	V
Input voltage (see Notes 1 and 3)	± 18	± 18	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	0 to 70	–40 to 85	°C
Storage temperature range	–65 to 150	–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

- NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-} .

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Single supply voltage, V_{CC}	5		30	V
Dual supply voltage, V_{CC+}	2.5		15	V
Dual supply voltage, V_{CC-}	–2.5		–15	V

TL322C, TL322I

DUAL LOW-POWER OPERATIONAL AMPLIFIERS

SLOS086 – D2567, OCTOBER 1979 – REVISED OCTOBER 1990

electrical characteristics at specified free-air temperature, $V_{CC\pm} = 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL322C			TL322I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 0, R _S = 50 Ω	25°C Full range	2 10 12		2 8 10		mV		
α _{VIO}	Temperature coefficient of input offset voltage	V _O = 0, R _S = 50 Ω	25°C	10		10		μV/°C		
I _{IO}	Input offset current	V _O = 0	25°C Full range	30 50 200		30 75 250		nA		
α _{IIO}	Temperature coefficient of input offset current	V _O = 0	25°C	50		50		pA/°C		
I _{IB}	Input bias current	V _O = 0	25°C Full range	−0.2 −0.5 −0.8		−0.2 −0.5 −1		μA		
V _{ICR}	Common-mode input voltage range‡		25°C	V _{CC} − to 13	V _{CC} − to 13.5	V _{CC} − to 13	V _{CC} − to 13.5	V		
V _{OM}	Peak output voltage swing	R _L = 10 kΩ	25°C	±12	±13.5	±12	±12.5	V		
		R _L = 2 kΩ	25°C	±10	±13	±10	±12			
			Full range	±10	±10					
A _{VD}	Large-signal differential voltage amplification	V _O = ±10 V, R _L = 2 kΩ	25°C	20	200	20	200	V/mV		
			Full range	15	15					
B _{OM}	Maximum-output-swing bandwidth	V _O (PP) = 20 V, A _{VD} = 1, THD ≤ 5%, R _L = 2 kΩ	25°C	9		9		kHz		
B ₁	Unity-gain bandwidth	V _O = 50 mV, R _L = 10 kΩ	25°C	1		1		MHz		
φ _m	Phase margin	R _L = 2 kΩ, C _L = 200 pF	25°C	60°		60°				
r _i	Input resistance	f = 20 Hz	25°C	0.3	1	0.3	1	MΩ		
r _o	Output resistance	f = 20 Hz	25°C	75		75		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, R _S = 50 Ω	25°C	70	90	70	90	dB		
k _{SVS}	Supply voltage sensitivity (ΔV _{IO} /ΔV _{CC})	V _{CC} = ±2.5 V to ±15 V, R _S = 50 Ω	25°C	30	150	30	150	μV/V		
I _{OS}	Short-circuit output current§	V _O = 0	25°C	±10	±30	±45	±10	±30	±45	mA
I _{CC}	Total supply current	V _O = 0, No load	25°C	1.4	4	1.4	4	mA		

† All characteristics are under open-loop conditions unless otherwise noted. Full range for T_A is 0°C to 70°C for TL322C and –40°C to 85°C for TL322I.

‡ The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+} .

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.



TL322C, TL322I

DUAL LOW-POWER OPERATIONAL AMPLIFIERS

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electrical characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL322C			TL322I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 2.5 V, R _S = 50 Ω	2 10			8			mV
I _{IO}	Input offset current	V _O = 2.5 V	30 50			75			nA
I _{IB}	Input bias current		−0.2 −0.5			−0.5			pA
V _{OM}	Peak output voltage swing‡	R _L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R _L = 10 kΩ, V _{CC+} = 5 V to 30 V	V _{CC+} − 1.7			V _{CC+} − 1.7			
A _{VD}	Large-signal differential voltage amplification	V _O = 1.7 V to 3.3 V, R _L = 2 kΩ	20	200		20	200		V/mV
k _{SVS}	Supply voltage sensitivity (ΔV _{IO} / ΔV _{CC+})	V _{CC} = ±2.5 V to ±15 V	150			150			μV/V
I _{CC}	Supply current	V _O = 2.5 V, No load	1.2 4			1.2 4			mA
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100, f = 1 kHz to 20 kHz	120			120			dB

† All characteristics are specified under open-loop conditions.

‡ Output will swing essentially to ground.

switching characteristics, $V_{CC+} = 15\text{ V}$, $V_{CC-} = -15\text{ V}$, $A_{VD} = 1$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = \pm 10\text{ V}$,	$C_L = 100\text{ pF}$, See Figure 1		0.6		V/ μs
t_r	Rise time	$\Delta V_O = 50\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Figure 1			0.35		μs
t_f	Fall time				0.35		μs
	Overshoot factor				20%		
	Crossover distortion	$V_{I(PP)} = 30\text{ mV}$,	$V_{O(PP)} = 2\text{ V}$, $f = 10\text{ kHz}$		1%		

PARAMETER MEASUREMENT INFORMATION

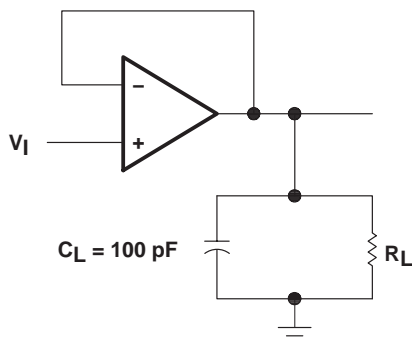


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS†

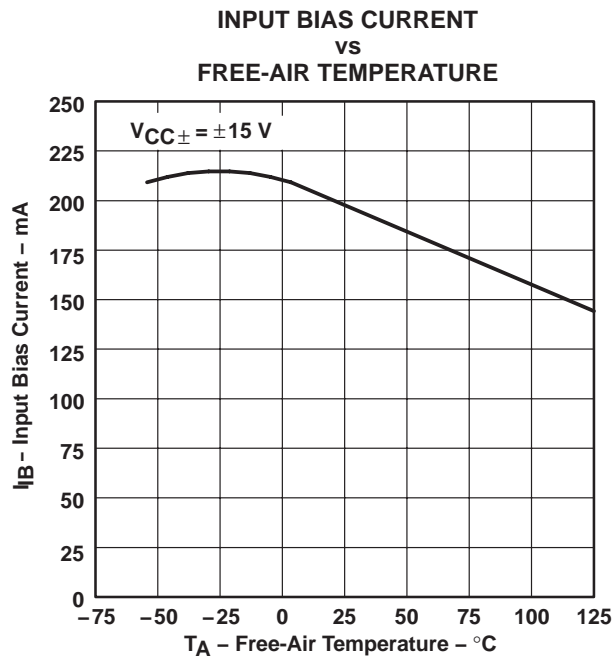


Figure 2

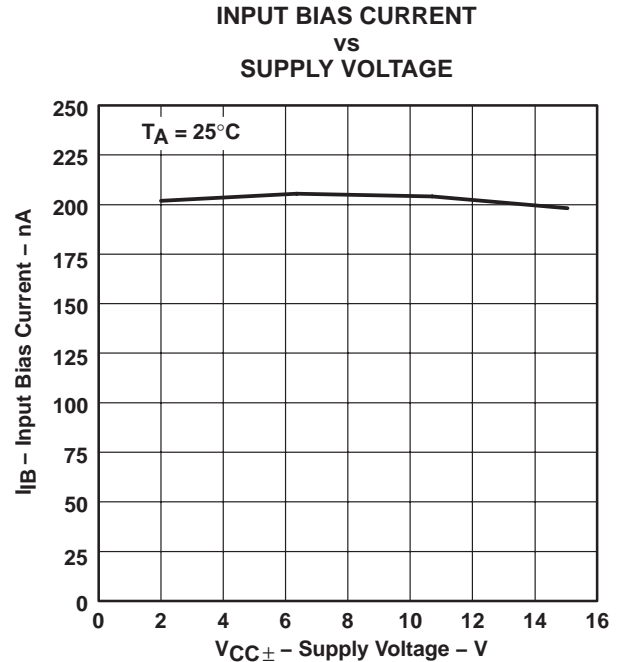


Figure 3

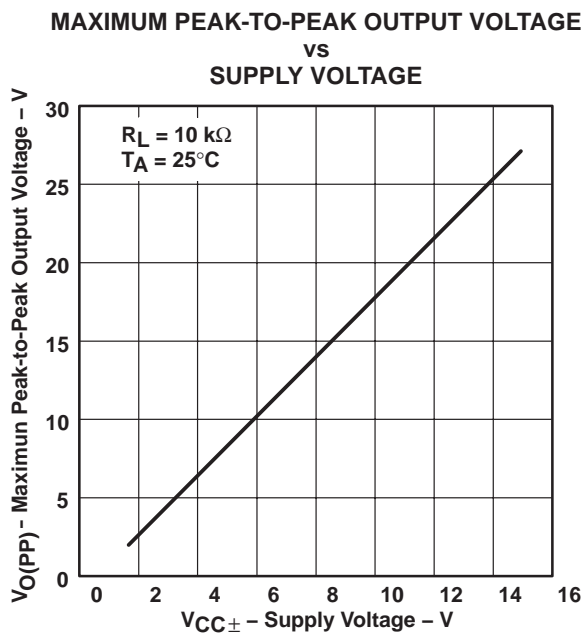


Figure 4

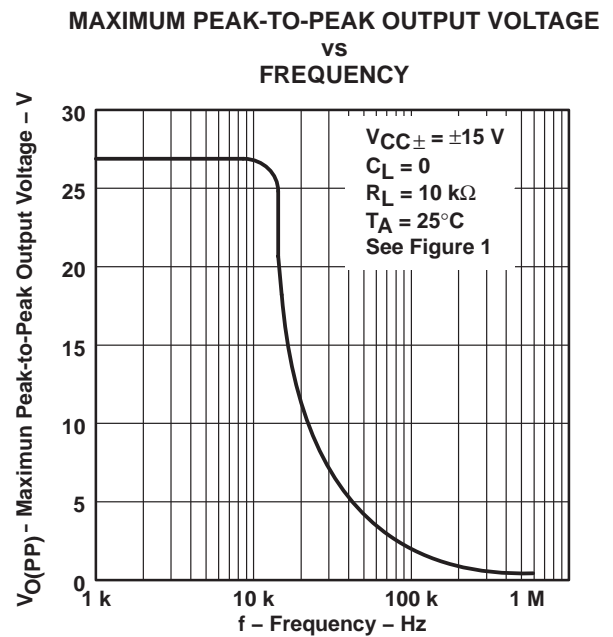


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TL322C, TL322I

DUAL LOW-POWER OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY**

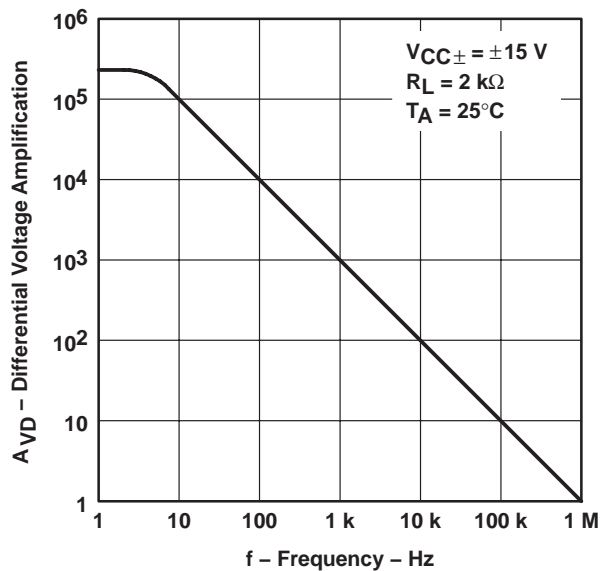


Figure 6

**VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE**

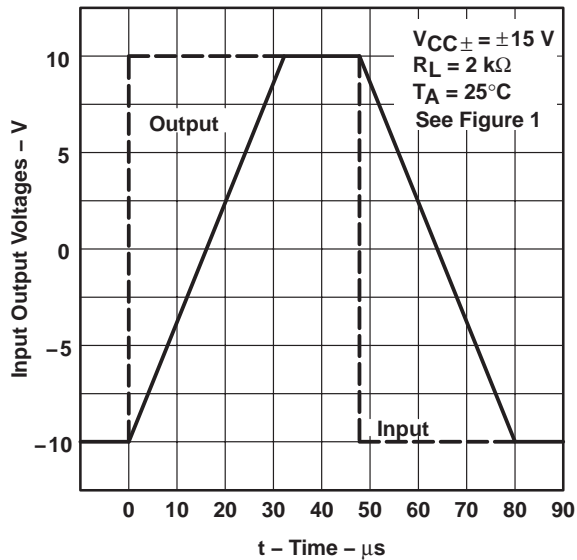


Figure 7

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL322CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL322ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL322ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL322IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL322IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

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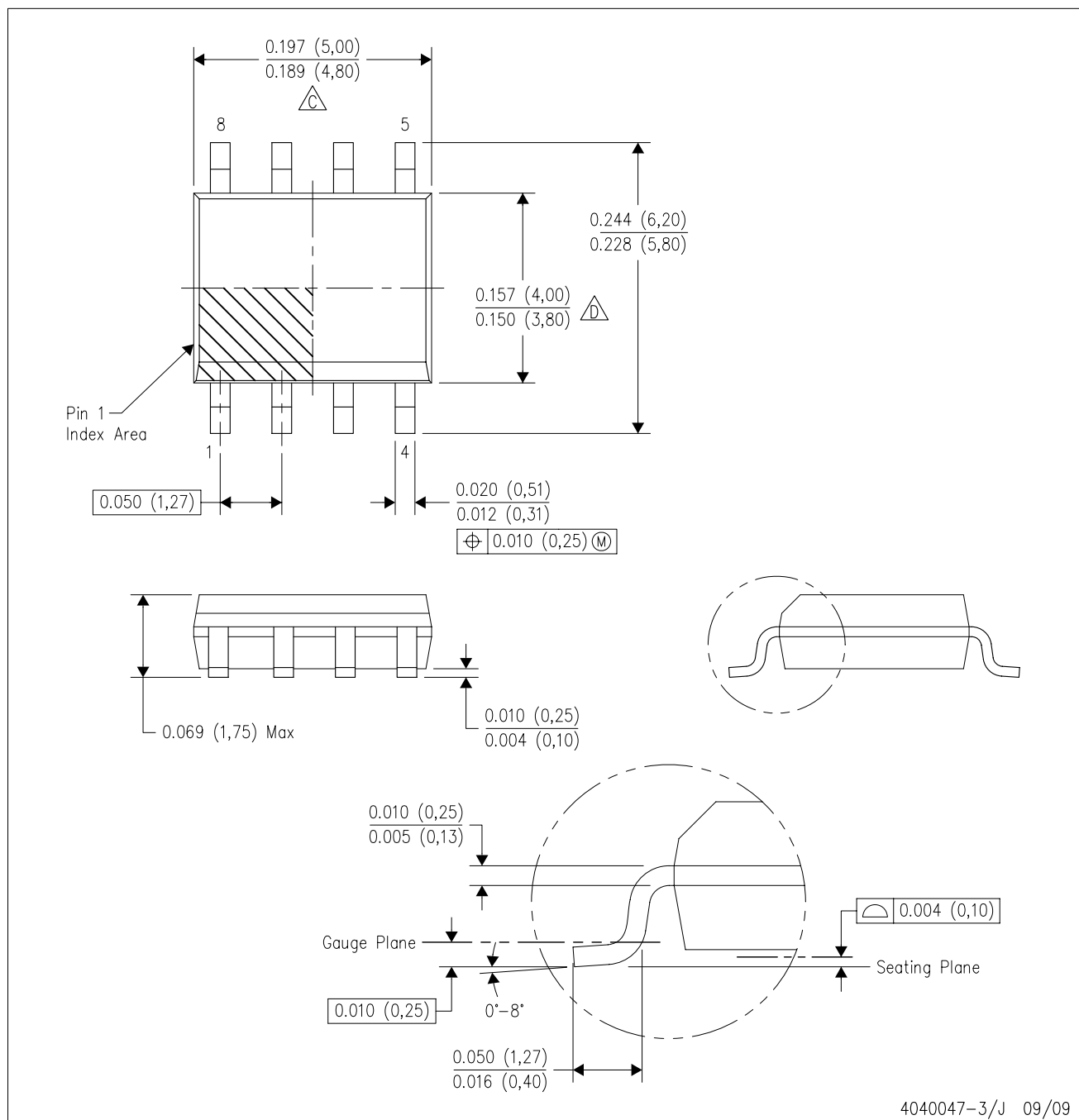
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
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 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
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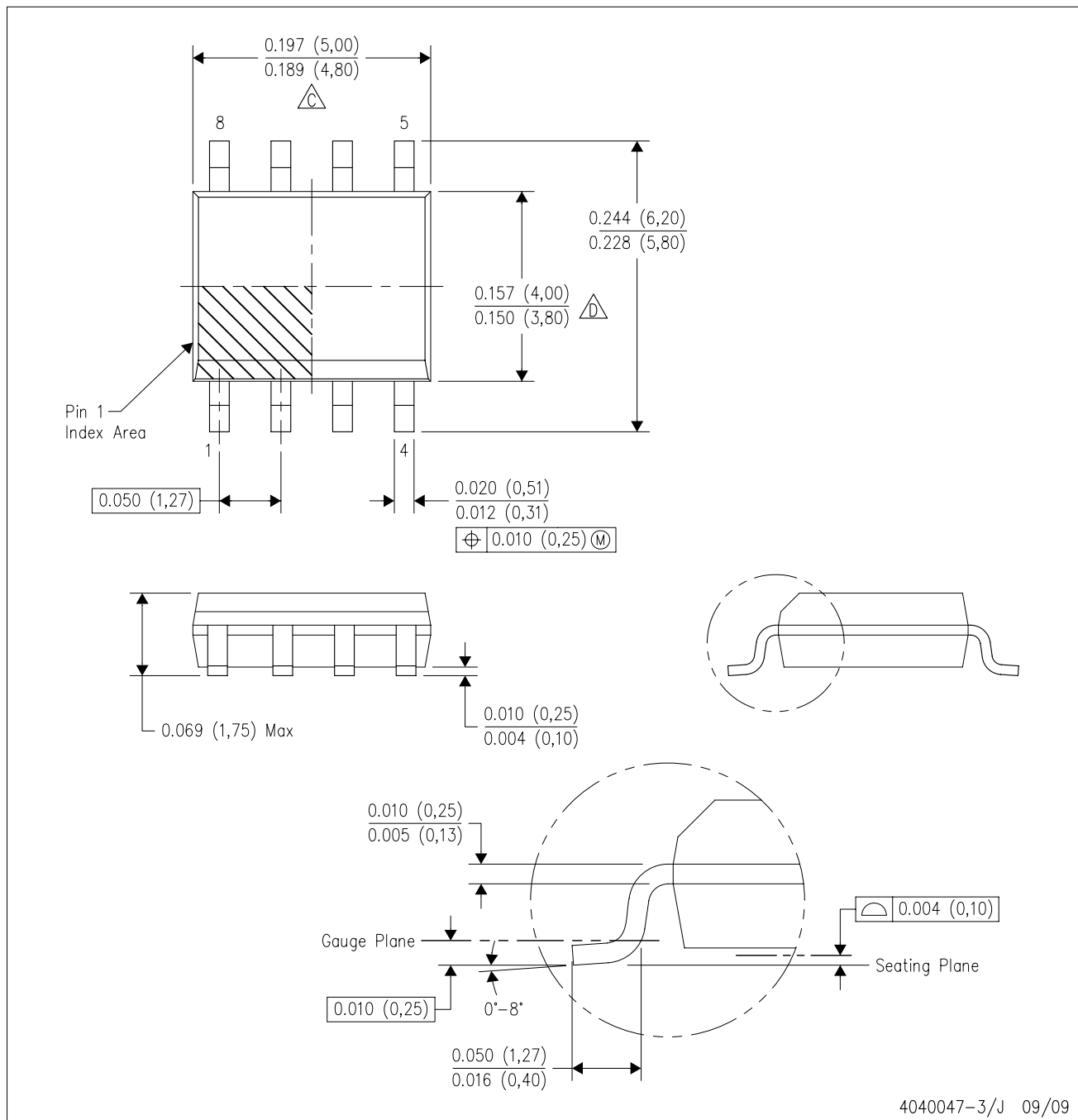
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PLASTIC SMALL-OUTLINE PACKAGE



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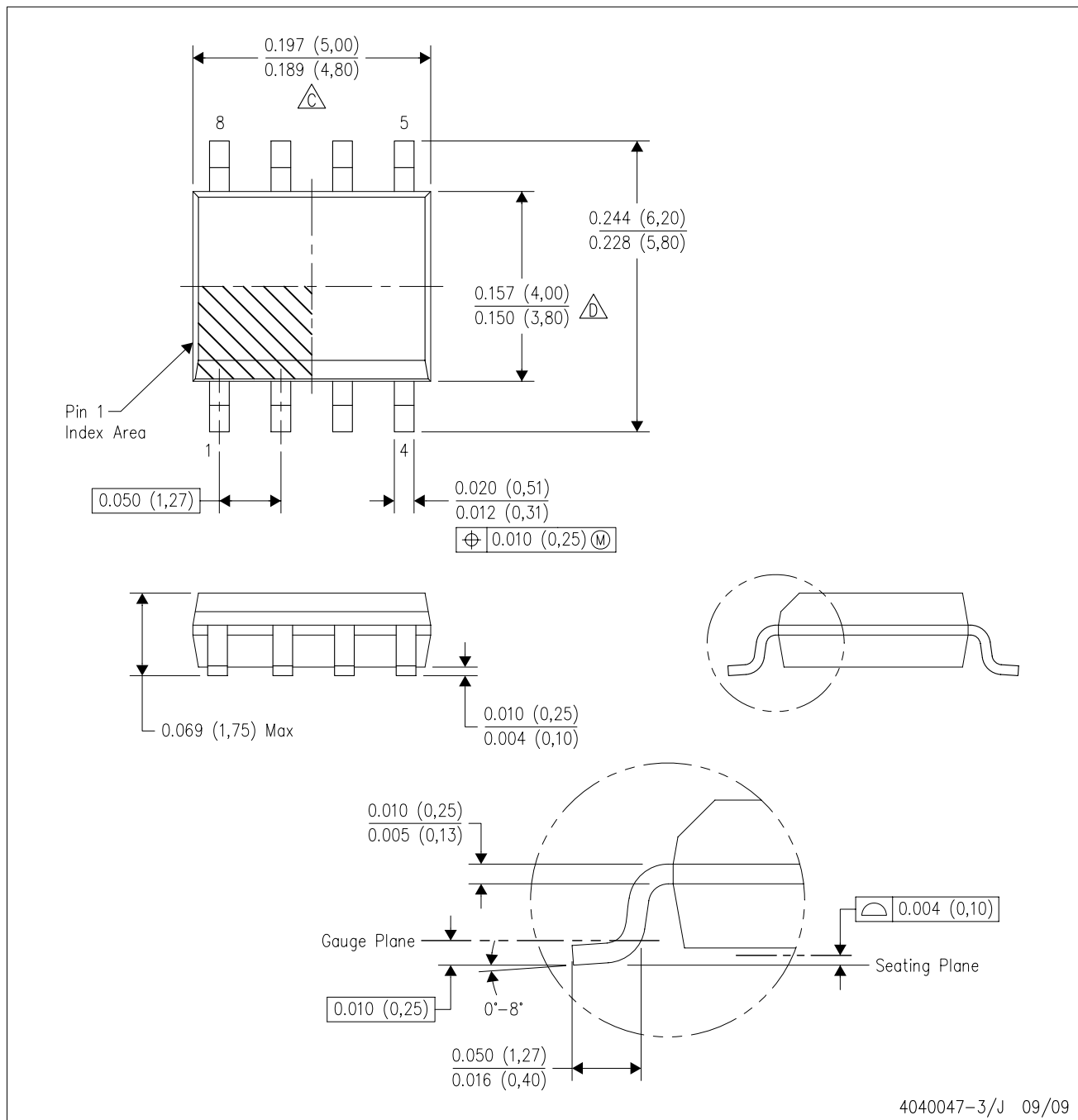
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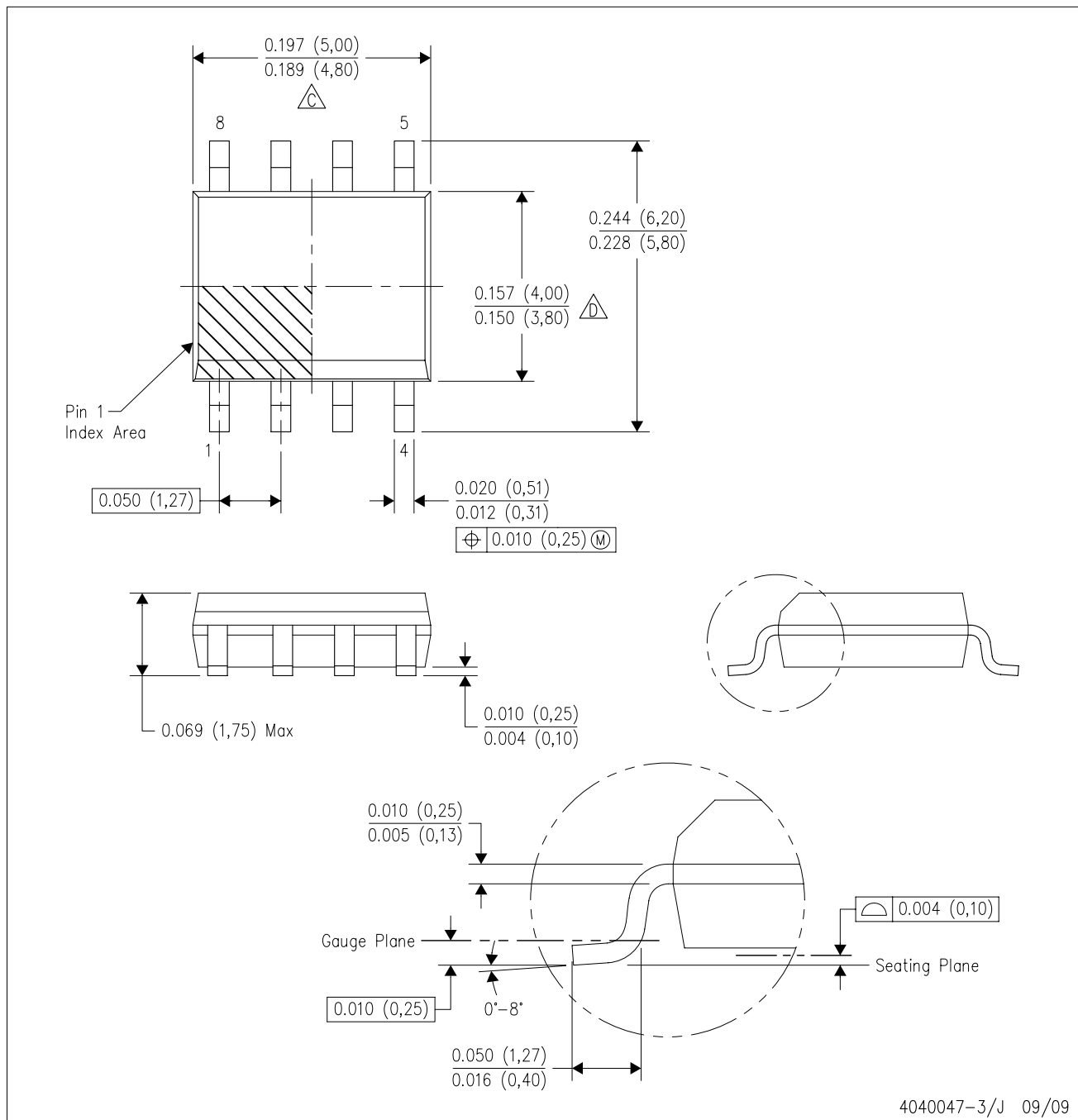
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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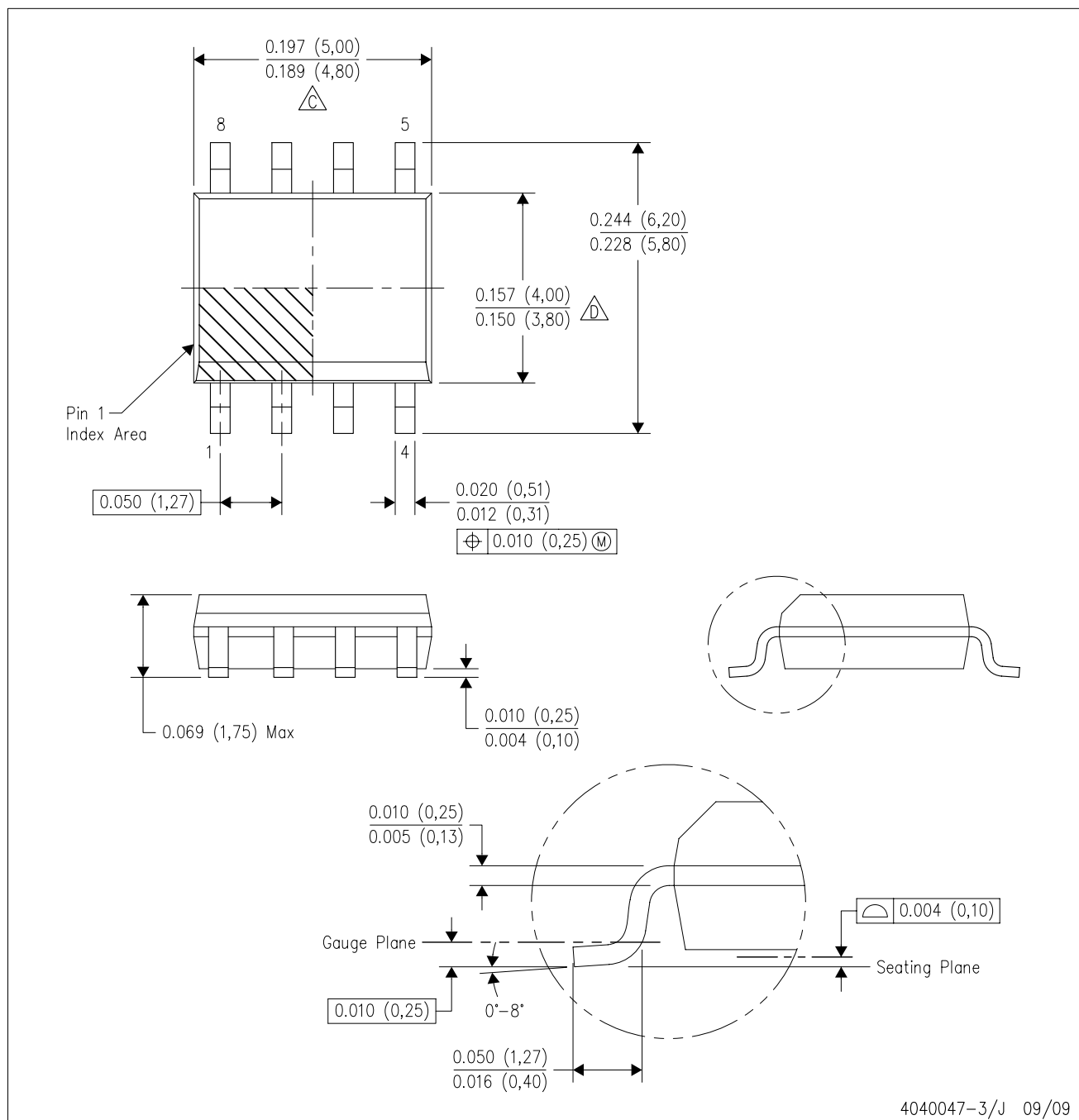
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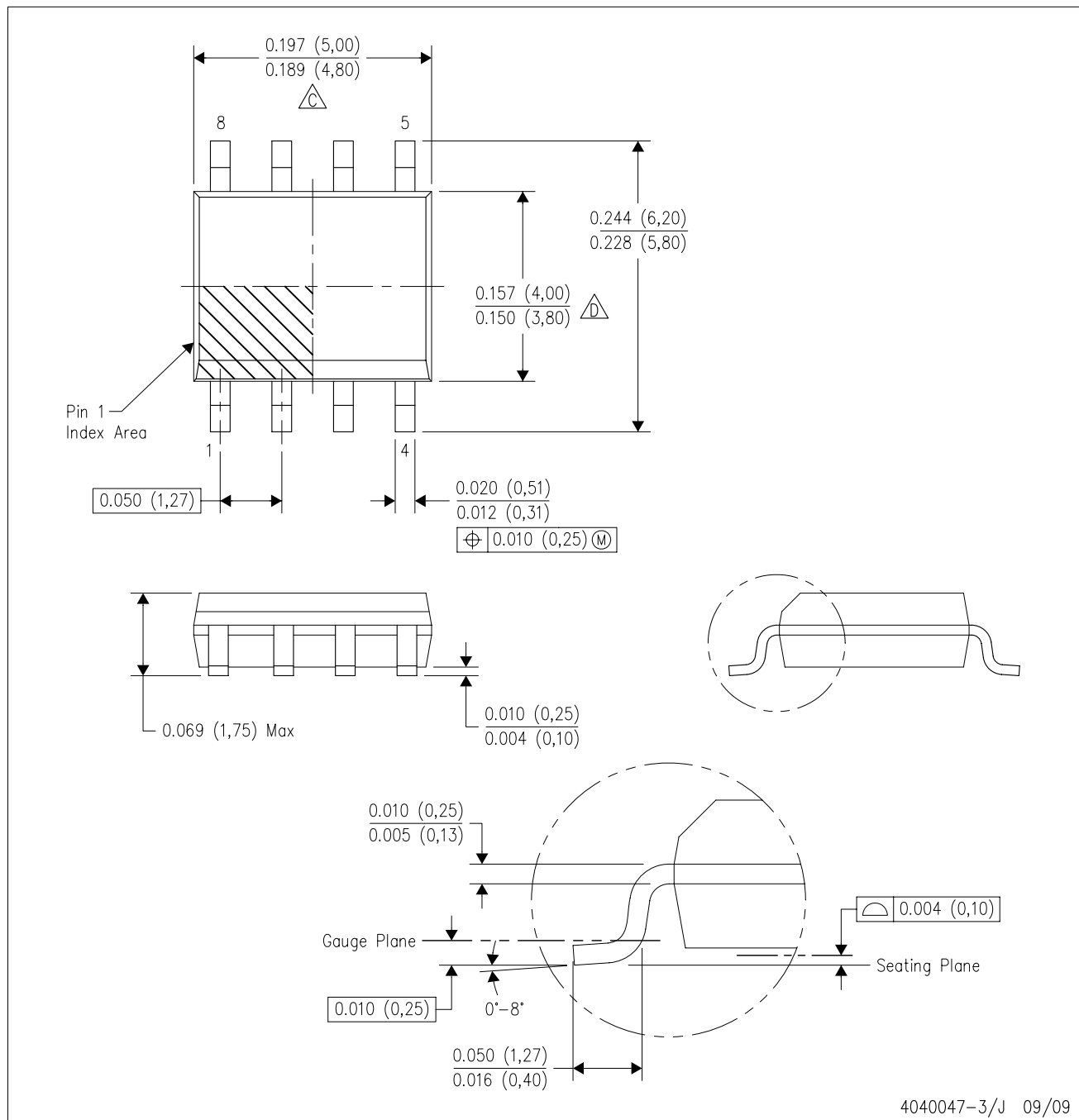
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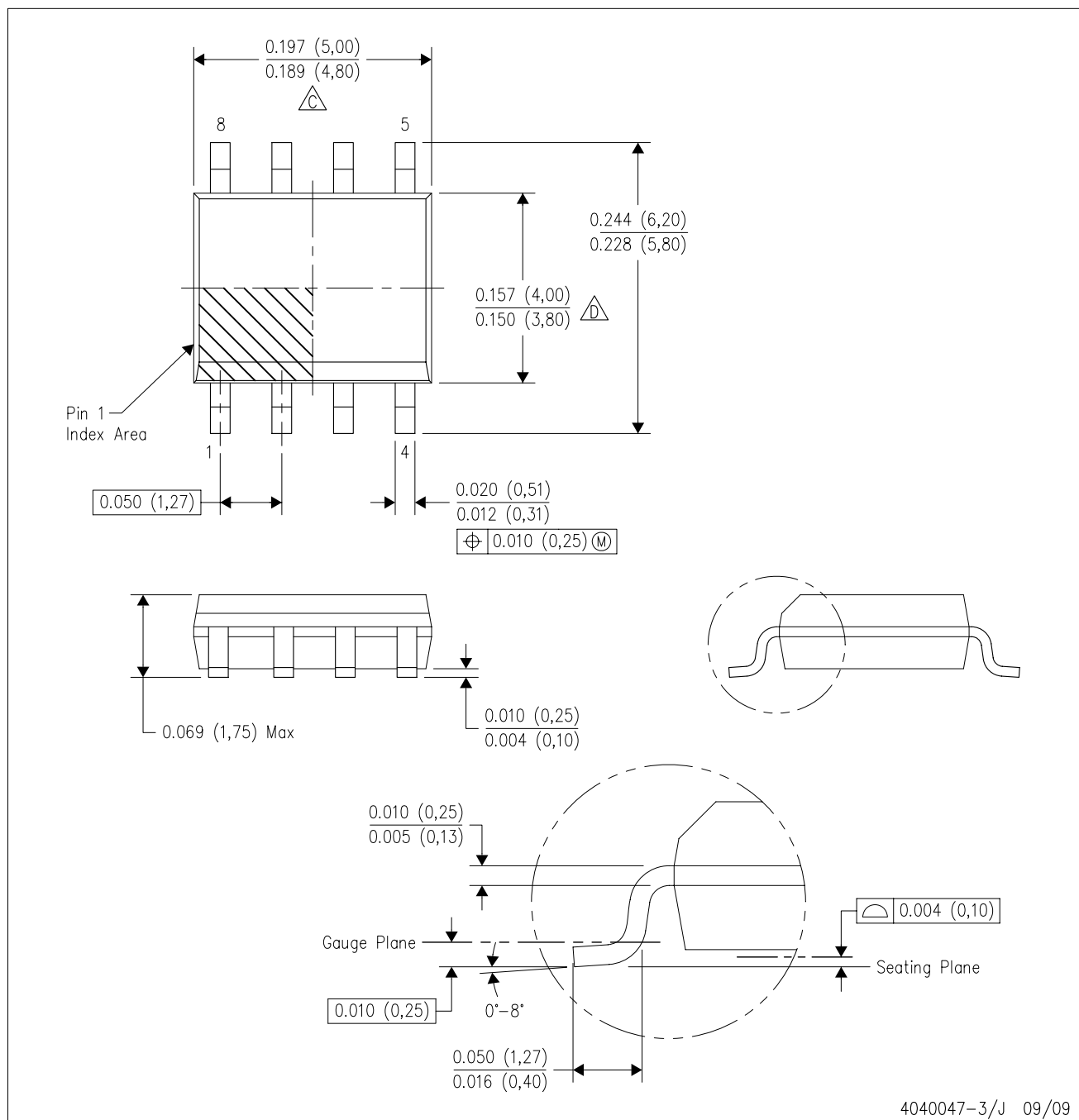
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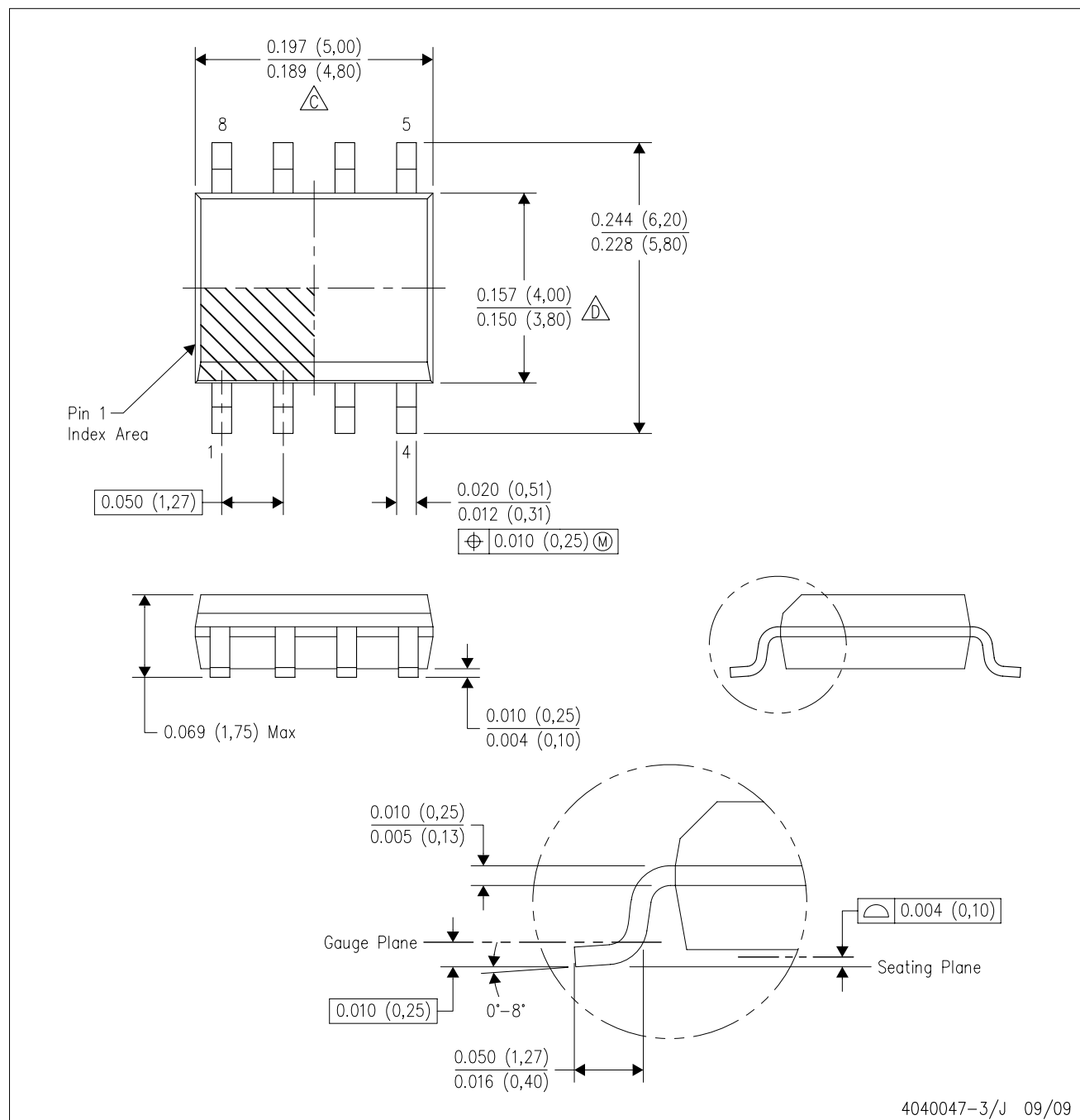
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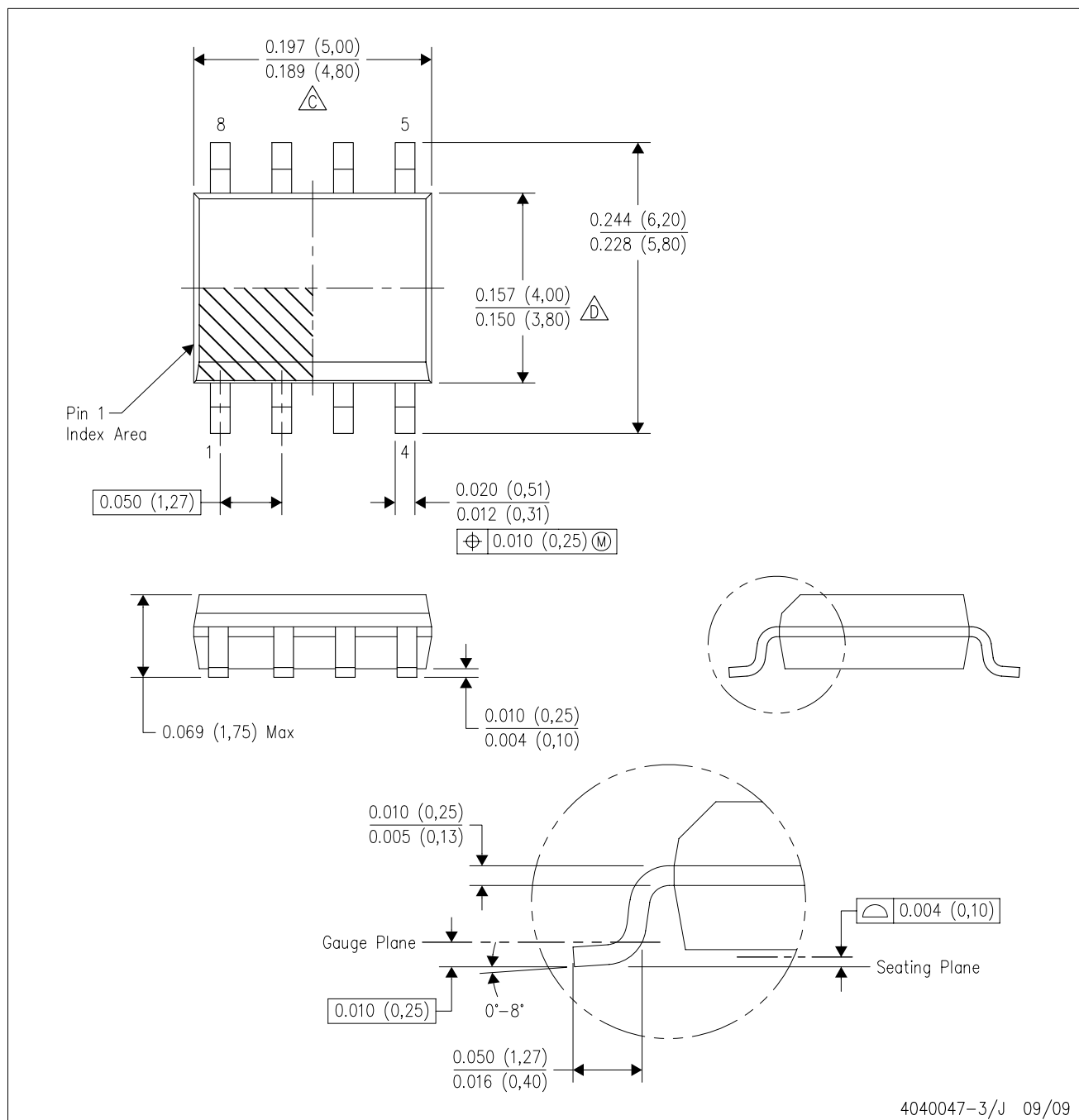
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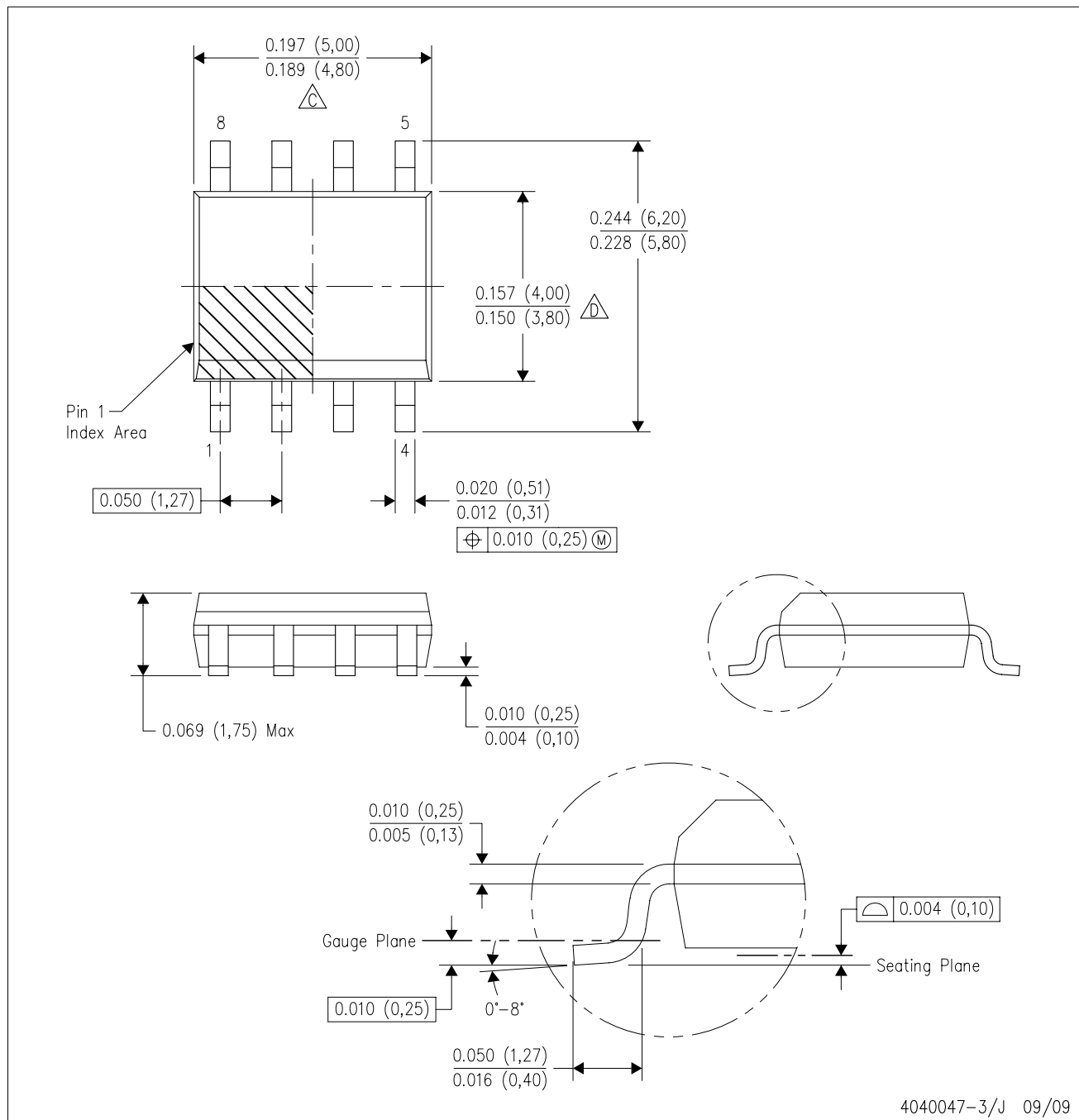
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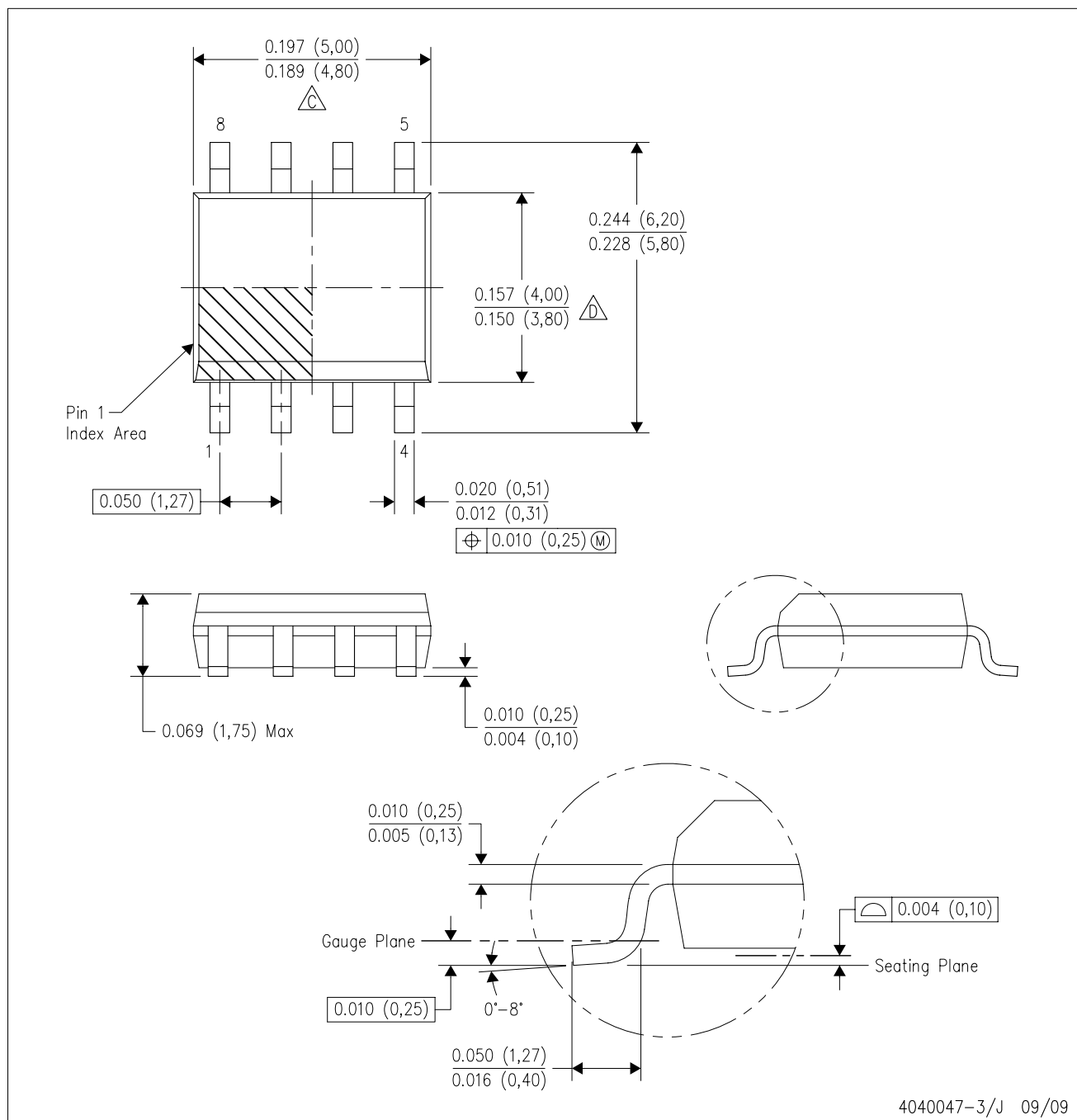
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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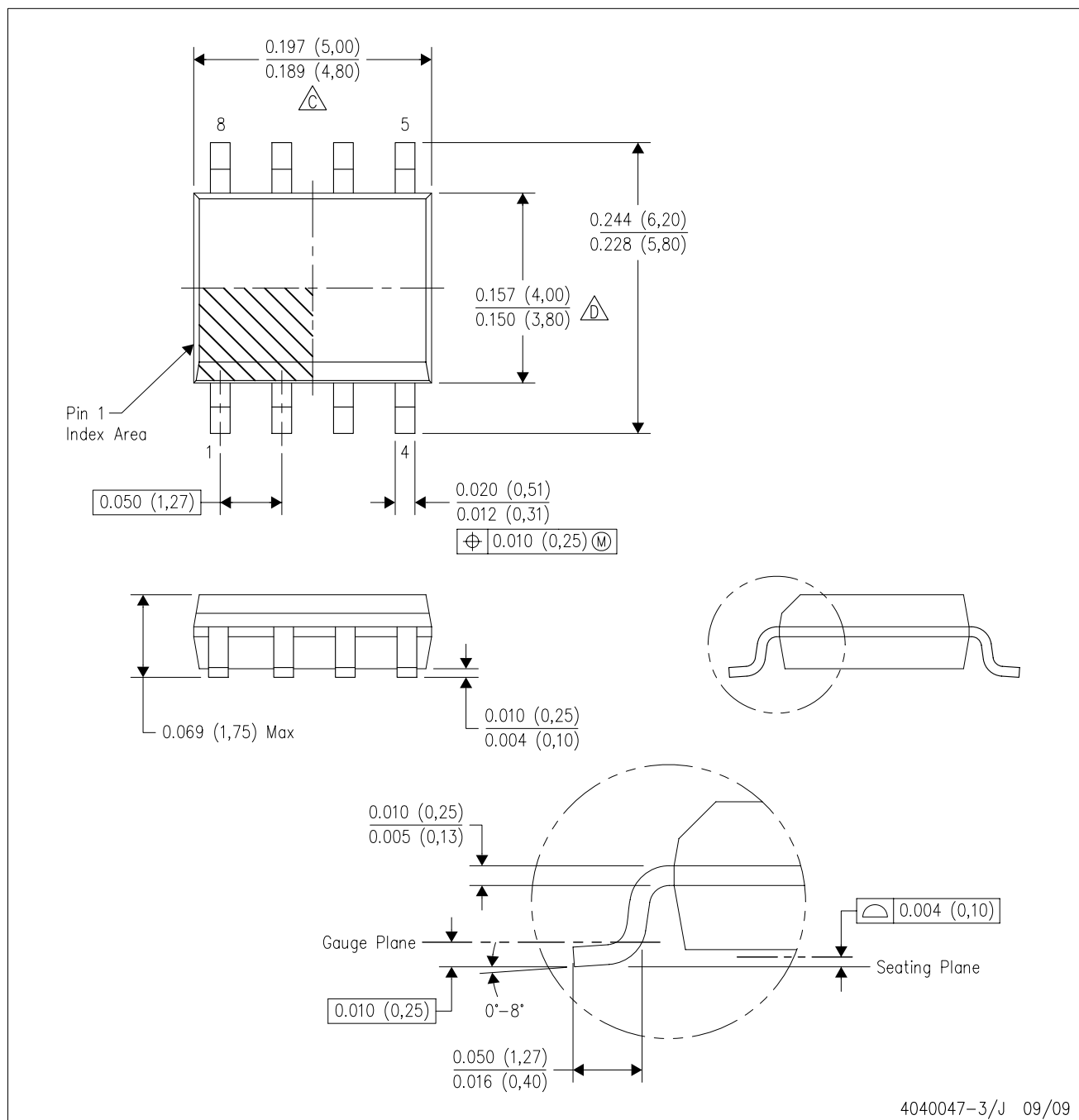
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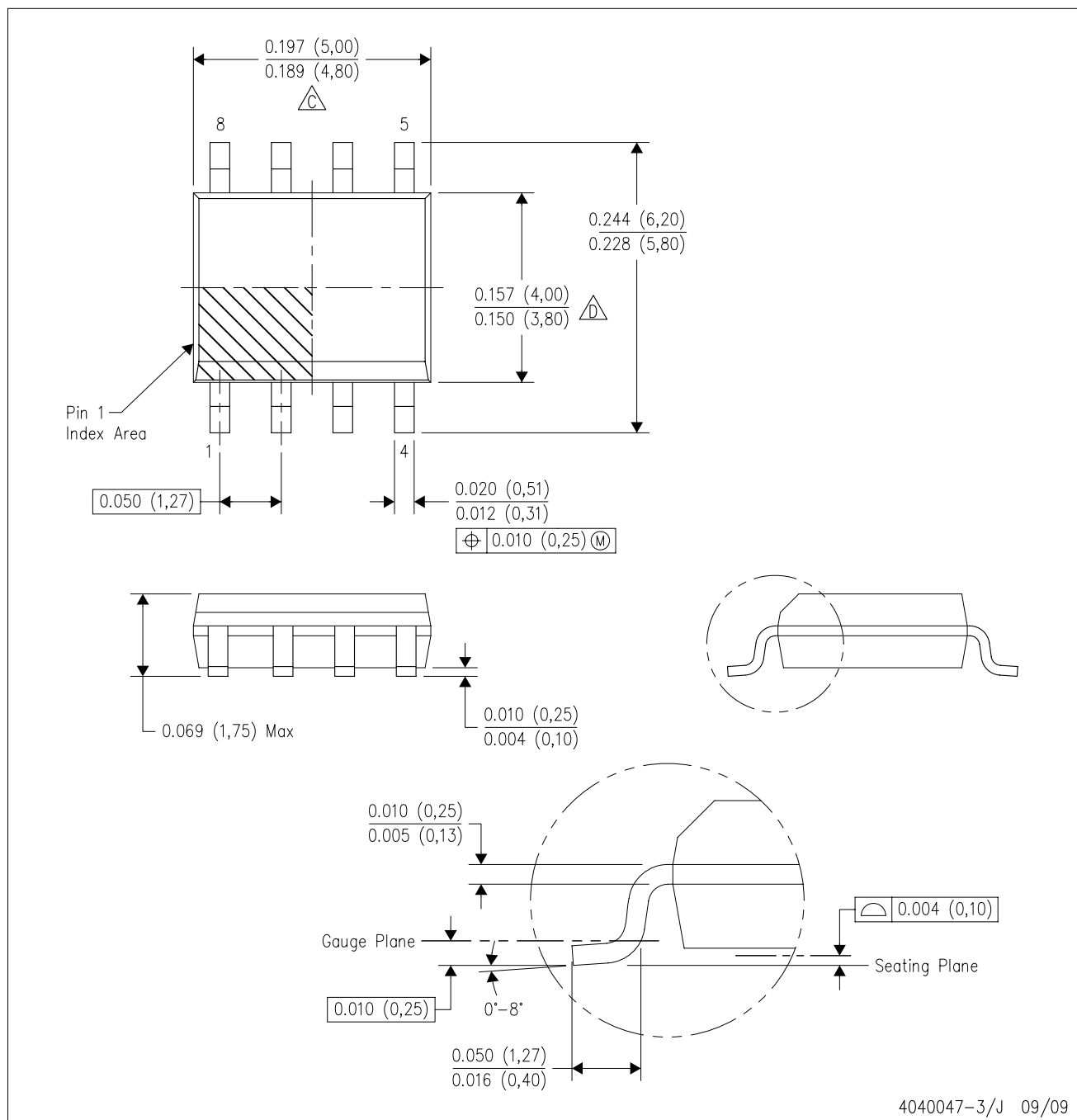
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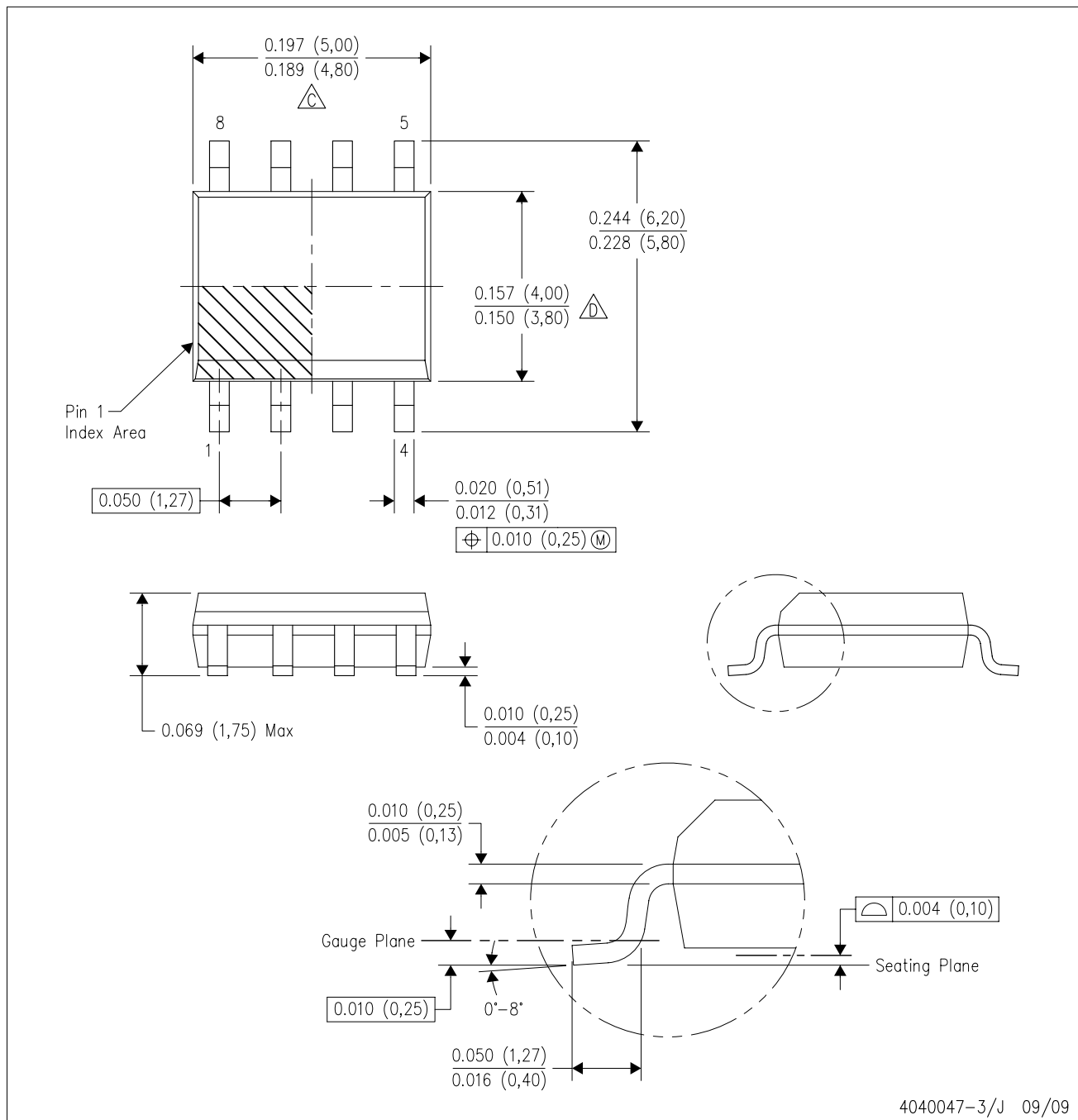
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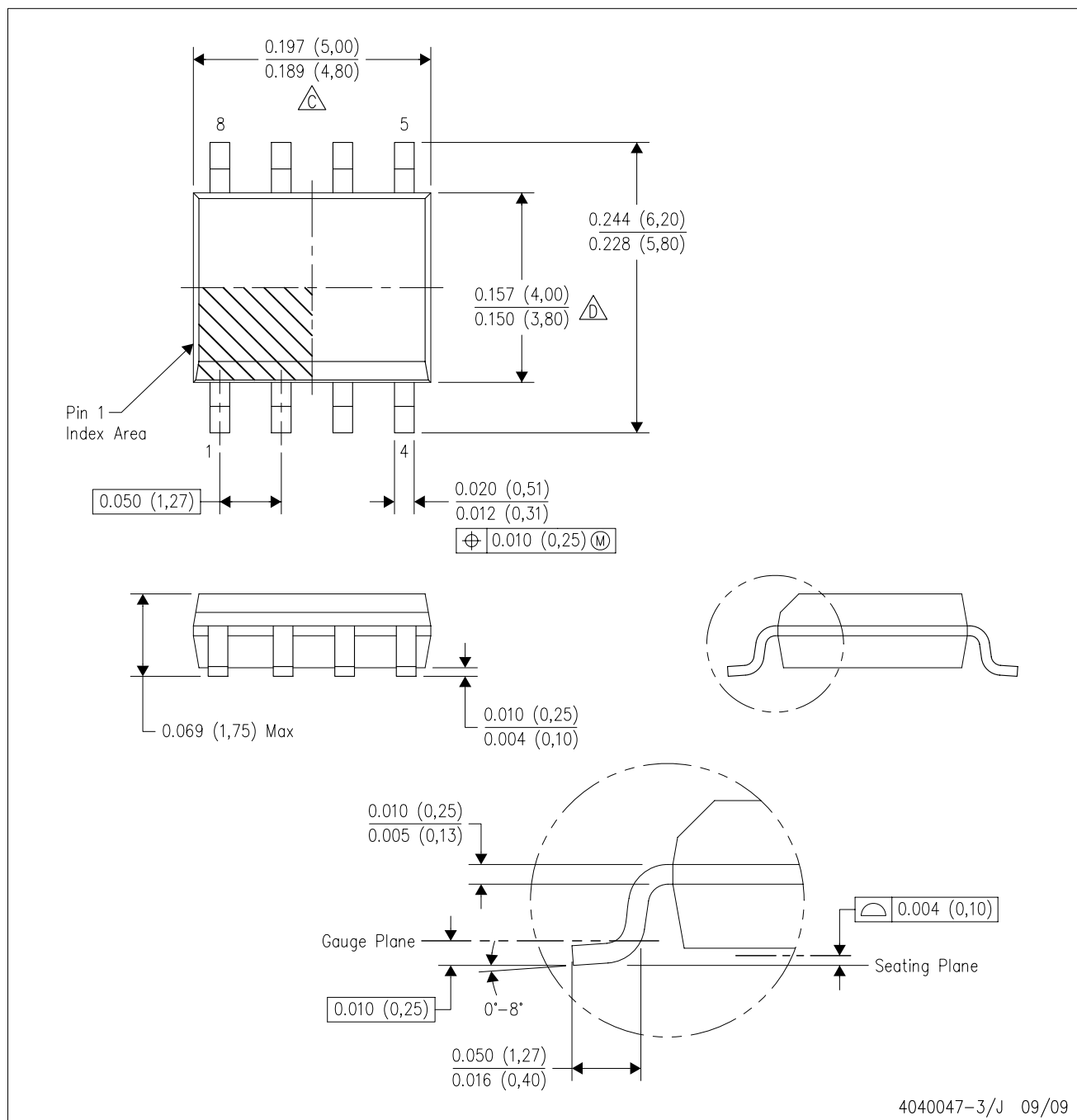
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4040047-3/J 09/09

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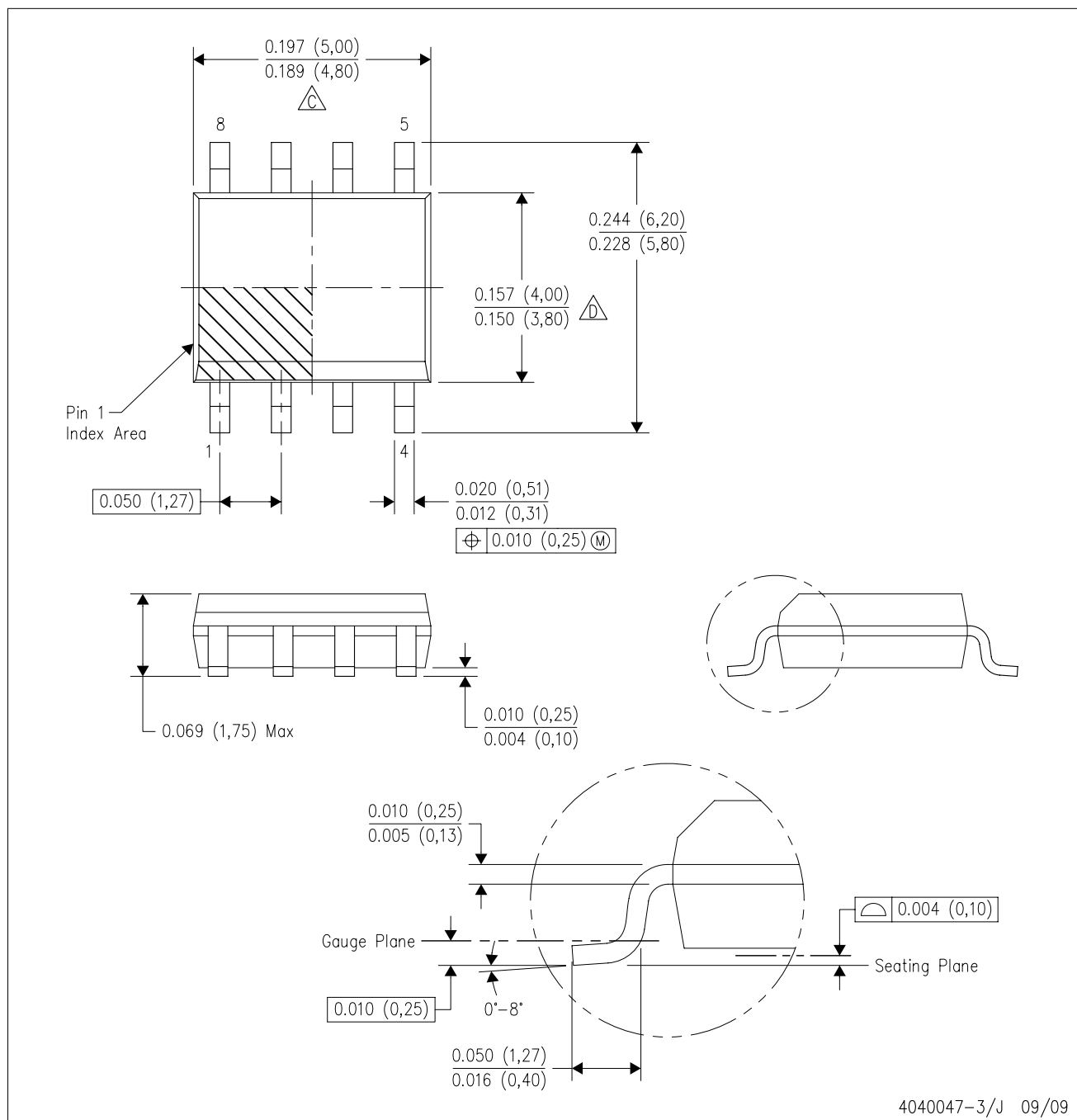
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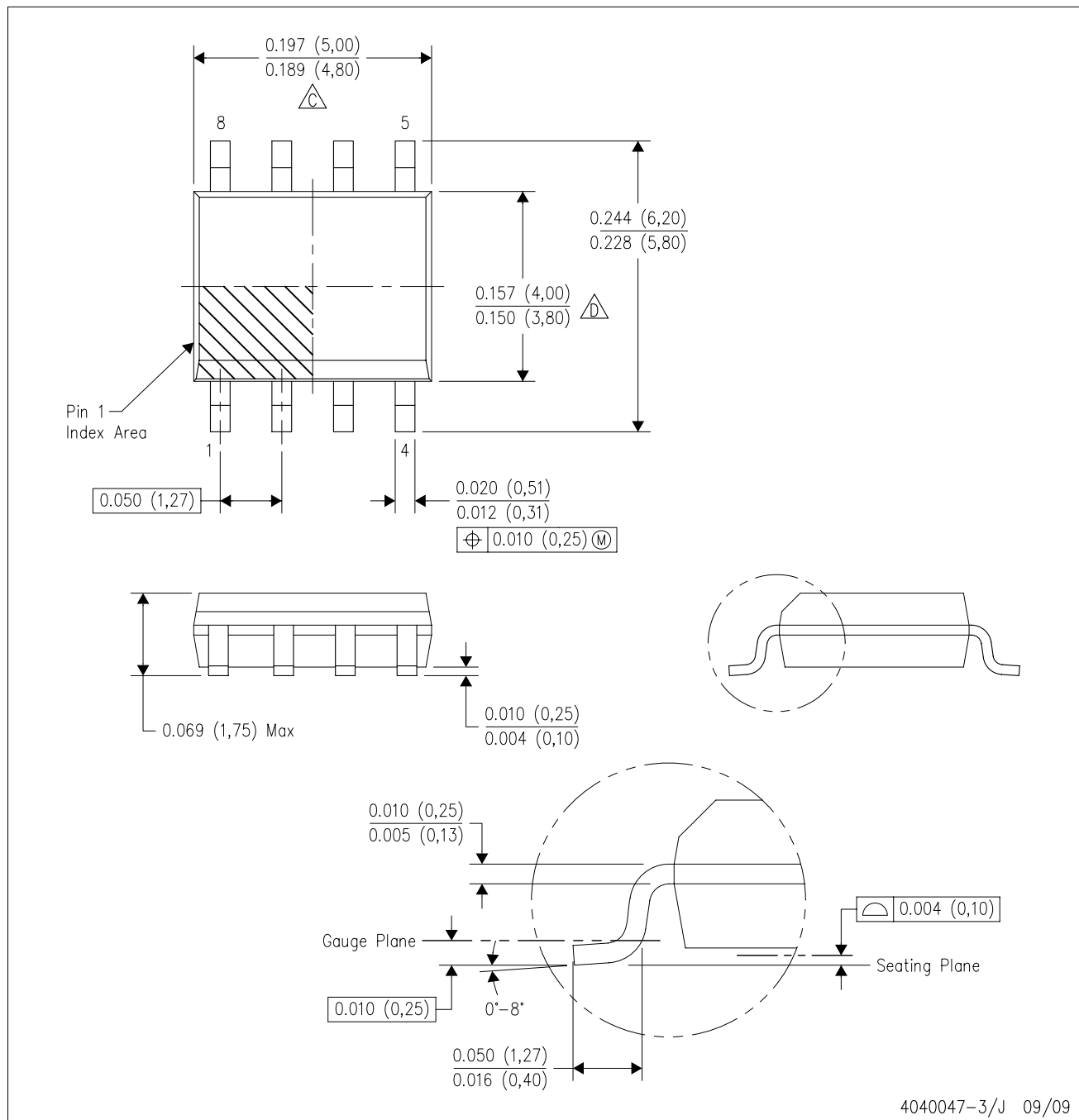
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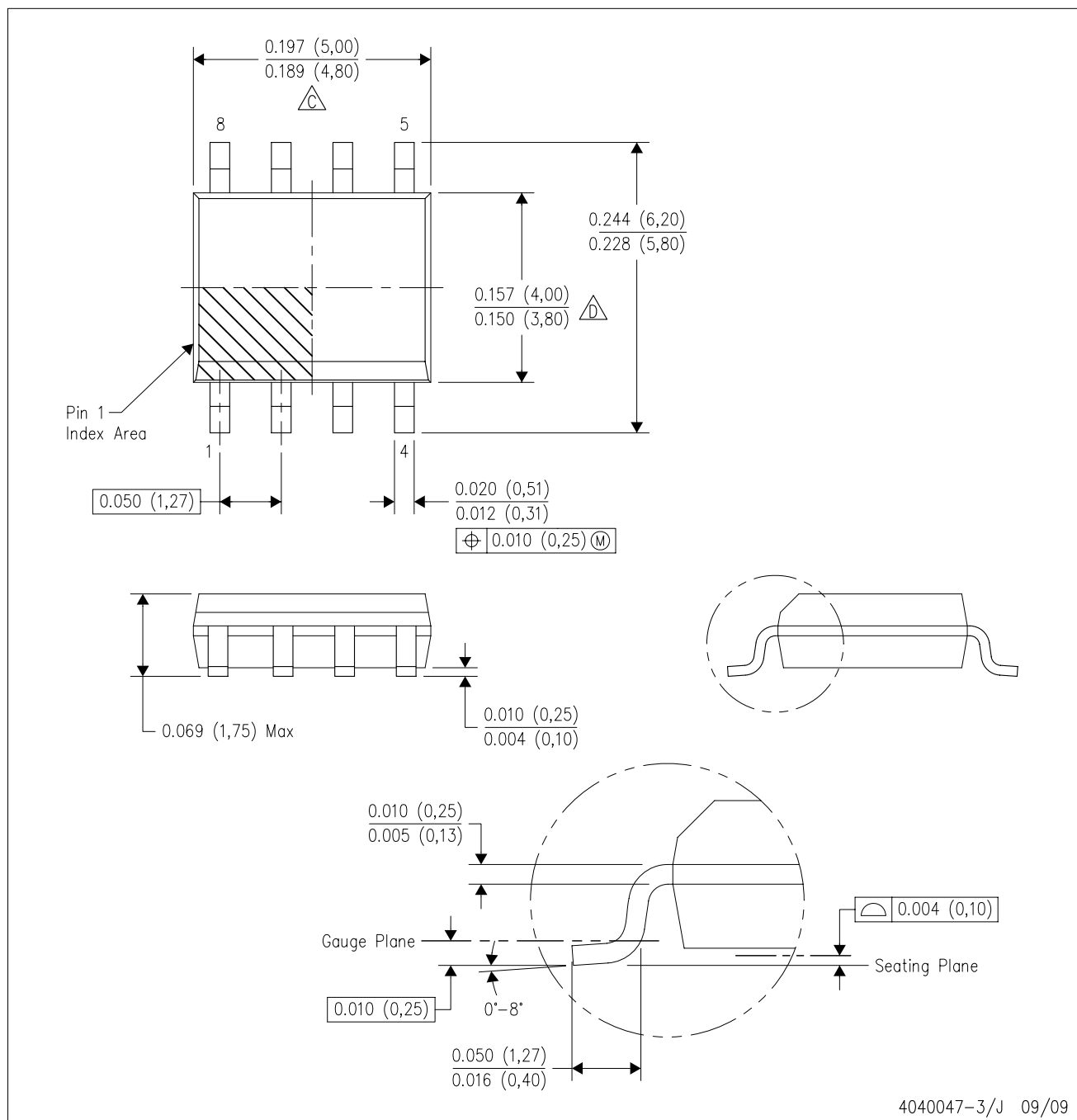
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



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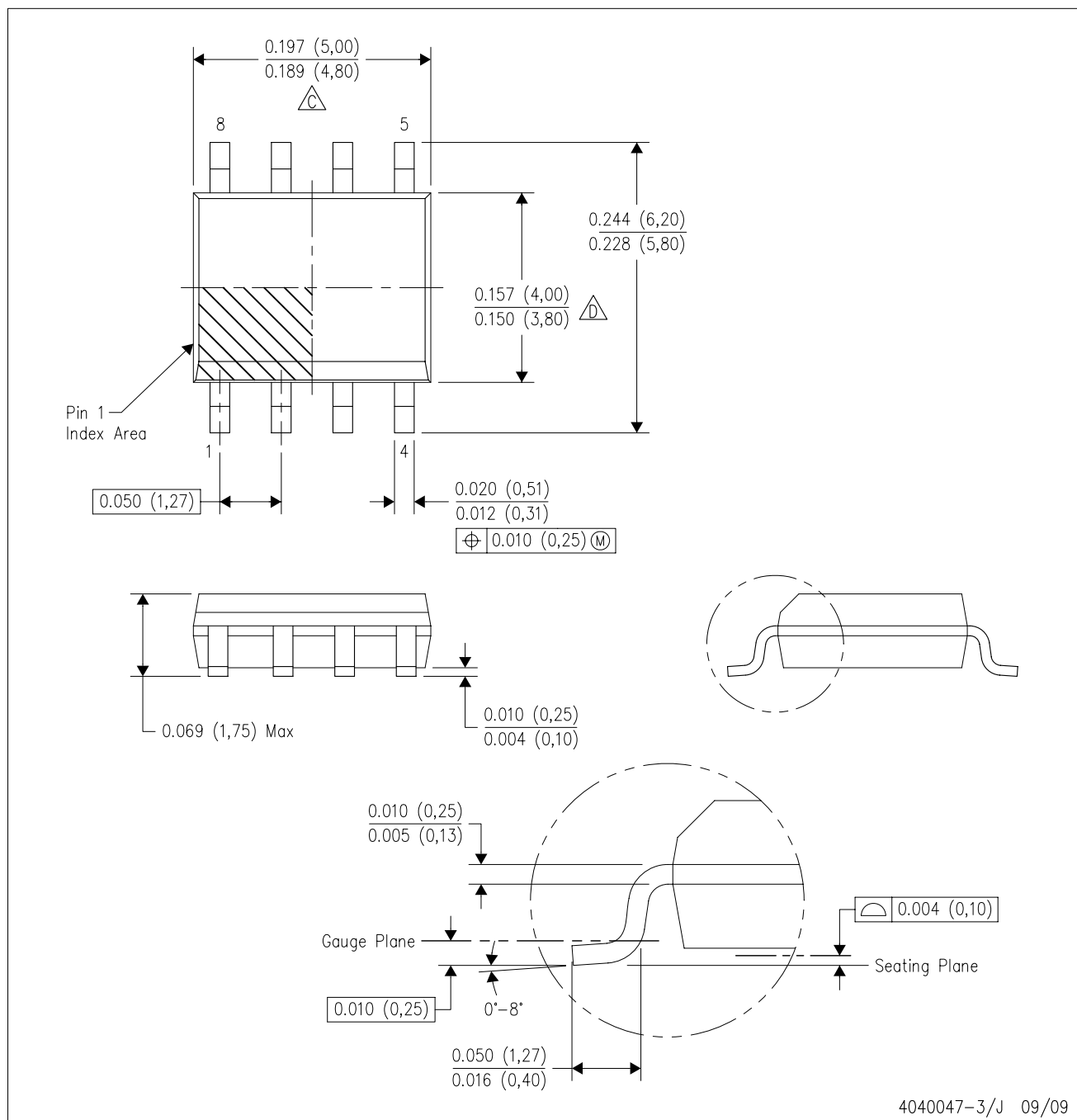
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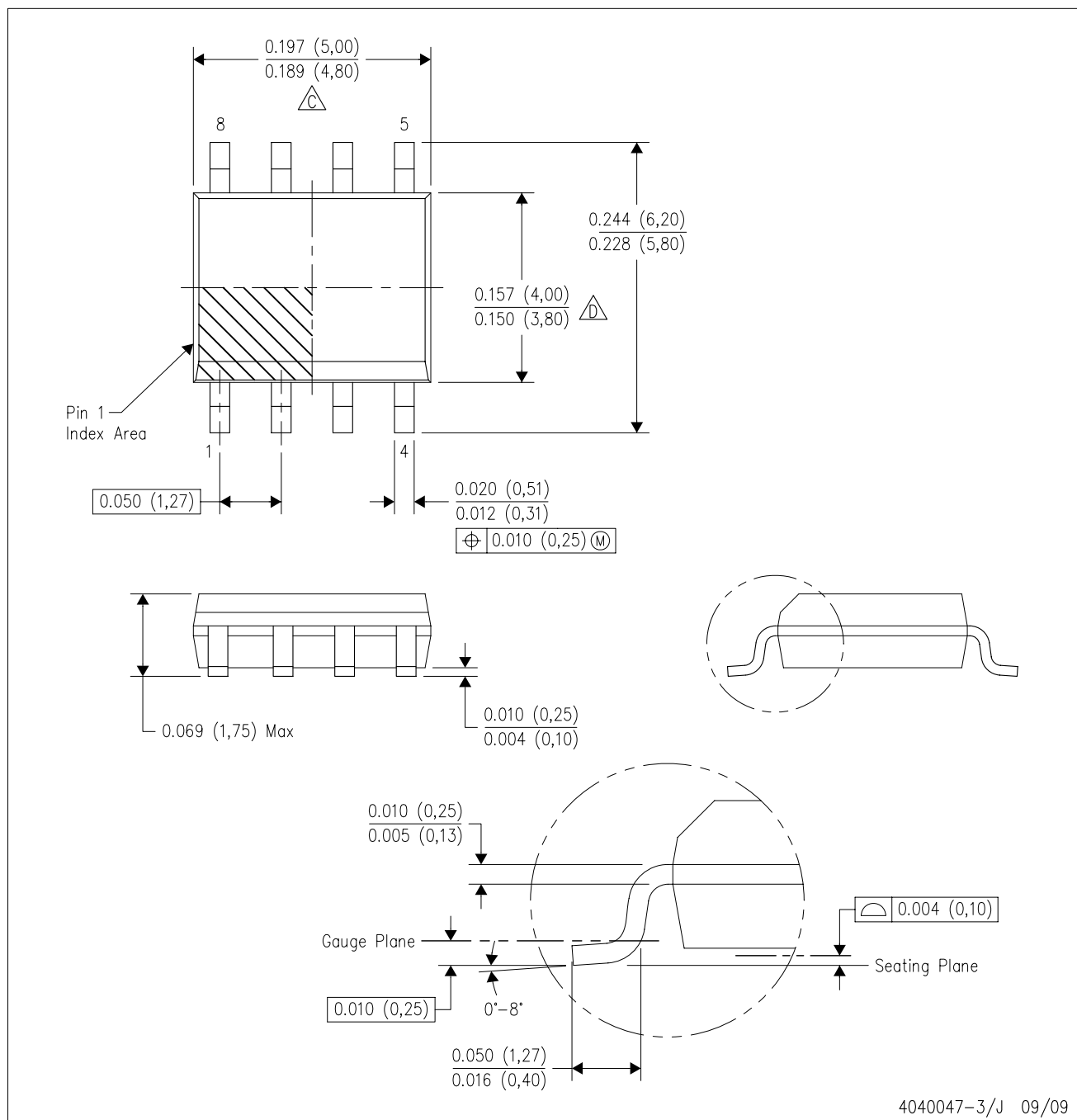
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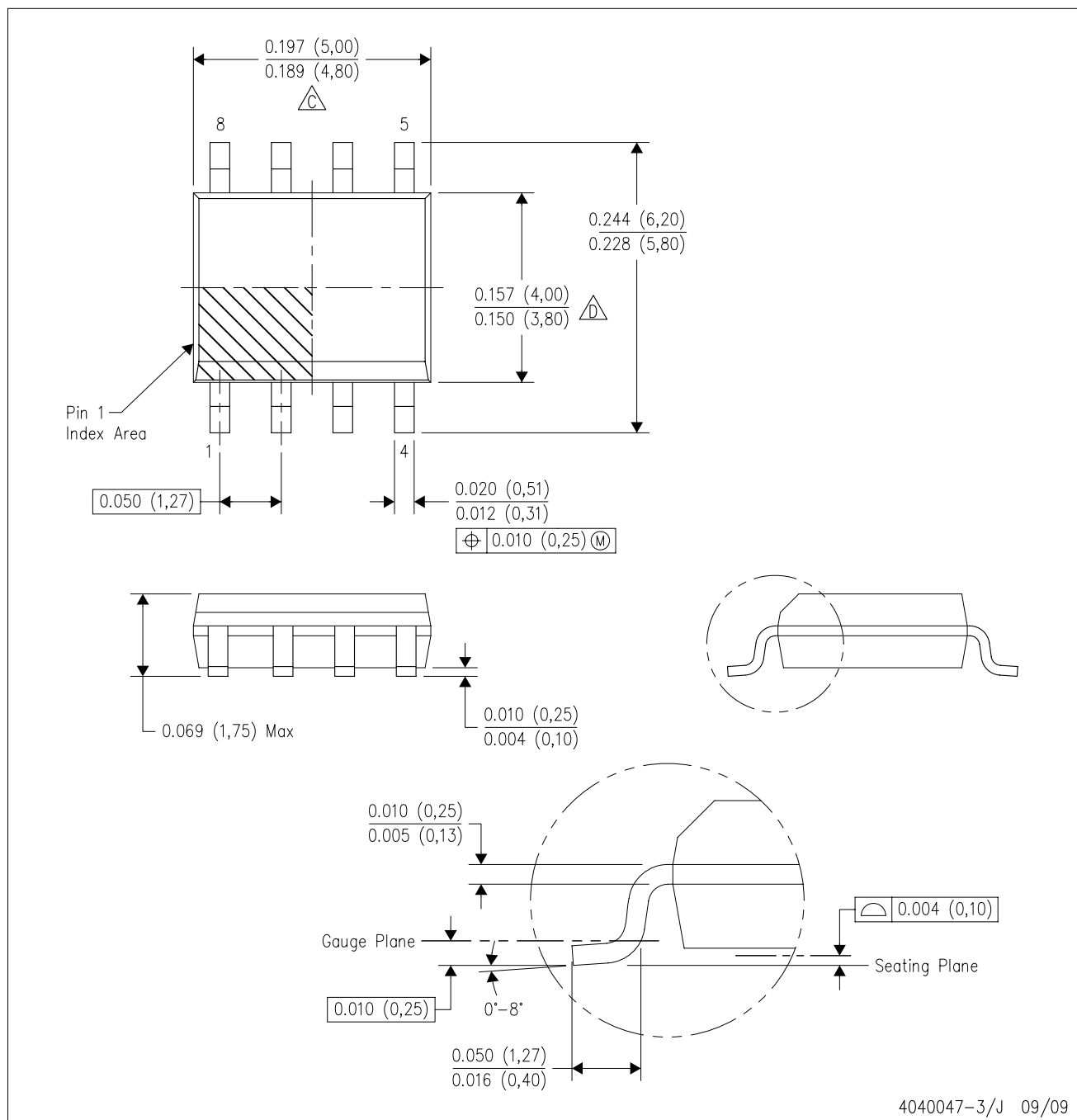
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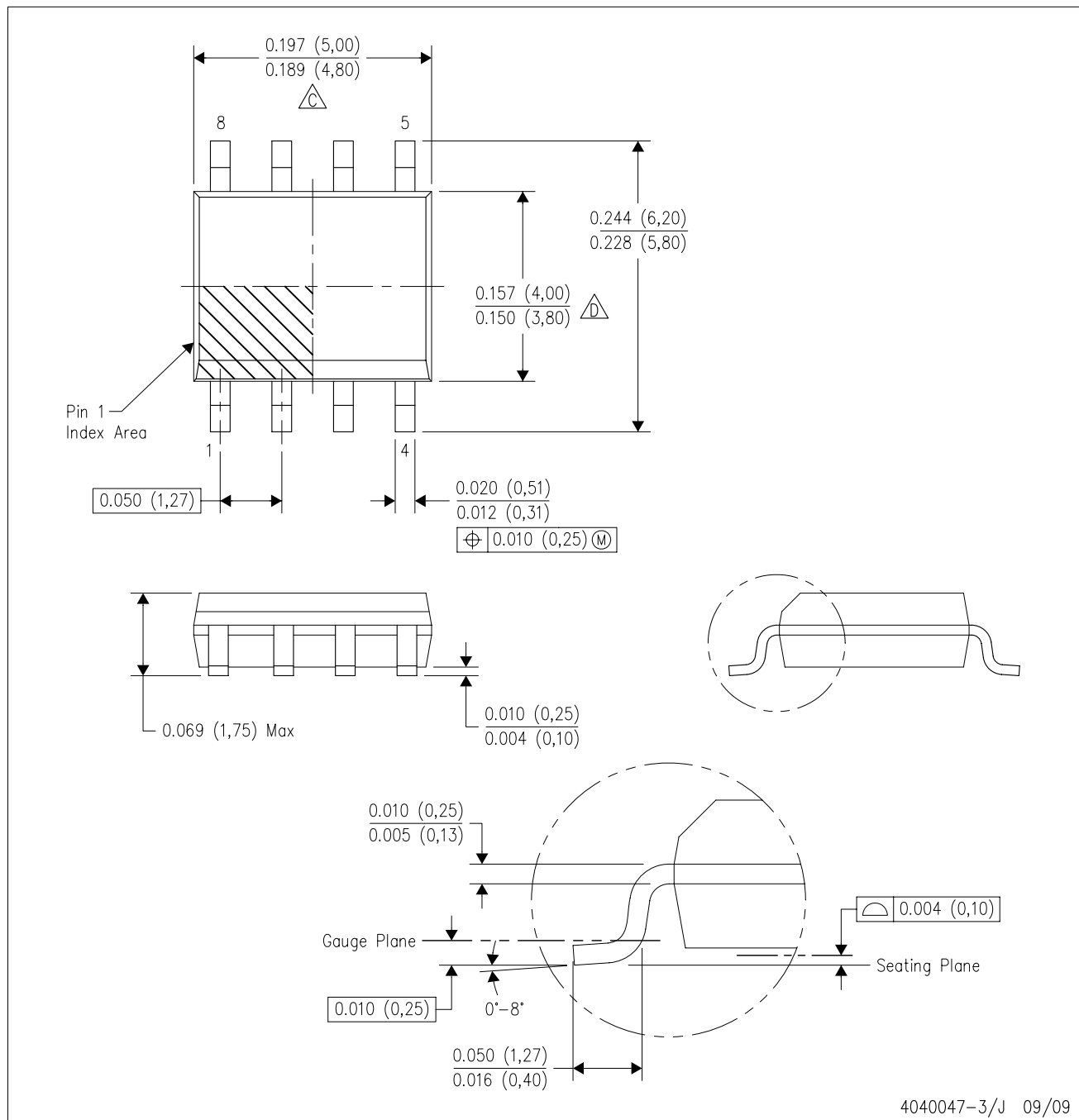
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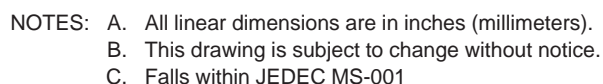
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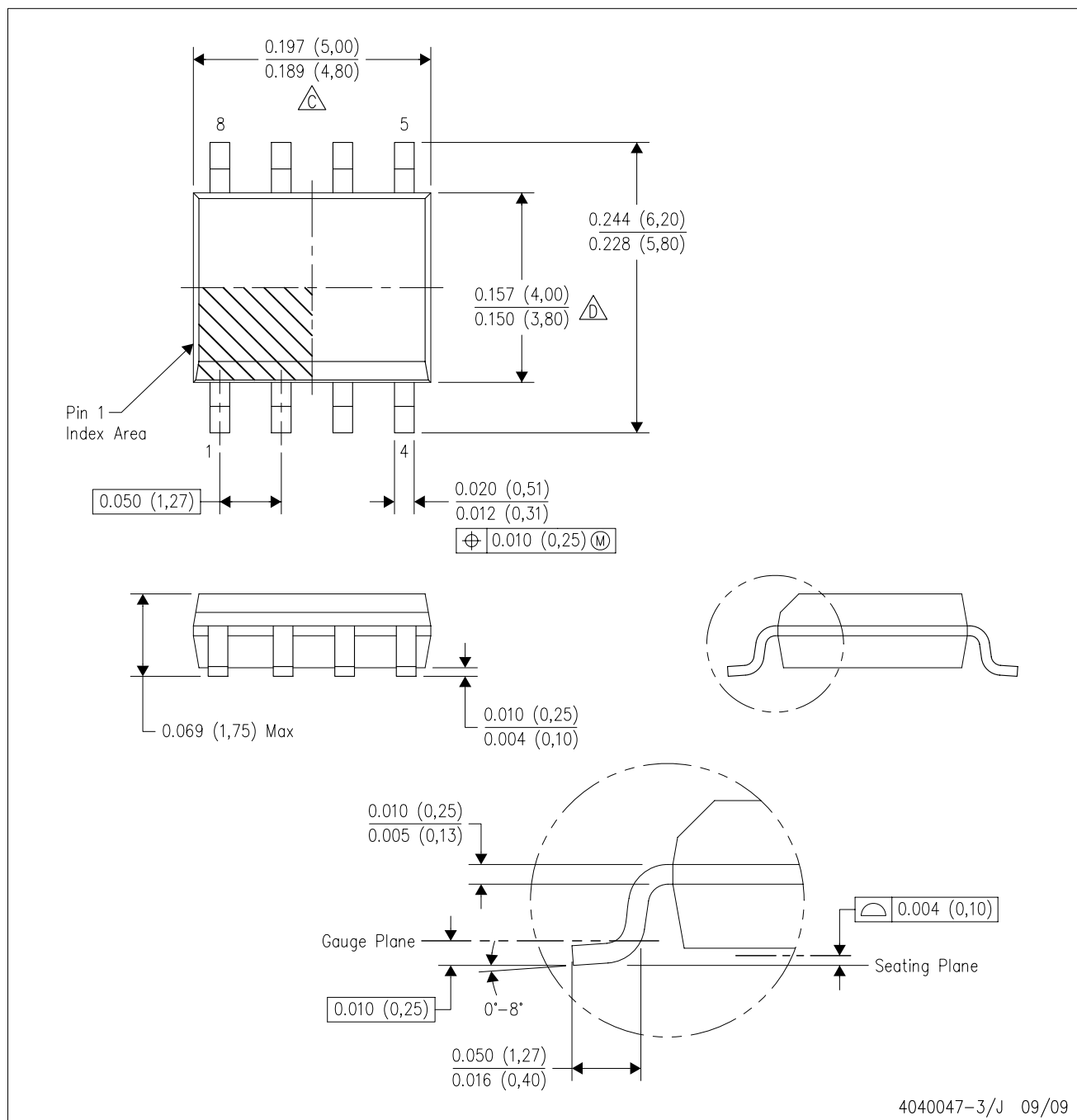
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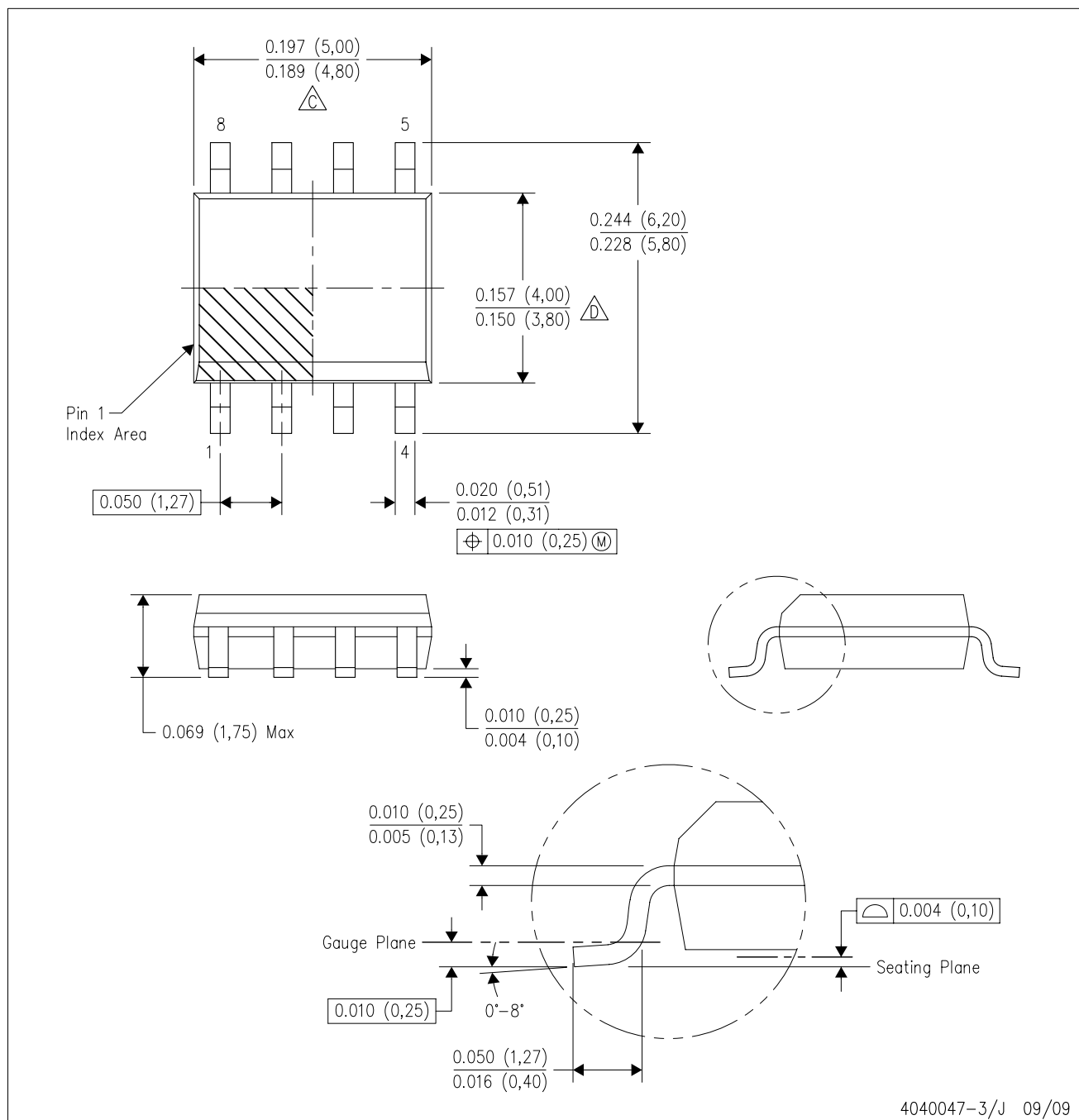
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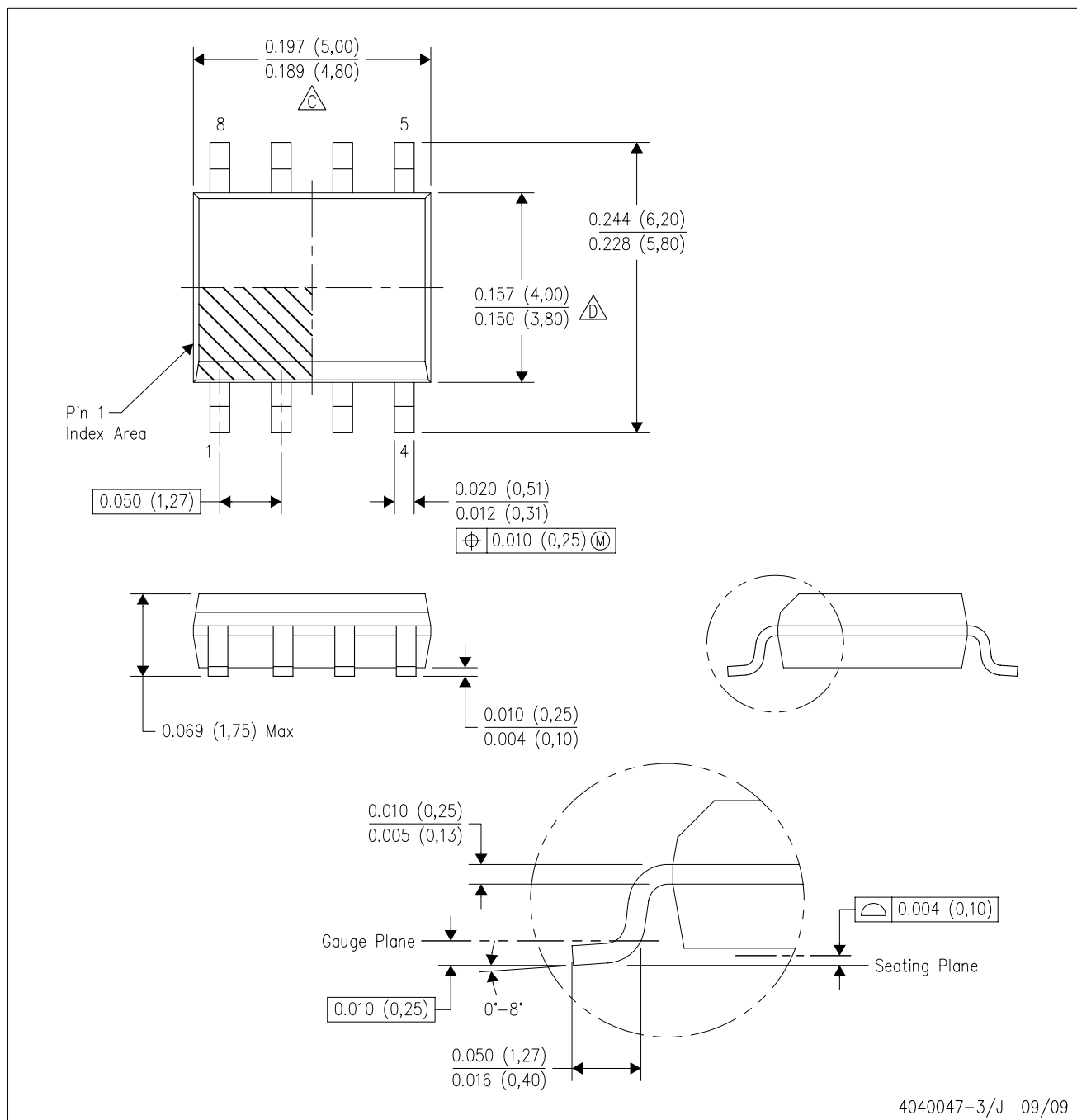
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

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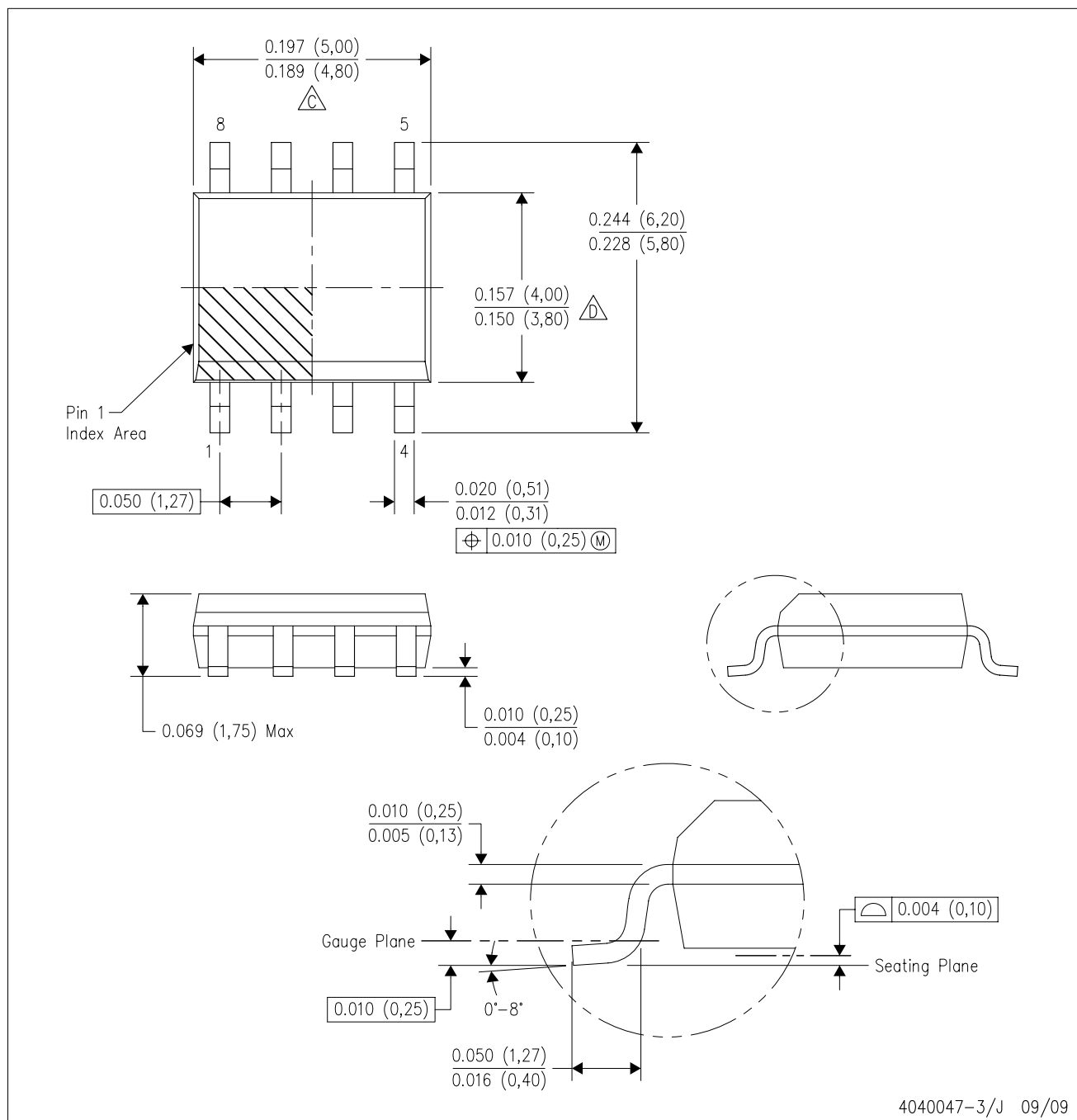
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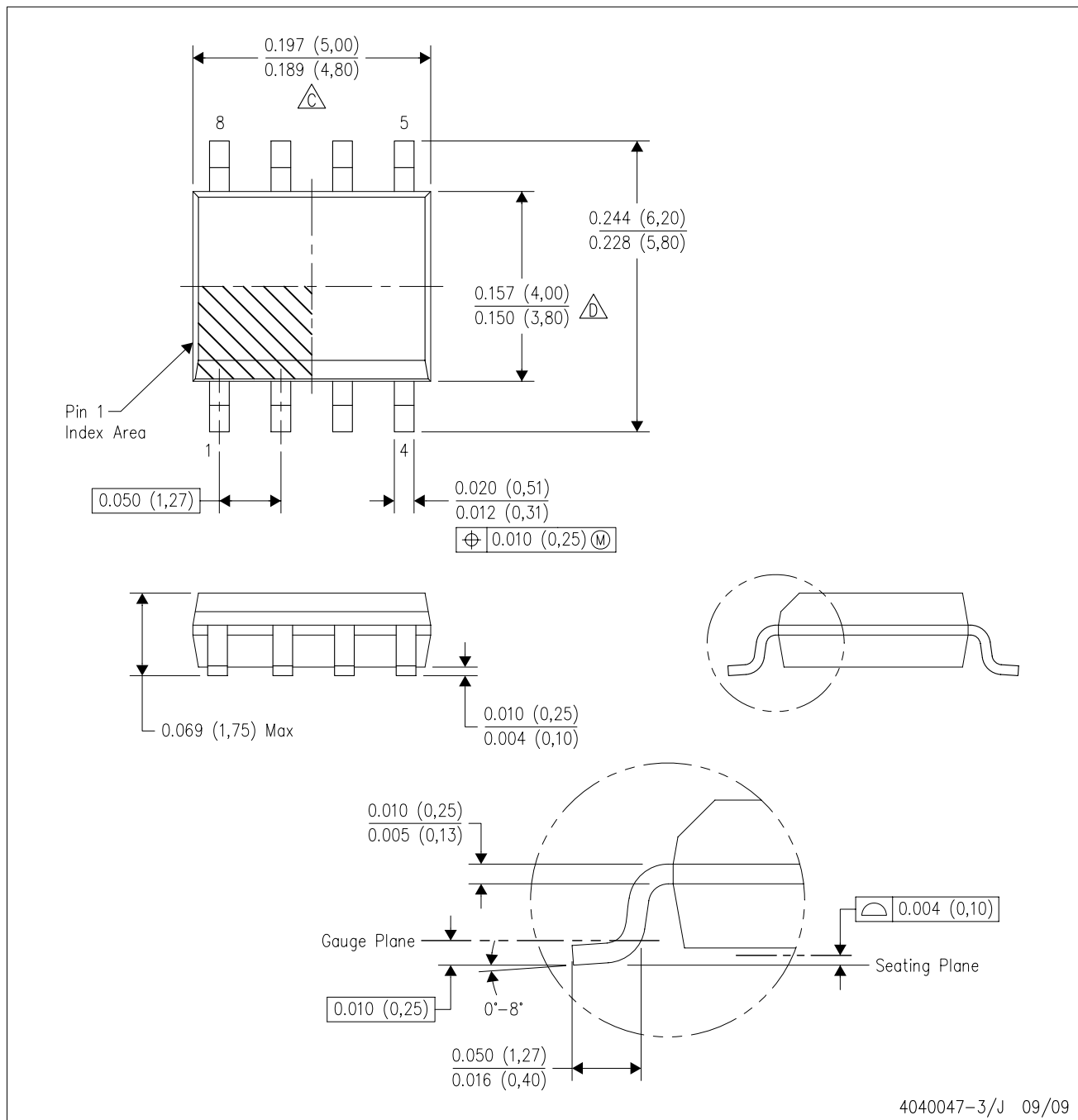
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4040047-3/J 09/09

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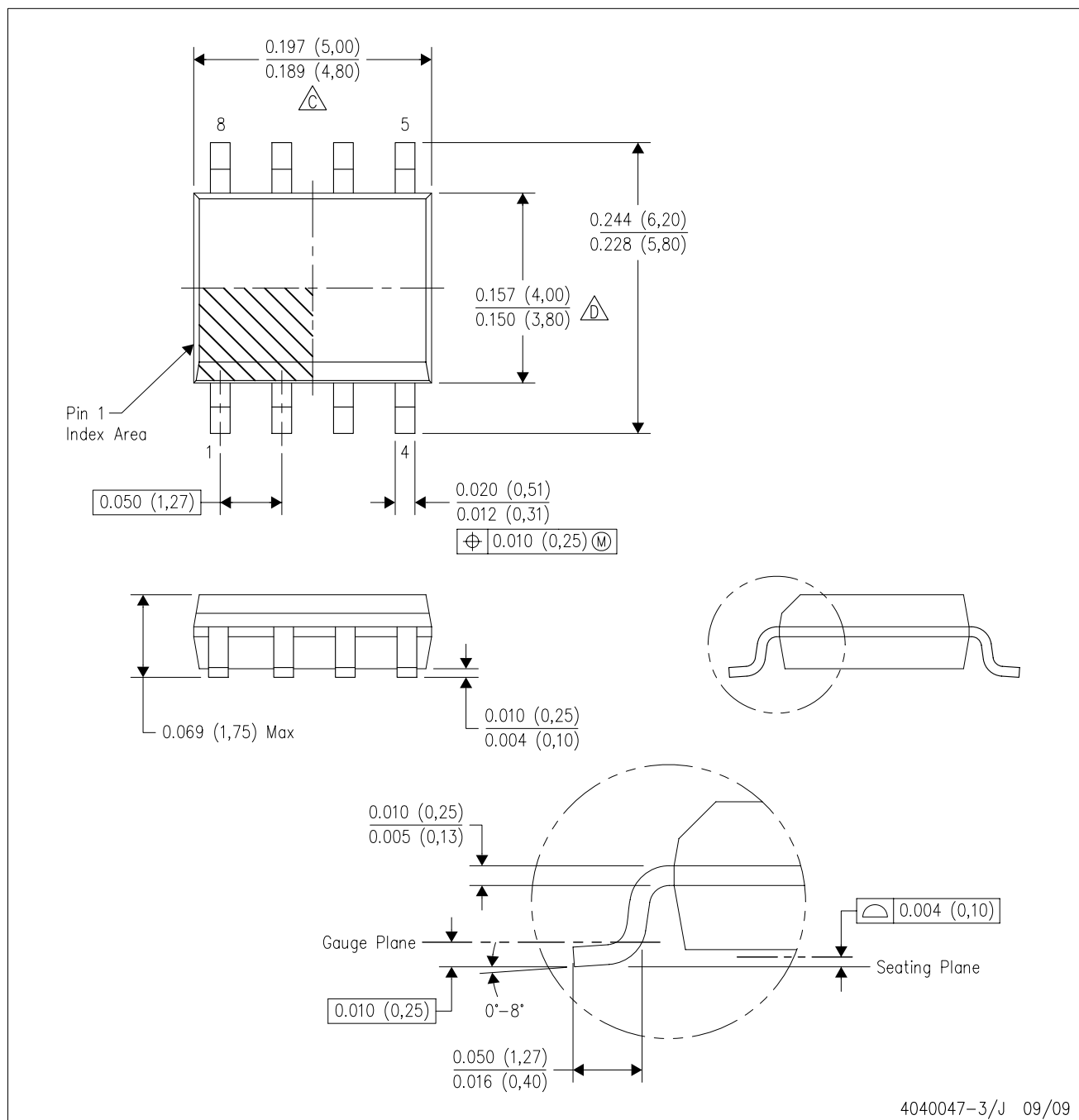
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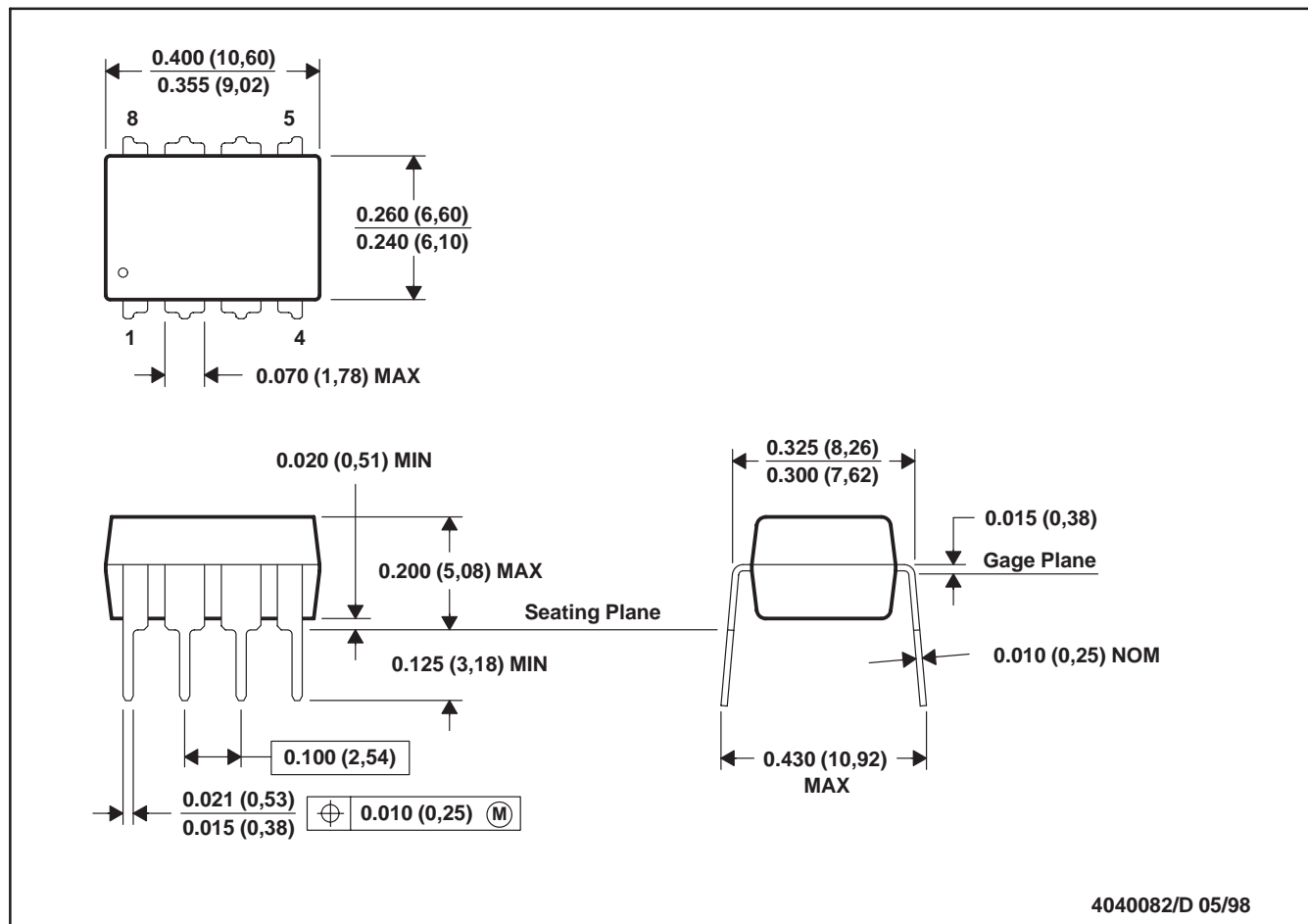
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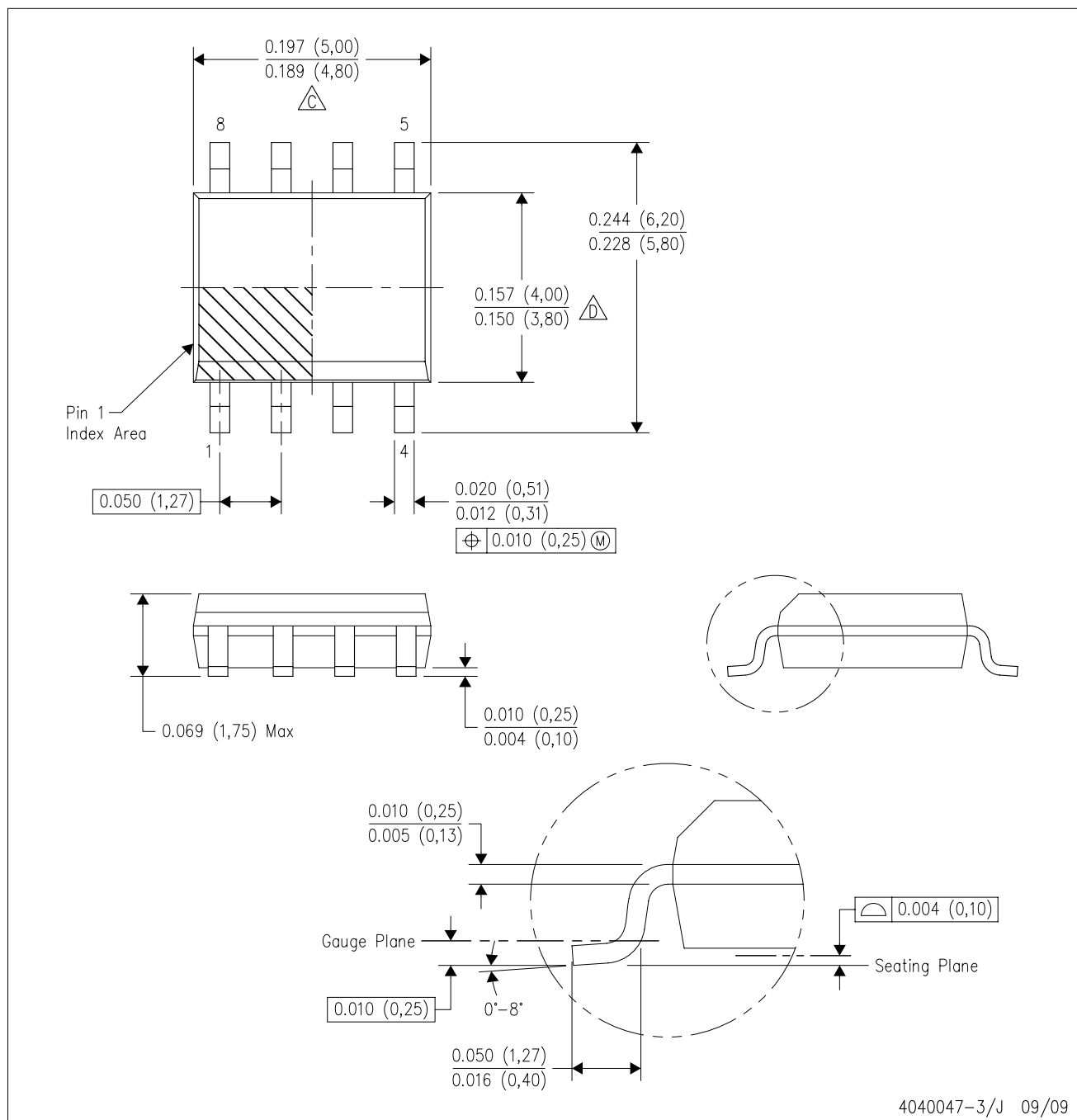
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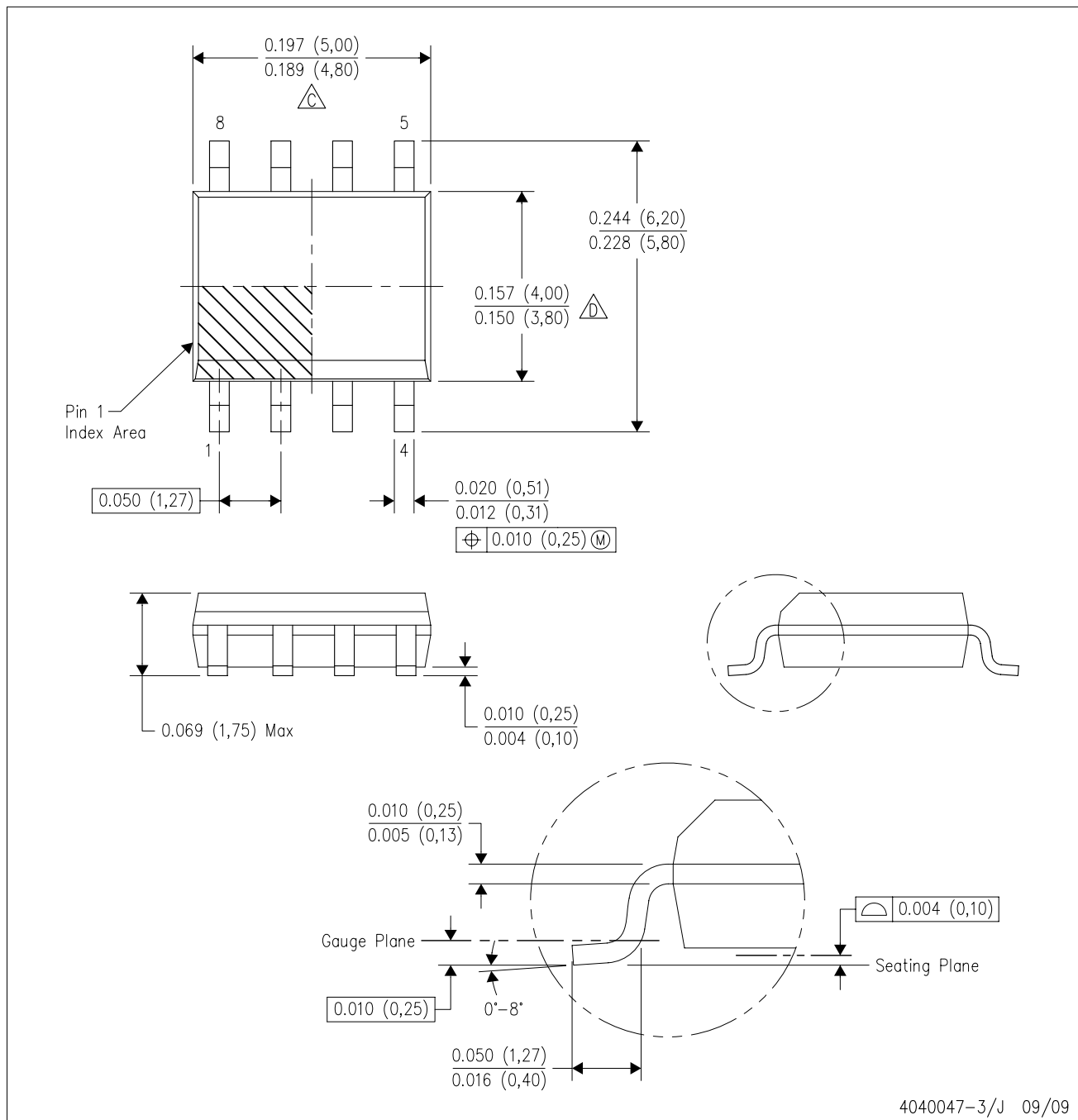
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4040047-3/J 09/09

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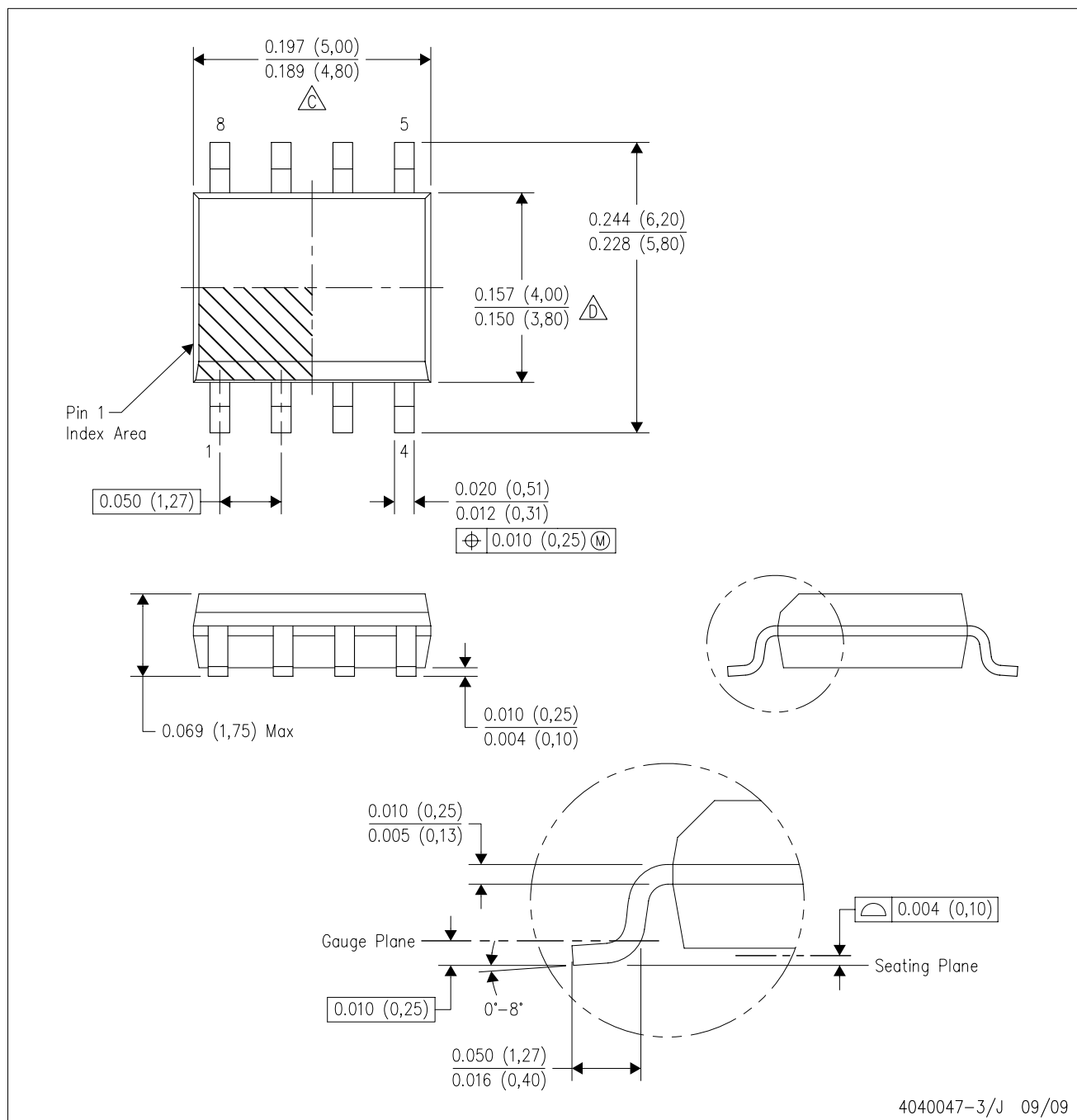
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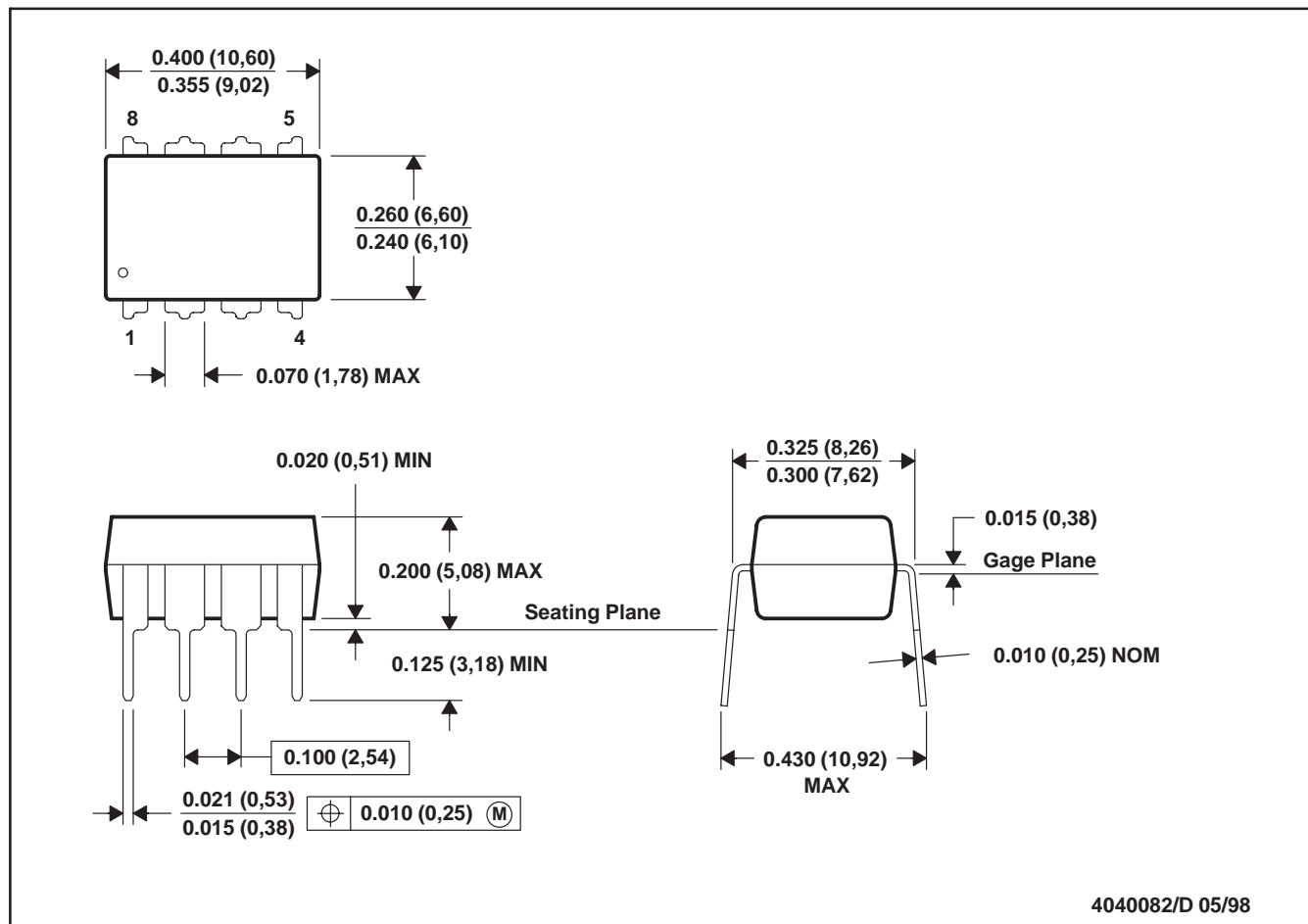


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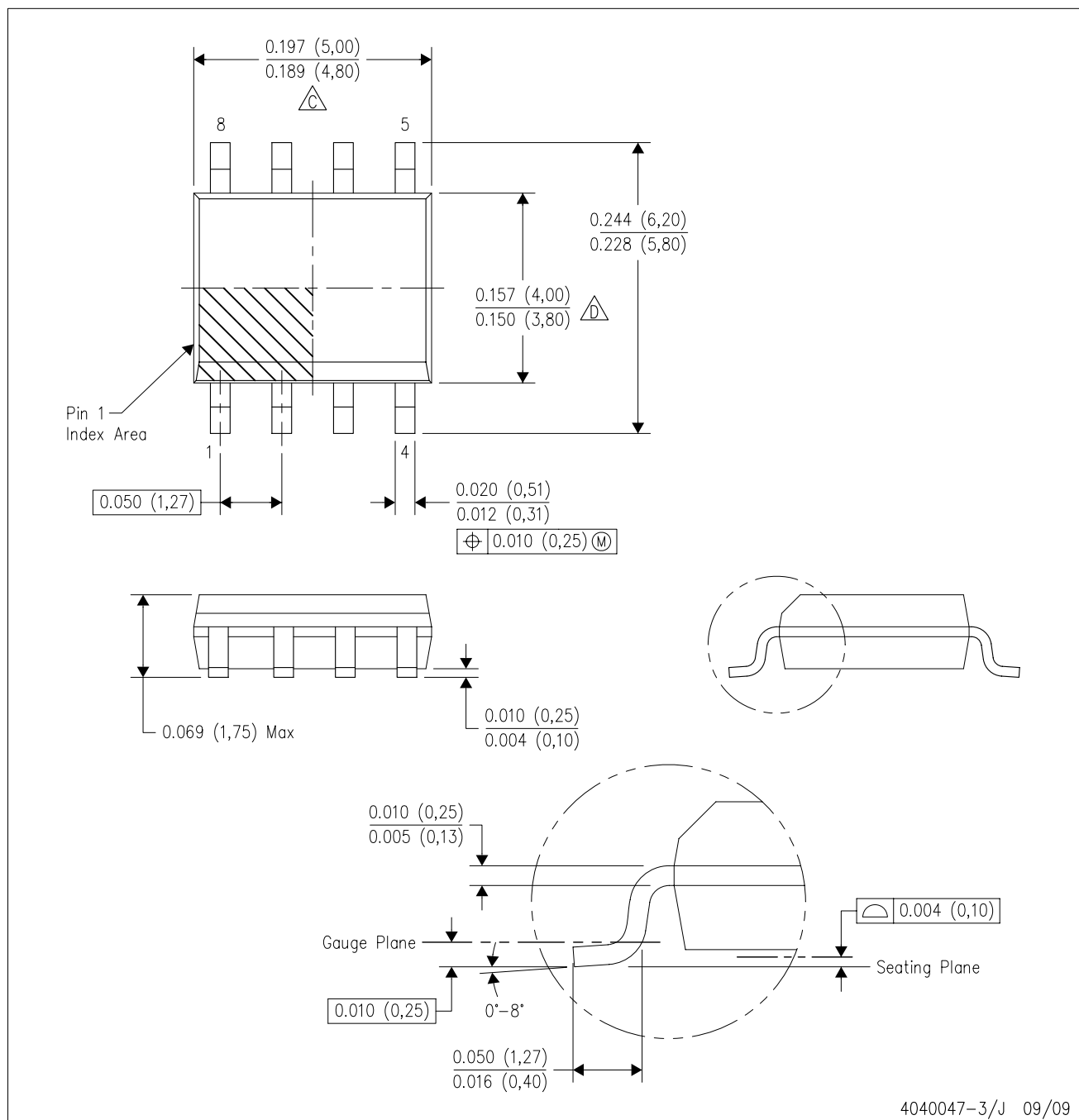
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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PACKAGING INFORMATION

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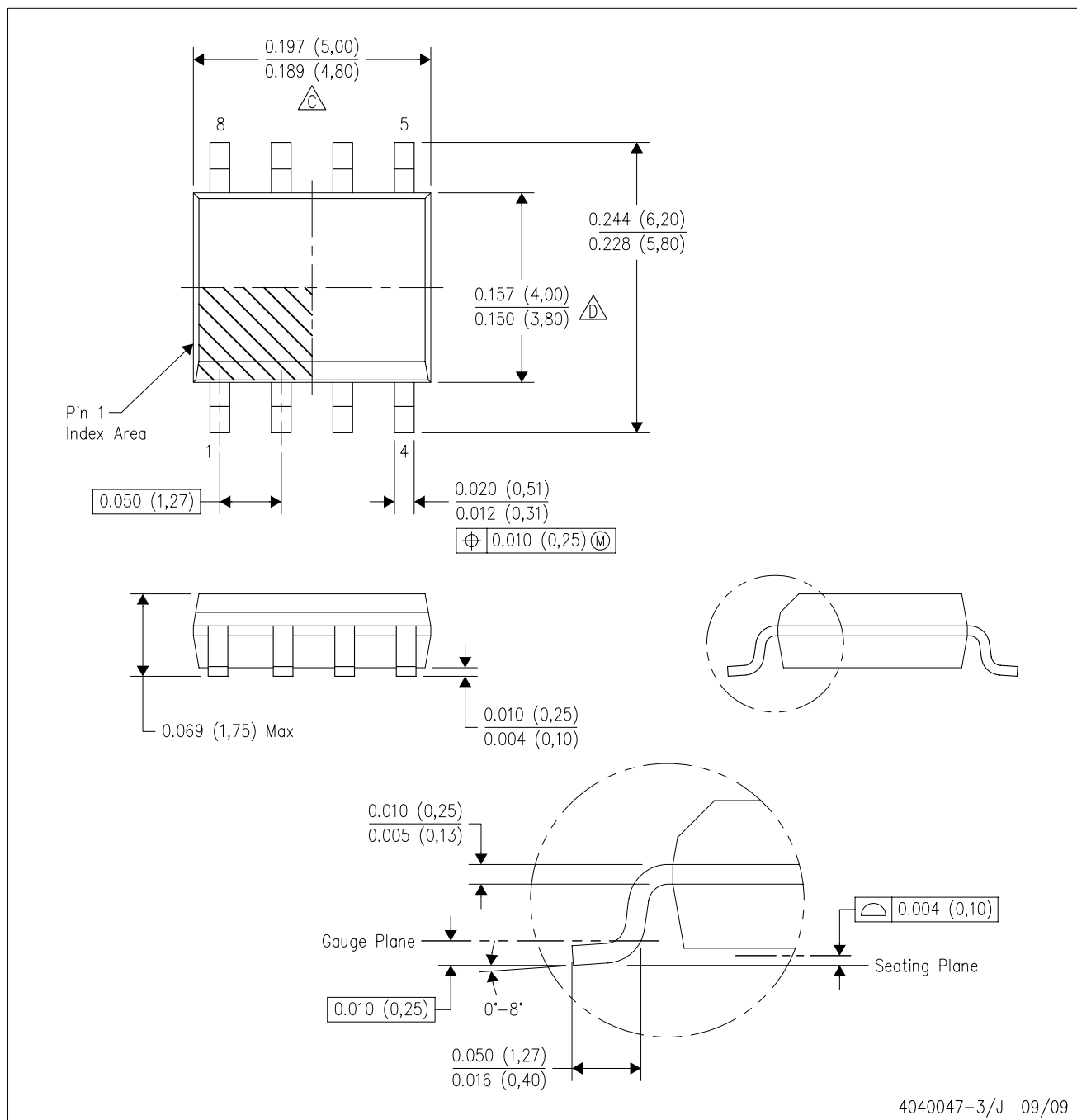
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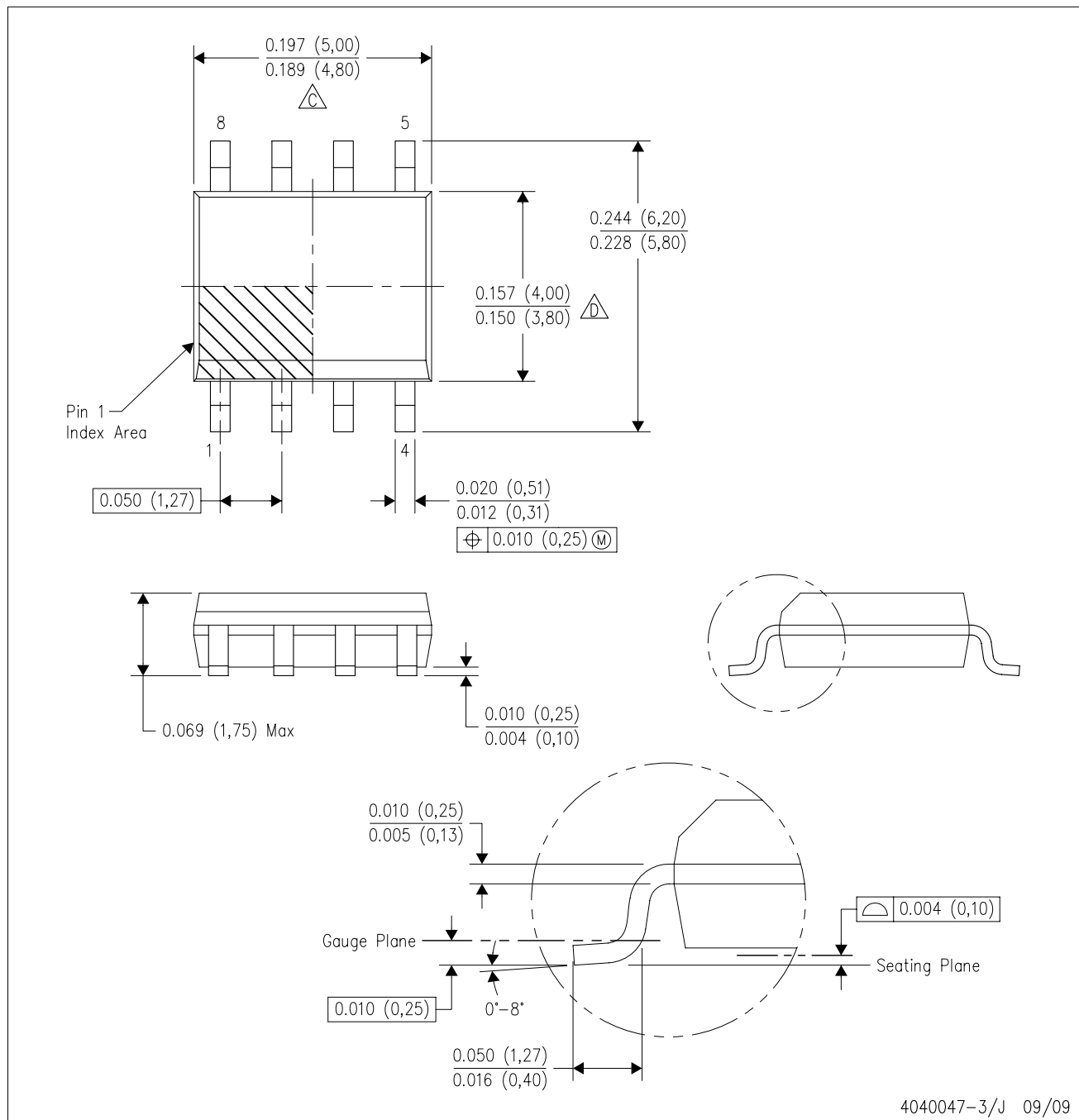
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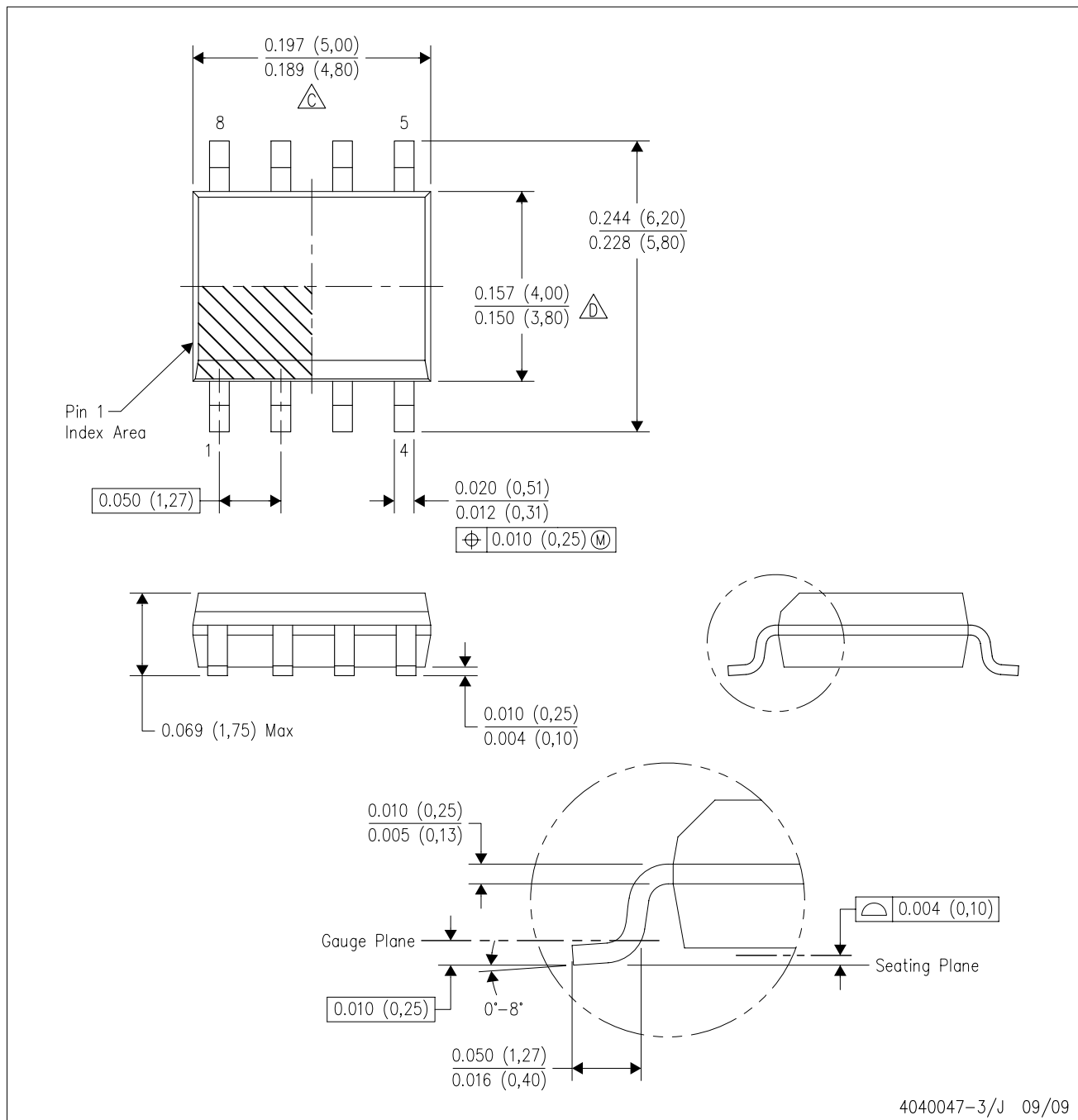
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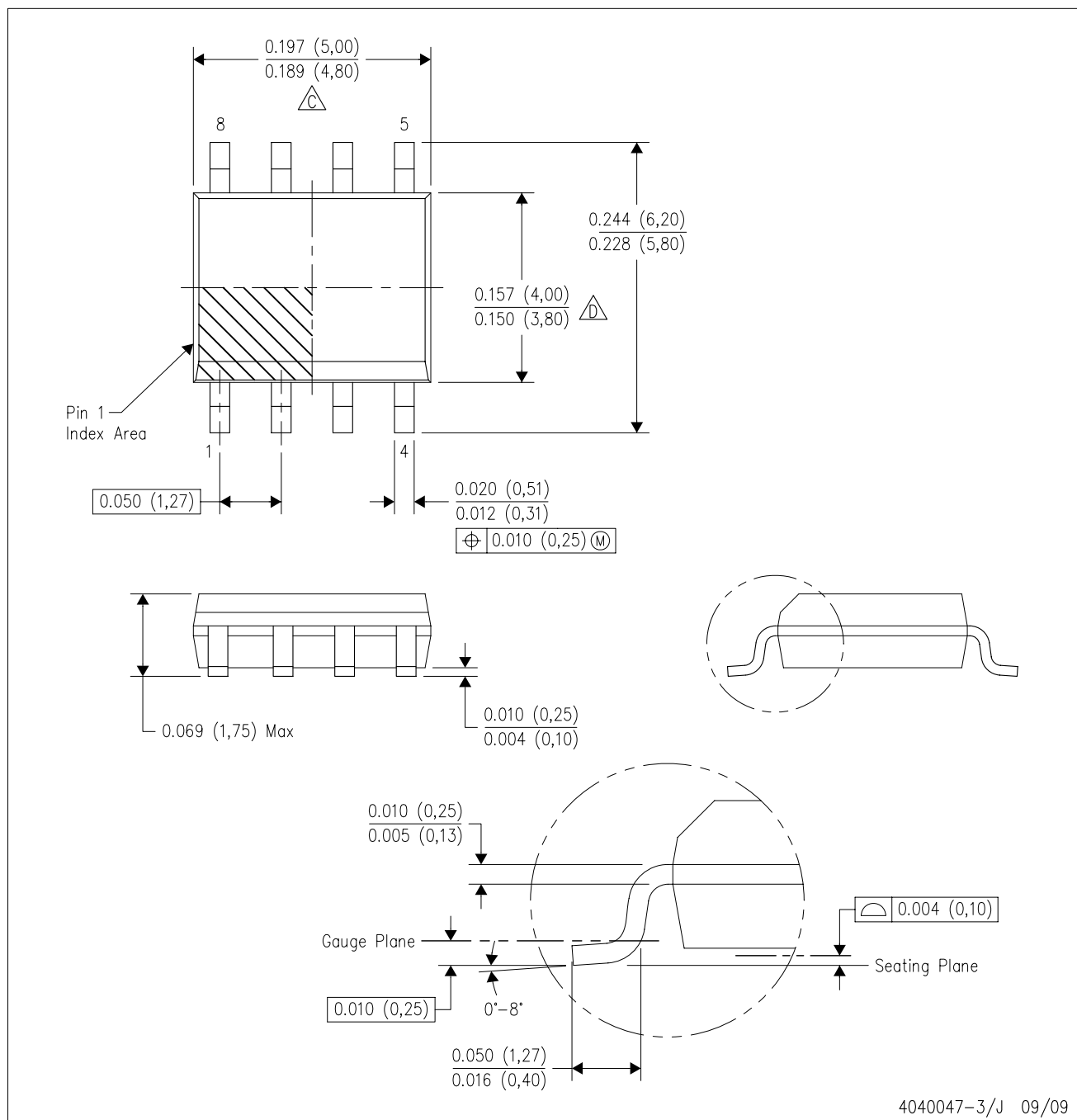
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4040047-3/J 09/09

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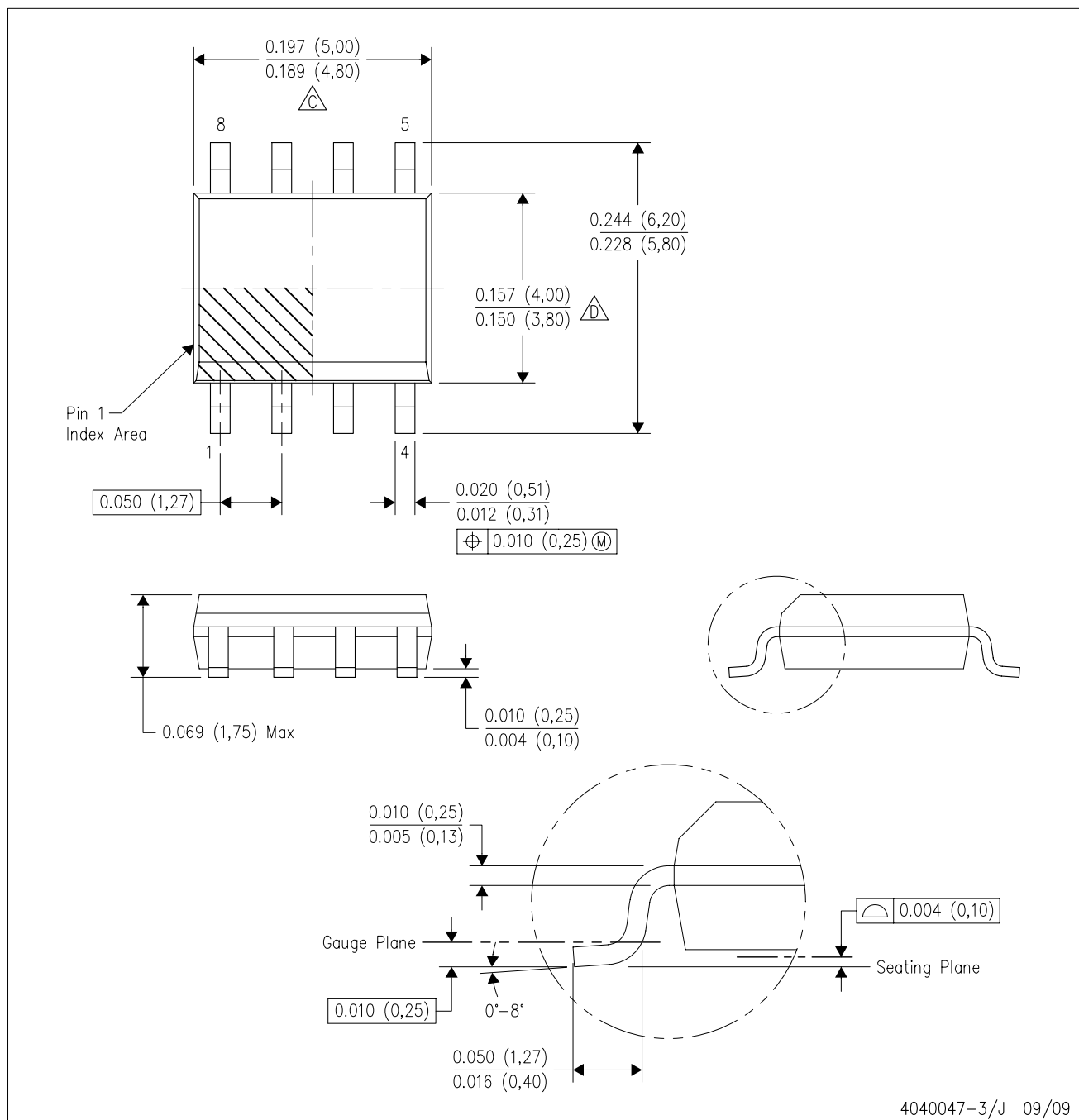
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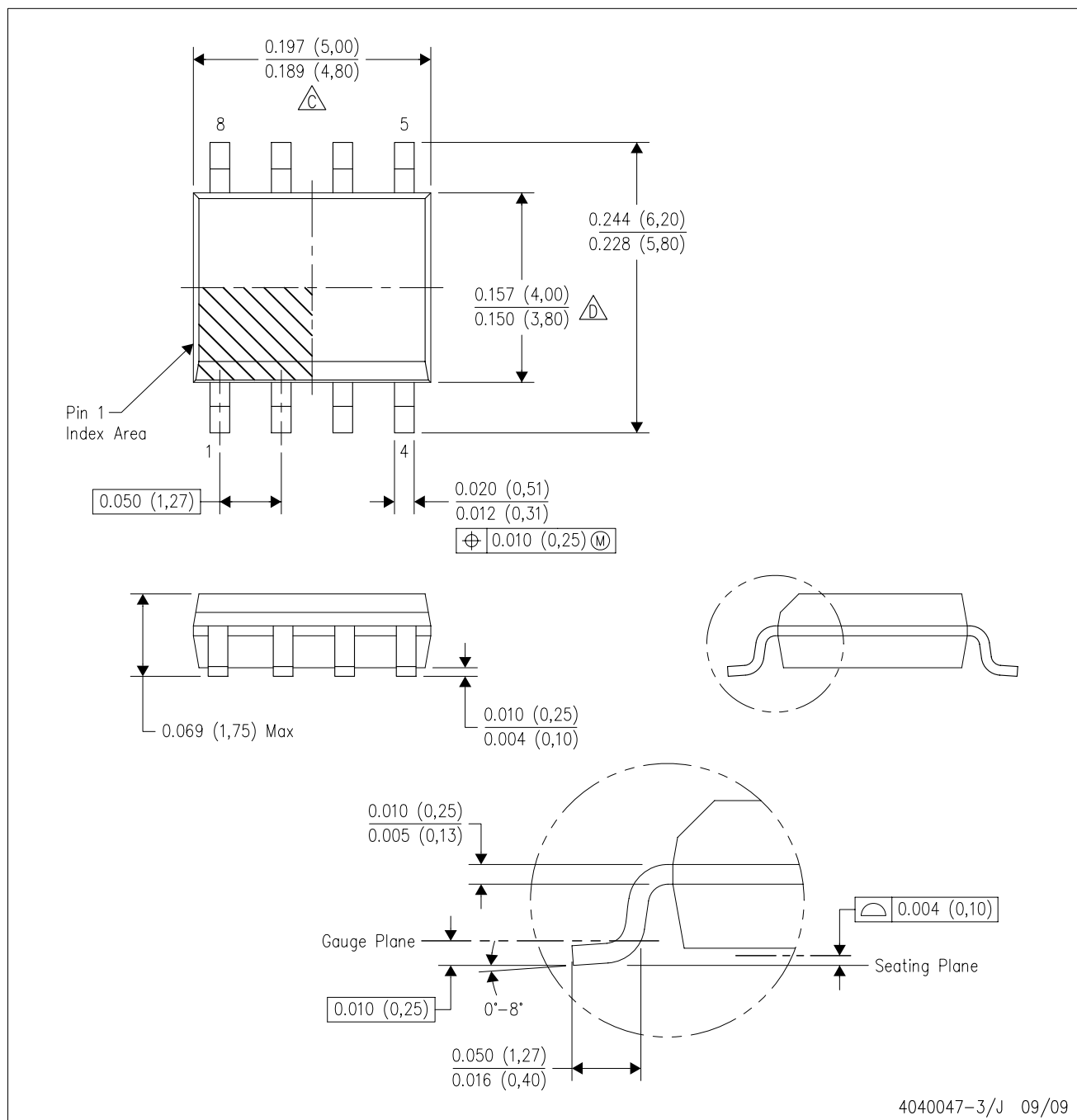
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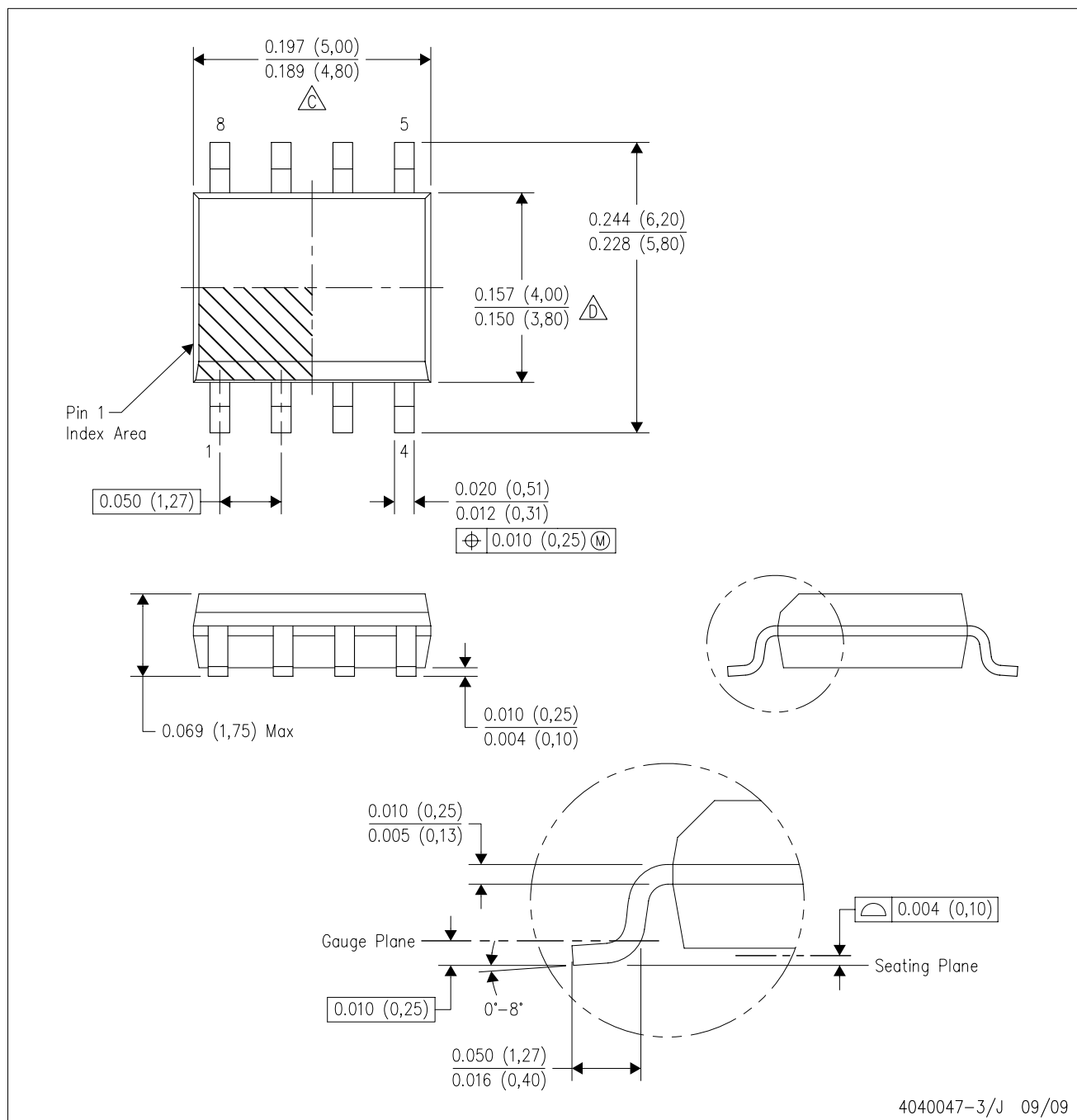
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

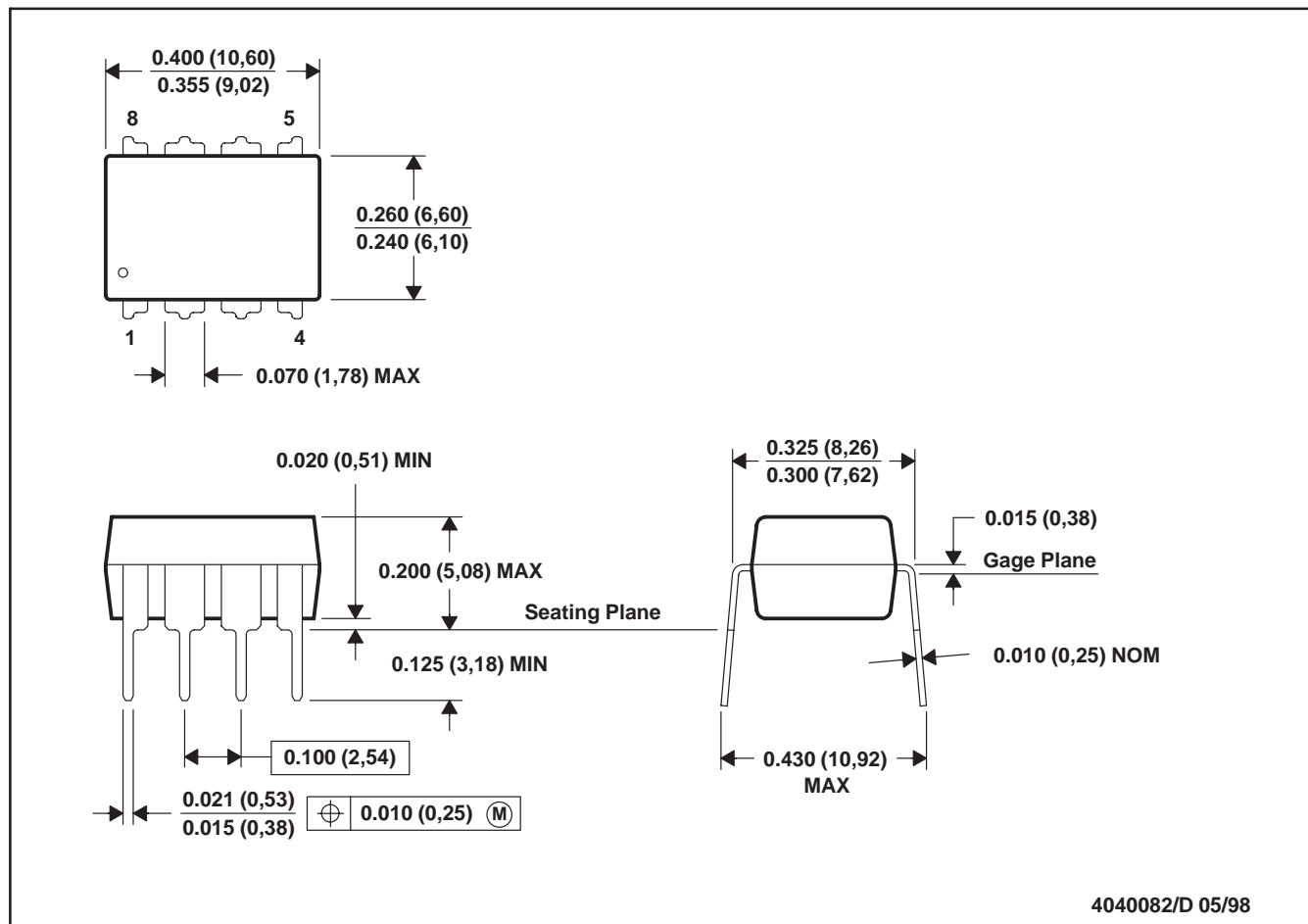


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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



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PACKAGING INFORMATION

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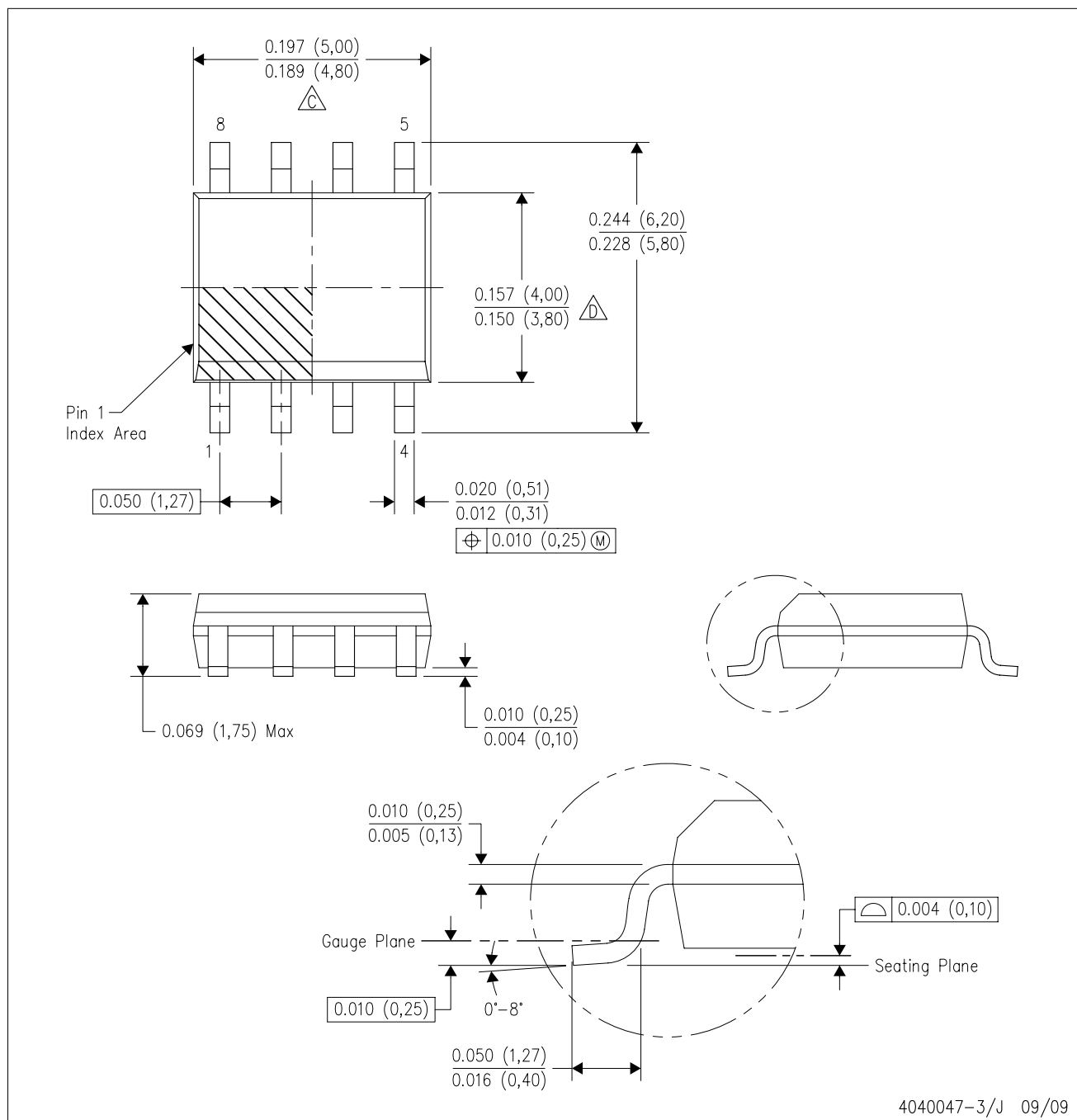
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PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/J 09/09

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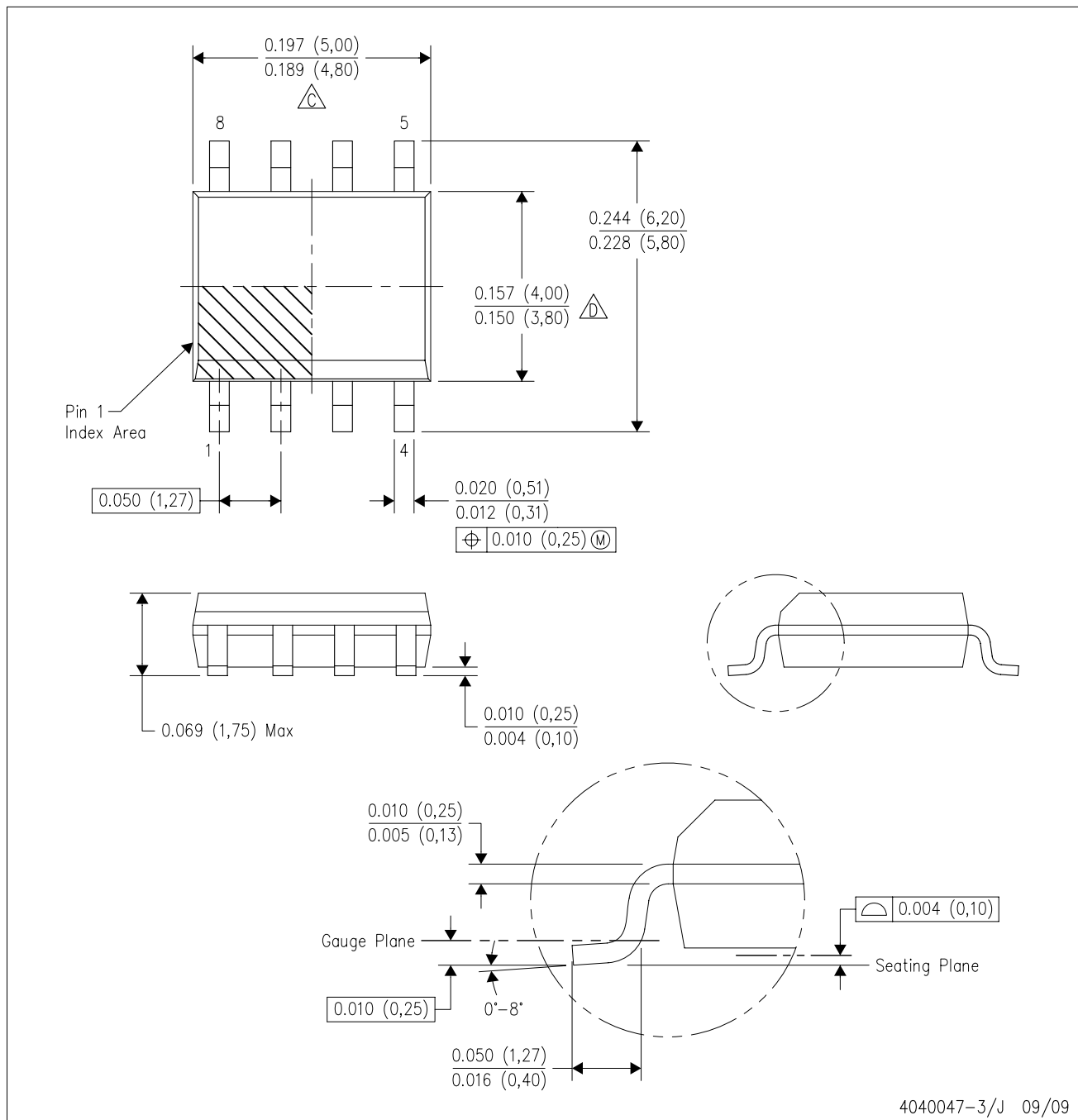
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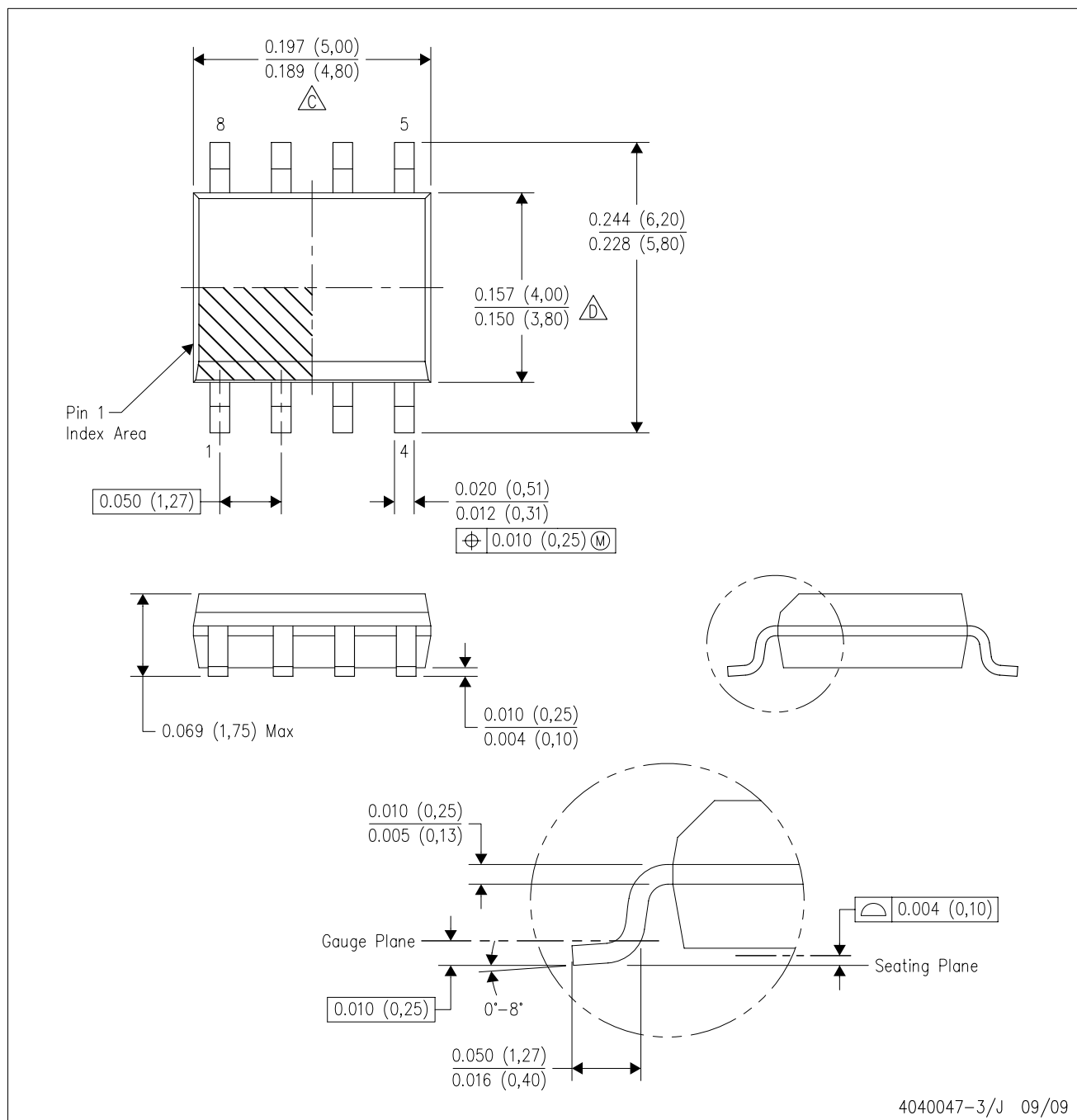
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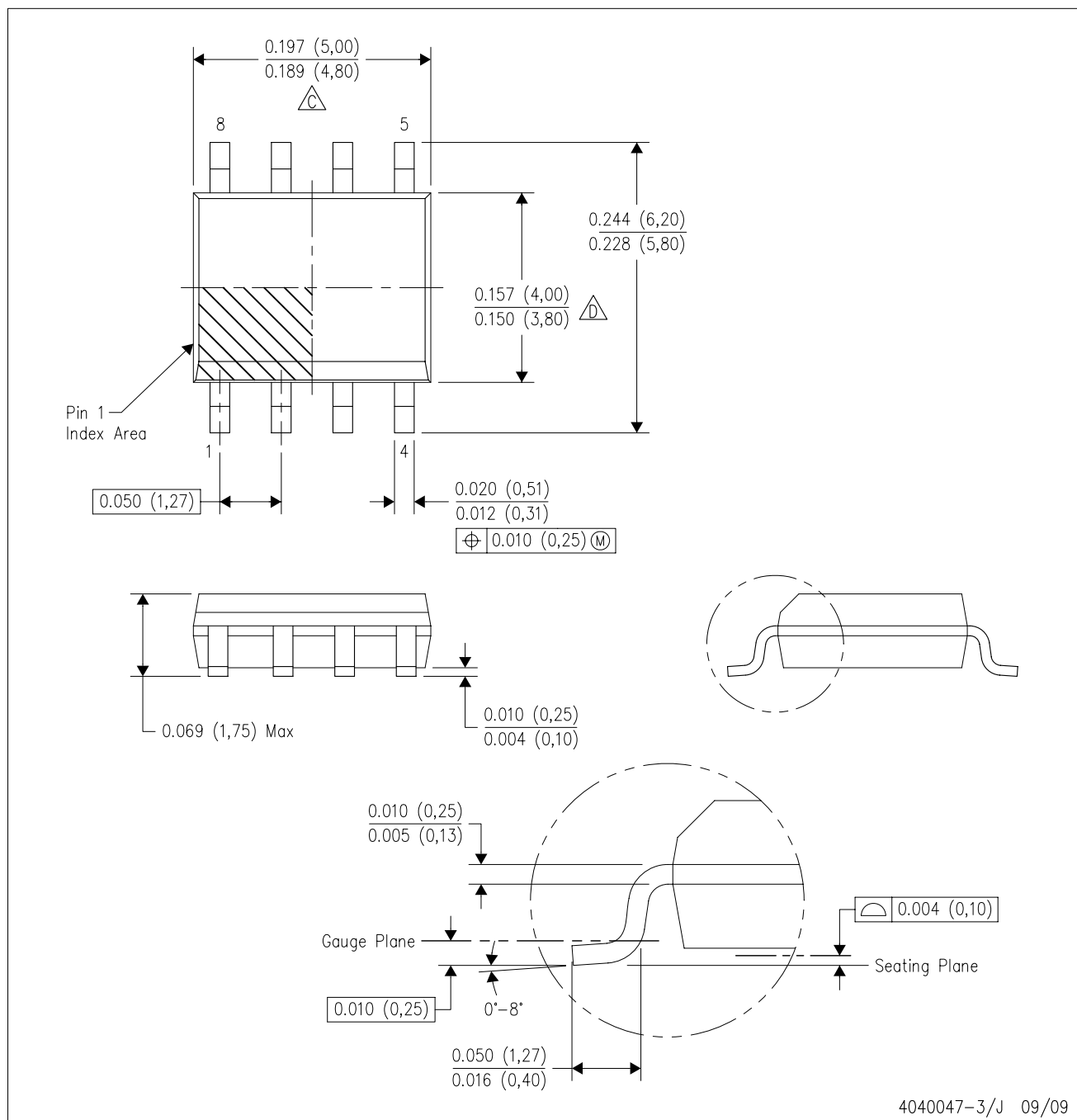
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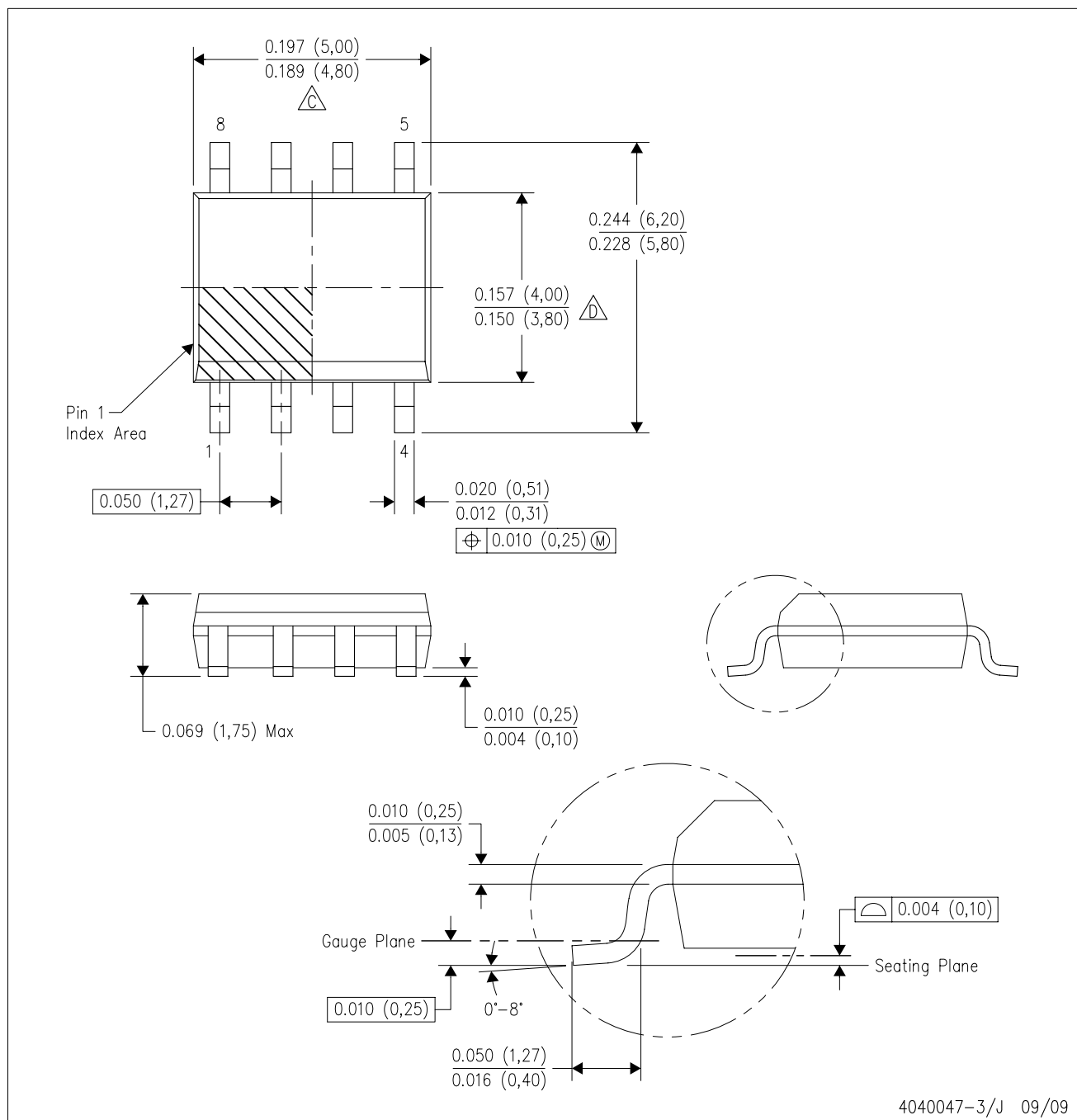
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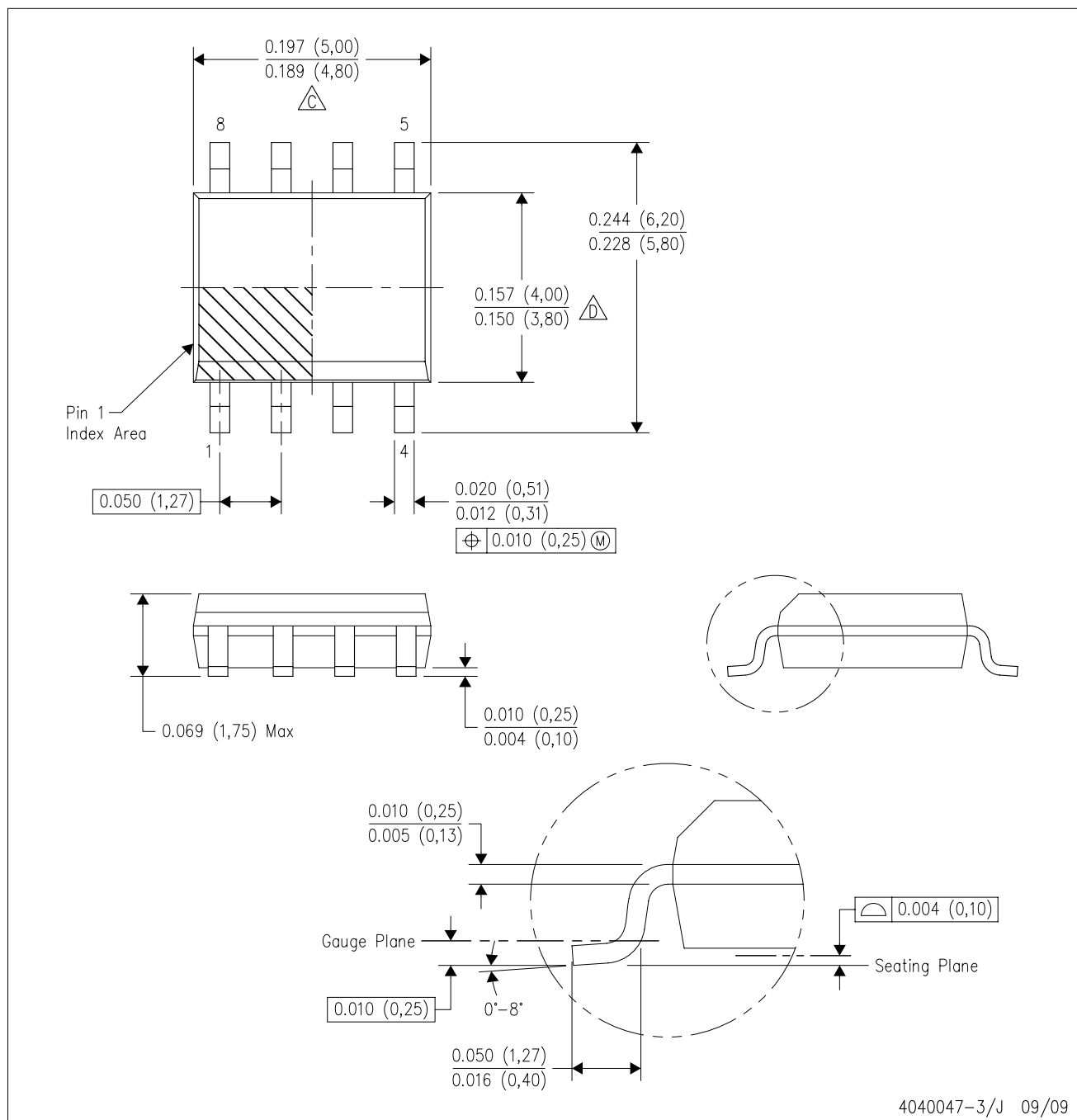
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⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

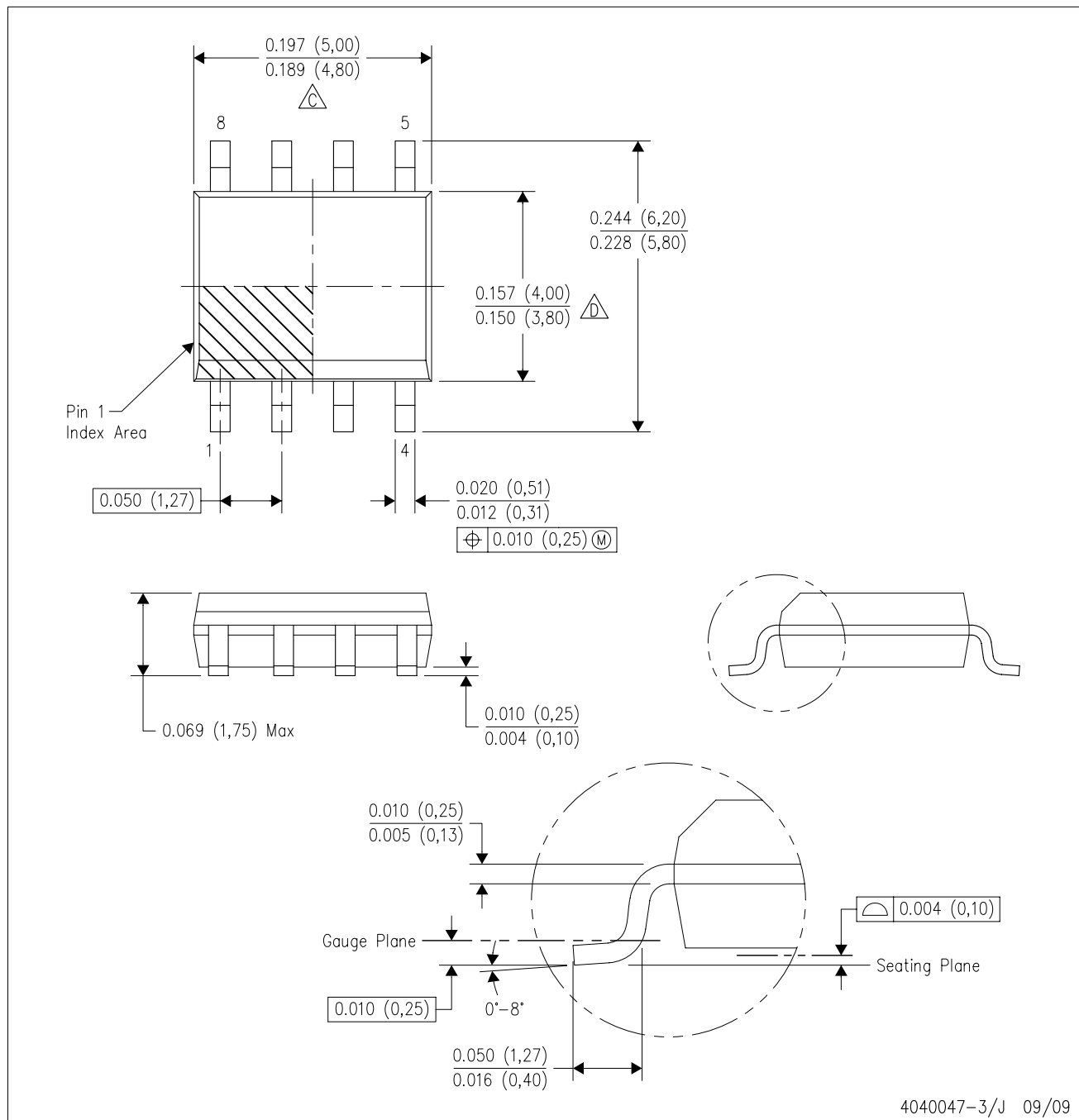
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/J 09/09

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL322CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL322ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL322ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL322IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL322IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

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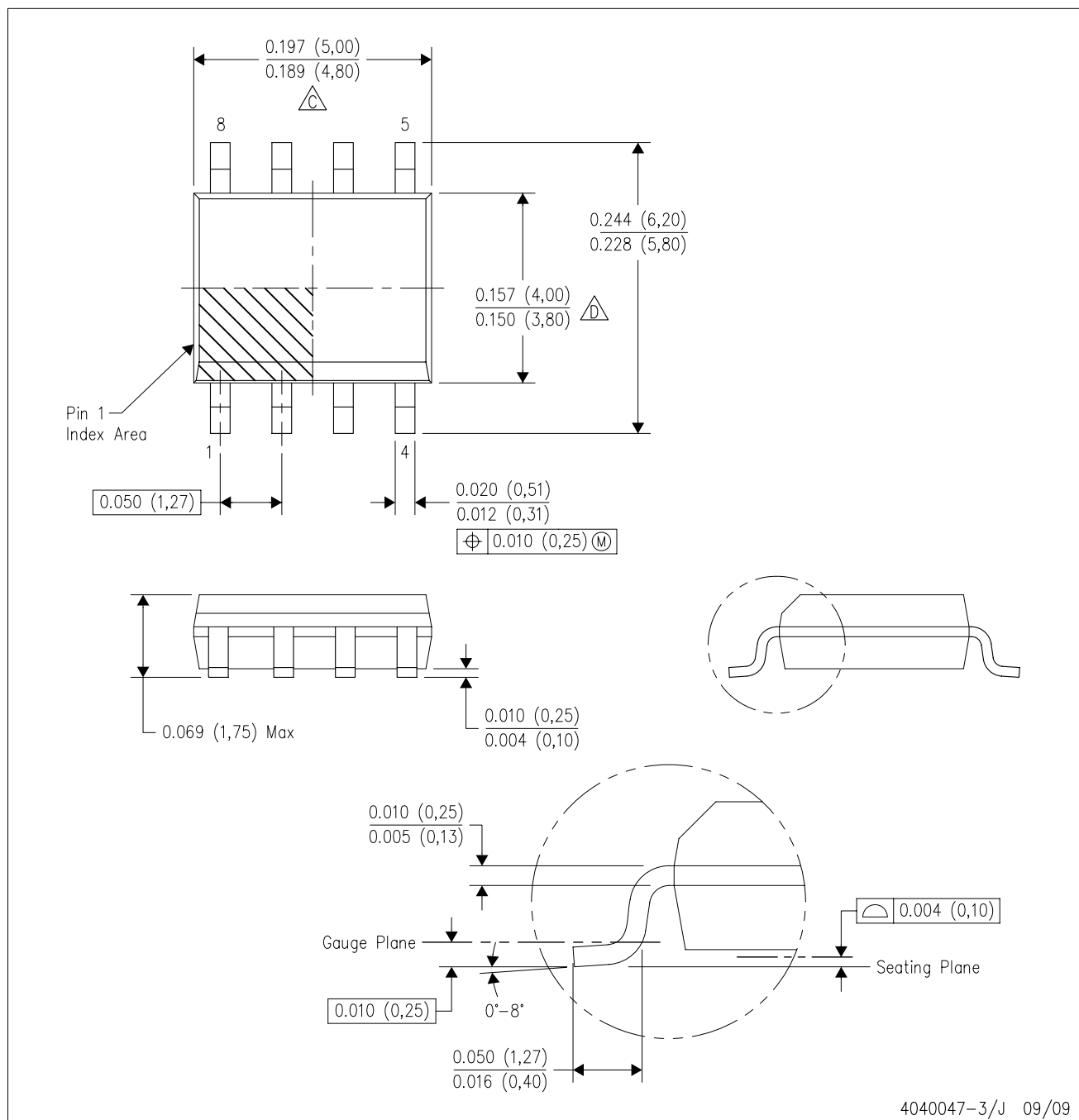
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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



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