# Si501/2/3

# 32 kHz–100 MHz CMEMS® Oscillator

## Features

- Wide frequency range: 32 kHz to 100 MHz
  - Contact Silicon Labs for frequencies above 100 MHz
- Si501 single frequency w/ OE
- Si502 dual frequency w/ OE/FS
- Si503 quad frequency w/ FS
- ±20/30/50 ppm frequency stability including 10-year aging
- LVCMOS output
- Low period jitter
- Low power
- Continuous supply voltage range: +1.71 V to +3.63 V
- User selectable tRise/tFall options
- Glitchless start and stop
- Excellent short-term stability, long-term aging
- Industry standard footprints: 2x2.5, 2.5x3.2, 3.2x5 mm
- RoHS compliant, Pb-free
- Short lead times: <2 weeks
- –20 to +70 °C: Extnd commercial
- –40 to +85 °C: Industrial
- The Si50x family also includes the Si504 for in-circuit programmability (See the Si504 Data Sheet)

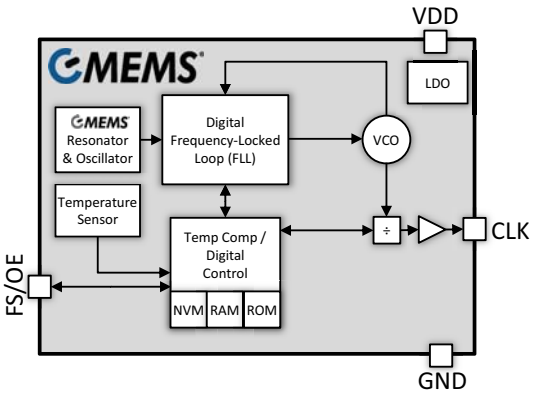
## Applications

- Storage (SATA/SAS/PCIe)
- General purpose processors
- Industrial controllers
- Embedded controllers
- Motor control
- Flow control
- Office/Home automation
- IP cameras/surveillance
- Display and control panels
- Outdoor electronics
- Multi-function printers
- Office equipment

## Description

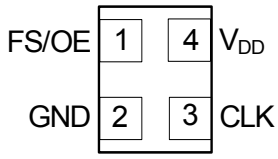
The Si501/2/3 CMEMS oscillator family provides monolithic, MEMS-based IC replacements for traditional crystal oscillators. Silicon Laboratories' CMEMS technology combines standard CMOS + MEMS in a single, monolithic IC to provide integrated, high-quality and high-reliability oscillators. Each device is factory tested and configured for guaranteed performance to data sheet specifications across voltage, process, temperature, shock, vibration, and aging.
Additional information on the Si50x CMEMS oscillator architecture and CMEMS technology is available in white papers on the Silicon Labs website at www.siliconlabs.com/cmems.

## Functional Block Diagram



**Ordering Information:**
See Section 5.

**Pin Assignments**




Patents pending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# 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

$V_{DD}$=1.71 to 3.63 V, $T_A$= –40 to 85 °C, unless otherwise specified

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage[1] | $V_{DD}$ | | 1.71 | — | 3.63 | V |
| Supply Current | $I_{DD1}$ | $C_L$=4 pF, 3.3 $V_{DD}$, $F_{CLK}$=1.0 MHz, low power option | — | 1.7 | 2.5 | mA |
| | | $C_L$=4 pF, 3.3 $V_{DD}$, $F_{CLK}$=100 MHz, low power option | — | 5.3 | 6.5 | mA |
| | | $C_L$=4 pF, 3.3 $V_{DD}$, $F_{CLK}$=1.0 MHz, low jitter option | — | 3.9 | 4.9 | mA |
| | | $C_L$=4 pF, 3.3 $V_{DD}$, $F_{CLK}$=100 MHz, low jitter option | — | 7.6 | 8.9 | mA |
| Static Supply Current | $I_{DD2}$ | Mode=Stop[2], low power option $F_{CLK}$=1 MHz | — | 1.7 | 2.5 | mA |
| | | Mode=Stop[2], low jitter option $F_{CLK}$=1 MHz | — | 3.9 | 4.9 | mA |
| | | Mode=Doze[2] | — | 670 | 890 | µA |
| | | Mode=Sleep[2] | — | 0.3 | 1 | µA |
| Input High Voltage | $V_{IH}$ | FS/OE pin | 0.70 x $V_{DD}$ | — | — | V |
| Input Low Voltage | $V_{IL}$ | FS/OE pin | — | — | 0.30 x $V_{DD}$ | V |
| OE Internal Pull Resistor | $R_I$ | Ordering option | 40 | 50 | 60 | kΩ |
| Operating Temperature | $T_A$ | Extended commercial grade | –20 | — | 70 | °C |
| | | Industrial grade | –40 | — | 85 | °C |

**Notes:**

1. The supply voltage range is continuous from 1.71 to 3.63 V.
2. Si501 and Si502 only. Si503 has FS only and does not support Stop, Doze, or Sleep. See Section 3. Functional Description for more information on operational modes.

### Table 2. Output Clock Characteristics

$V_{DD}$=1.71 to 3.63 V, $T_A$= –40 to 85 °C, unless otherwise specified.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Range | $F_{CLK}$ | | 0.032 | — | 100 | MHz |
| Clock Period | $T_{CLK}$ | $1/F_{CLK}$ | 31,250 | — | 10 | ns |
| Total Stability[1] | $F_{STAB}$ | | –20 | — | +20 | ppm |
| | | | –30 | — | +30 | ppm |
| | | | –50 | — | +50 | ppm |
| Initial Accuracy | $F_I$ | Measured at 25 °C at the time of shipping | — | ±2 | — | ppm |
| Startup Time[2] | $T_{SU}$ | From $V_{DD}$ crossing 1.71 V to first clock output | — | 2.5 | 4 | ms |
| Resume Time[3,4] | $T_{RUN}$ | From Sleep mode | — | 2.5 | 5 | ms |
| | | From Doze mode | — | 1.7 | 2.55 | ms |
| | | From Stop mode[5] | — | — | 1.5 x $T_{CLK}$ + 35 | ns |
| Output Disable Time[3,4] | $T_D$ | To Sleep/Doze mode, from output running | — | — | 225 | µs |
| | | To Stop, from output running | — | — | 1.5 x $T_{CLK}$ + 35 | ns |
| Frequency Update Time[4,6] | $T_{NEW_FREQ}$ | | — | — | 5 | ms |

**Notes:**

1. Orderable option. Stability budget consists of initial tolerance, operating temperature range, rated power supply voltage change, load change, 10-year aging, shock, and vibration.
2. Hold FS/OE high (strong or weak) during powerup for fastest time to clock.
3. Si501 and Si502 only. Si503 has FS only and does not support Stop, Doze, or Sleep.
4. Asserted FS/OE actions must be held stable for the maximum duration of the invoked FS/OE event (e.g., $T_{RUN}$, $T_{NEW_FREQ}$, $T_D$, etc).
5. If the Si502 frequency is switched while the device is in Stop mode, the frequency prior to Stop will be output briefly until the glitchless switch to the other frequency. Doze mode and Sleep mode do not have this behavior.
6. Si502 and Si503 only. Si501 is a single frequency device with OE only.

### Table 3. Output Clock Levels and Symmetry

$V_{DD}$ = 1.71 to 3.63 V, $T_A$ = –40 to 85 °C unless otherwise indicated.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | 1st ordering option code: A and H<br>$I_{OH}$=–4 mA | 0.90 x $V_{DD}$ | — | — | V |
| Output Low Voltage | $V_{OL}$ | 1st ordering option code: A and H<br>$I_{OH}$=+4 mA | — | — | 0.10 x $V_{DD}$ | V |
| Rise/Fall Time[1] | tRise /tFall | 1st ordering option code[2]: A and H<br>$Z_0$=25 Ω @ 3.3 V | 0.4 | 0.7[2] | 1.2 | ns |
| | | 1st ordering option code: B and J<br>$Z_0$= 50 Ω @ 3.3 V | 1 | 1.3 | 1.6 | ns |
| | | 1st ordering option code: C and K<br>$Z_0$= 50 Ω @ 2.5 V | 1 | 1.3 | 1.6 | ns |
| | | 1st ordering option code: D and L<br>$Z_0$ = 50 Ω @ 1.8 V | 1 | 1.3 | 1.6 | ns |
| | | 1st ordering option code: E and M<br>$Z_0$= 110 Ω @ 3.3 V | 2 | 3 | 4 | ns |
| | | 1st ordering option code: F and N<br>$Z_0$=220 Ω @ 3.3 V[3] | 4 | 5 | 7 | ns |
| | | 1st ordering option code: G and P<br>$Z_0$=440 Ω @ 3.3 V[3] | 7 | 8 | 11 | ns |
| Duty Cycle | DC | Drive strength selected such that tRise/tFall (20% to 80%)<10% of period | 45 | 50 | 55 | % |

**Notes:**
1. $C_L$=15 pF, tRise/tFall (20% to 80%), 3.3 V, unless otherwise stated.
2. Recommended series termination resistor ($R_S$) = 24.9 Ω for $Z_0$=50 Ω.
3. Ordering options F, N, G, and P are not recommended for $F_{CLK}$ > 5 $MH_2$.

### Table 4. Output Clock Jitter and Phase Noise

$V_{DD}$ = 1.71 to 3.63 V, $T_A$ = –40 to 85 °C unless otherwise indicated.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Cycle-to-Cycle Jitter | $J_{CCPP}$ | 100 MHz, Low Jitter Option<br>1st ordering option code: H | — | 14 | 25 | ps pk-pk |
| | | 100 MHz, Low Power Option<br>1st ordering option code: A | — | 16 | 26 | ps pk-pk |
| Period Jitter | $J_{PRMS}$ | 100 MHz, Low Jitter Option<br>1st ordering option code: H | — | 1 | 1.6 | ps rms |
| | | 100 MHz, Low Power Option<br>1st ordering option code: A | — | 1.3 | 1.9 | ps rms |
| Period Jitter Pk-Pk | $J_{PPKPK}$ | Low Jitter Option<br>10k samples<br>1st ordering option code: H | — | 9 | 13 | ps pk-pk |
| | | Low Power Option<br>10k samples<br>1st ordering option code: A | — | 10 | 16 | ps pk-pk |
| Phase Jitter[1] | $\phi$ | 75 MHz<br>$F_{OFFSET}$=900 kHz to 7.5 MHz<br>Low Jitter Option<br>1st ordering option code: H | — | 1 | 1.3 | ps rms |
| | | 75 MHz<br>$F_{OFFSET}$=900 kHz to 7.5 MHz<br>Low Power Option<br>1st ordering option code: A | — | 2.5 | 3.2 | ps rms |

**Notes:**

1. Integrated phase jitter exceeds the requirements of some high-performance data communications systems. See AN783 for additional information.

### Table 5. Environmental Compliance and Package Information

| Parameter | Test Condition |
|---|---|
| Mechanical Shock | MIL-STD-883, Method 2002, Cond B. (1,500 g) |
| Mechanical Shock High g | MIL-STD-883, Method 2002, Cond E. (10,000 g) |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Temperature Cycle | JESD22, Method A104 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Contact Pads | Gold over Nickel/Palladium |

### Table 6. Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Impedance | $\theta_{JA}$ | 3.2x5 mm, still air | 187 | °C/W |
| | | 2.5x3.2 mm, still air | 239 | |
| | | 2x2.5 mm, still air | 241 | |

### Table 7. Absolute Maximum Limits[1]

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum Operating Temperature | $T_{MAX}$ | 85 | °C |
| Storage Temperature | $T_S$ | –55 to +125 | °C |
| Supply Voltage | $V_{DD}$ | –0.5 to +3.8 | V |
| Input Voltage | $V_{IN}$ | –0.5 to $V_{DD}$ +0.3V | V |
| ESD Sensitivity (JESD22-A114) | HBM | 2000 | V |
| ESD Sensitivity (CDM) | CDM | 500 | V |
| Soldering Temperature (Pb-free profile)[2] | $T_{PEAK}$ | 260 | °C |
| Soldering Time at $T_{PEAK}$ (PB-free profile)[2] | $T_P$ | 20–40 | s |
| Junction Temperature | $T_J$ | 125 | °C |

**Notes:**
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

# 2. Si501/2/3 Typical Applications Circuits, AC Waveforms, and Functional Descriptions

The Si501/2/3 family has various applications circuits and ac waveforms depending on the selected device and ordering configuration options. Pay careful attention when reading the following section to be sure you refer to the correct diagrams.

## 2.1. Si501/2 Applications Circuits

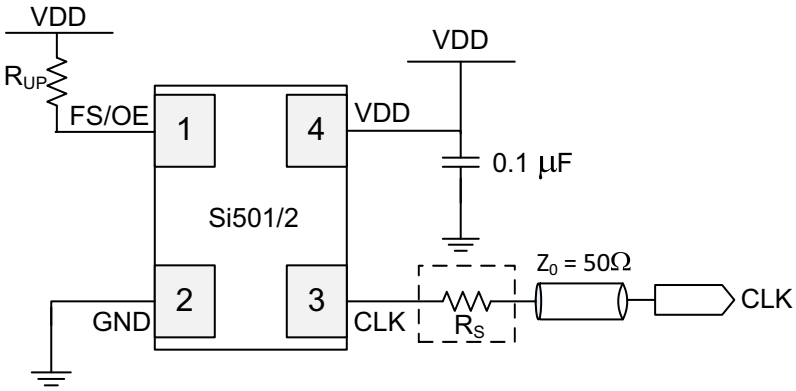
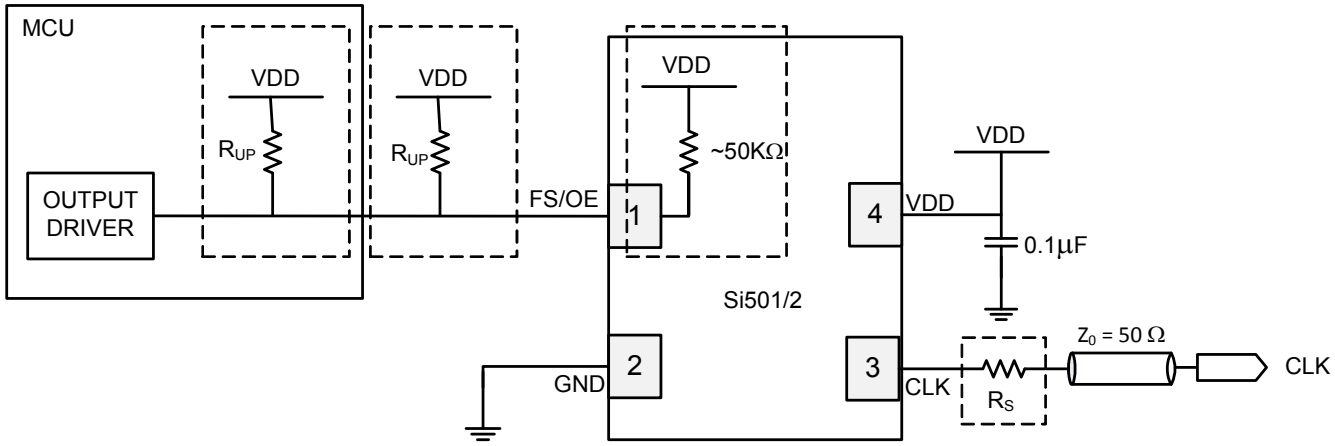



**Figure 1. Si501/2 Applications Circuit with Optional Output Series Resistor**

**Note:** The dotted line box in Figure 1 is an optional component depending on tRise/tFall configuration option. This diagram applies to all Si50x product drive strength configuration options. See Table 3 for $R_S$ recommendations. See Section 5. "Ordering Guide" for configuration options.




**Note:** The dotted line boxes in Figure 2 show resistor options depending on MCU pull-up resistors configuration and the Si501/2 internal resistor configuration options. See Section 5. "Ordering Guide" for configuration options. Users should design only one of the pin 1 dotted-line options. The series resistor ($R_S$) on pin 3 is also optional. See Table 3 for $R_S$ recommendations.

**Figure 2. Si501/2 Applications Circuit with MCU Configuration Options**

**Table 8. Si502 FS/OE States and Resistor Values**

| FS/OE Pin State | $R_{UP}$ | Clock Output |
|---|---|---|
| Strong High | $0\ \Omega \le R_{UP} \le 1\ k\Omega$ | Frequency 1 |
| Weak High | $20\ k\Omega \le R_{UP} \le 200\ k\Omega$ | Frequency 2 |
| Low | — | Hi-Z |

**Notes:**
1. If the Si502 internal pull-up resistor configuration option is not selected, an MCU internal pull-up resistor or an external pull-up resistor should be used.
2. The parallel combination of all pull-up resistors on the FS/OE pin, including the optional internal device pull-up resistor must be > 20 kΩ to select the Weak High state.
3. If the Si502 internal pull-up resistor is enabled with no other external FS/OE connections, the FS/OE state will be detected as `Weak High' which selects the Frequency 2 output by default.

## 2.2. Si501/2 AC Waveforms and Functional Descriptions

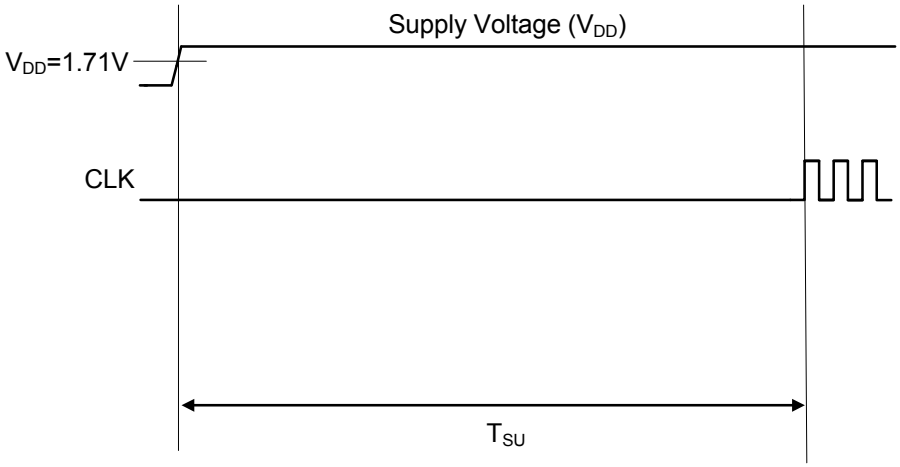



**Figure 3. Si501/2 Power On Time (refer to Table 2)**

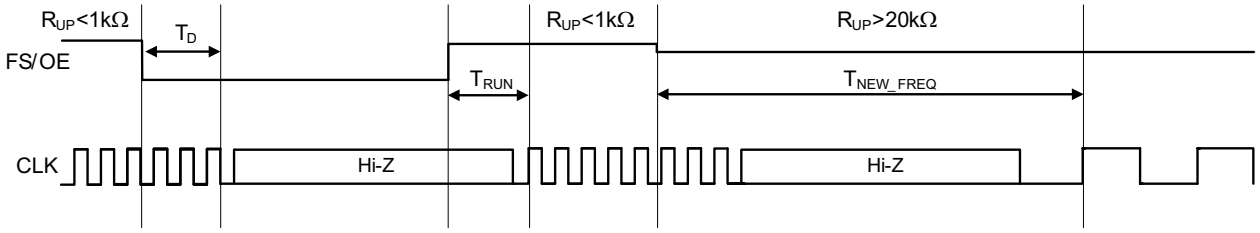
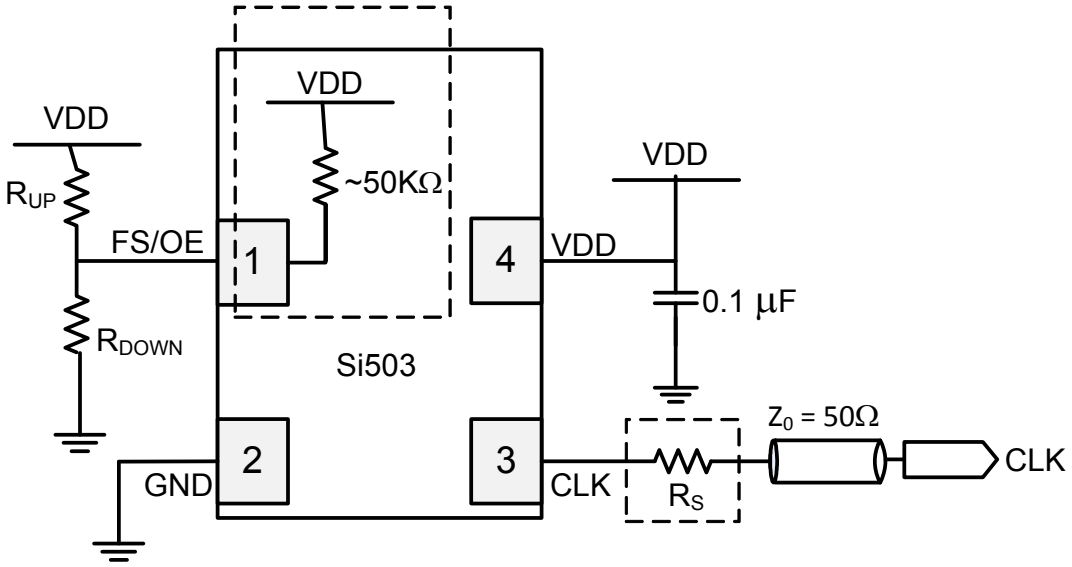



**Figure 4. Si501/2 AC Waveform (refer to Table 2)**

## 2.3. Si503 Applications Circuits

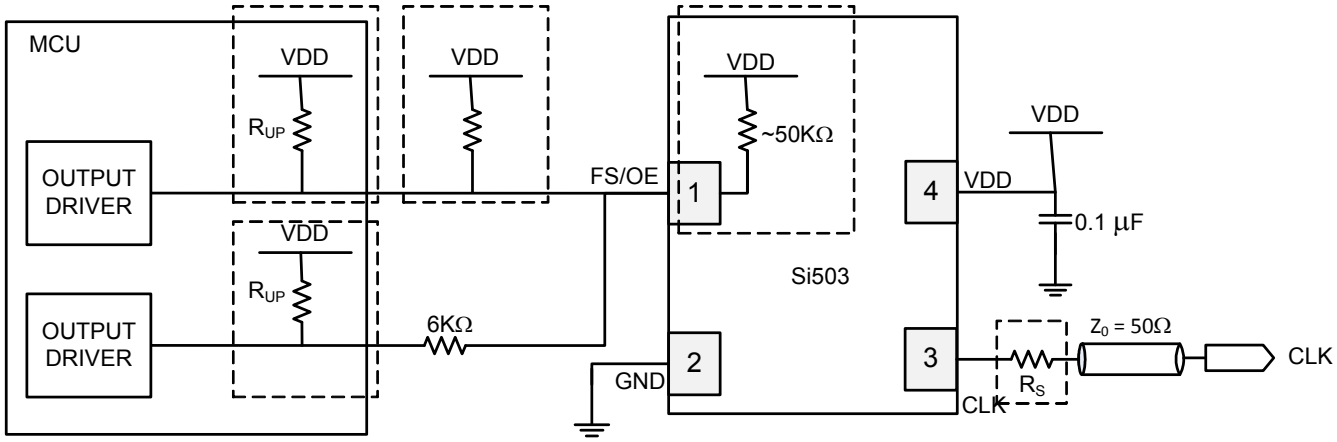



**Note:** The dotted line boxes show optional components depending on tRise/tFall and internal pull up resistor configuration options. See Section 5. "Ordering Guide" for configuration options. See Table 3 for $R_S$ recommendations.

**Figure 5. Si503 Applications Circuit with Configuration Options**

**Table 9. Si503 Frequency Select with External Resistor Options**

| FS/OE Pin State | $R_{UP}$ | $R_{DOWN}$ | Clock Output |
|---|---|---|---|
| Strong High | $0\ \Omega \le R_{UP} \le 1\ k\Omega$ | Do not populate | Frequency 1 |
| Weak High | $20\ k\Omega \le R_{UP} \le 200\ k\Omega$ | Do not populate | Frequency 2 |
| Weak Low | Do not populate | $20\ k\Omega \le R_{DOWN} \le 200\ k\Omega$ | Frequency 3 |
| Strong Low | Do not populate | $0\ \Omega \le R_{DOWN} \le 1\ k\Omega$ | Frequency 4 |
| **Note:** If the Si503 internal pull-up resistor is enabled with no other external FS/OE connections, the FS/OE state will be detected as `Weak High' which selects the Frequency 2 output by default. | | | |




**Note:** The dotted line boxes in Figure 6 show resistor options depending on MCU pull-up resistors configuration and the Si503 internal resistor configuration options. See Section 5. "Ordering Guide" for configuration options. Users should design only one of the pin 1 dotted-line options. The series resistor ($R_S$) on pin 3 is also optional. See Table 3 for $R_S$ recommendations.

**Figure 6. Si503 Applications Circuit with MCU and Configuration Options**

**Table 10. Si503 Frequency Select**

| FS/OE Pin State | MCU Output 1 | MCU Output 2 | Clock Output |
|---|---|---|---|
| Strong High | High | Hi-Z | Frequency 1 |
| Weak High | Hi-Z | Hi-Z | Frequency 2 |
| Weak Low | Hi-Z | Low | Frequency 3 |
| Strong Low | Low | Hi-Z | Frequency 4 |
| **Note:** If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as `Weak High' which selects the Frequency 2 output by default. | | | |

## 2.4. Si503 AC Waveform and Functional Description

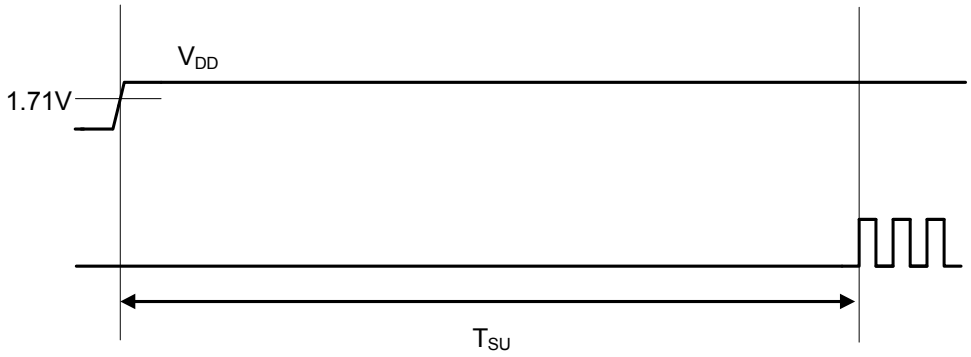



**Figure 7. Si503 Power On Time (refer to Table 2)**

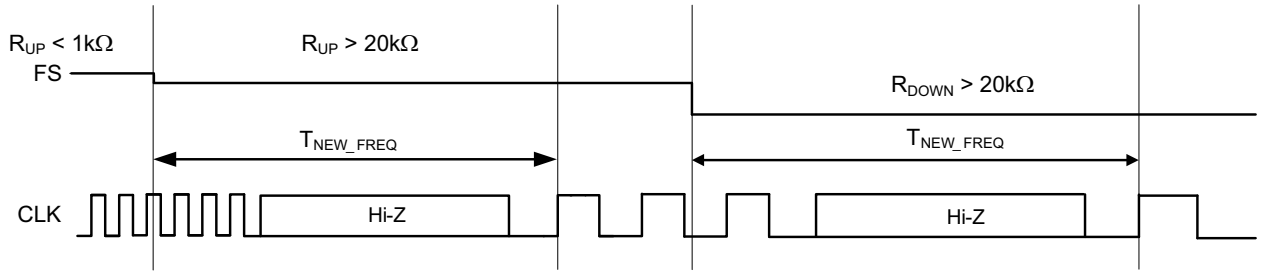



**Figure 8. Si503 AC Waveform (refer to Table 2)**

# 3. Functional Description

The Si50x series oscillator family includes four base devices. All devices are configurable according to the Section 5. "Ordering Guide". The four devices each support a single clock output frequency at any one time and are segmented according to the number of clock frequencies they store in on-chip memory.

The Si501 supports a single stored frequency, enabled with the OE functionality. The Si502 stores two frequencies that can be selected with FS and enabled/disabled with OE functionality. The Si503 stores four frequencies, selected with FS functionality. The Si503 does not support OE functionality. The Si501/2/3 are covered in this data sheet.

The Si504 is a programmable oscillator, controlled through a single pin interface (C1D). It is covered in its own Si504 data sheet available at www.siliconlabs.com/cmems.

All devices in the Si50x CMEMS series employ a cost-optimized, power-efficient, digital FLL architecture to produce a highly accurate and stable output clock from a passively compensated MEMS resonator reference frequency.

The architecture uses the MEMS resonator as its reference frequency along with a divided signal from an on-chip, digitally-controlled VCO to drive a frequency comparator for the FLL's digital loop filter. The digital loop filter accumulates and further processes the frequency error values to produce the target output frequency.

The architecture also uses a high-resolution, low-noise temperature sensor and temperature compensation algorithm to offset any temperature drift of the passively compensated MEMS resonator. Each device is calibrated for temperature and MEMS-resonator frequency pairs and derives a device-specific compensation polynomial. As the temperature changes, this compensation circuitry offsets any frequency drift.

This tightly coupled system is extremely accurate and fast because the MEMS resonator and CMOS compensation circuitry are in a single, monolithic chip, and, therefore, separated by a few microns.

The complete system process occurs many thousands of times per second, providing excellent frequency accuracy and stability across temperature changes, including any fast temperature transients. The oscillator also supports a low-power version that reduces the sampling cycle to a longer period, reducing power consumption for applications that can tolerate relaxed jitter specifications of approximately 1 ps RMS to reduce power by approximately 2-3 mA. See Table 1 for exact specifications.

## 3.1. OE Enable and Disable States

The Si50x CMEMS series supports four operational output states via the FS/OE configuration pin. If enabled, the Si50x is in Run mode, the clock is output and power is as specified in Table 1. The disable modes are Stop, Sleep, and Doze. Each of these states has a different power consumption profile as specified in Table 1.

### 3.1.1. Stop Mode

The Si50x output in Stop mode is high-impedance, also known as High-Z (Hi-Z) or Tri-State. Stop mode disables the output driver, but the digital core and MEMS resonator remain enabled for fast transition to Run mode. The output is stopped and held at High-Z after completing the last cycle glitch-free. No other power saving measure is taken in Stop mode.

### 3.1.2. Doze Mode

The Si50x output in Doze mode is high-impedance, also known as High-Z (Hi-Z) or Tri-State. Doze mode disables the output driver, the VCO, and the MEMS resonator, but the digital core remains enabled. The output is stopped and is held at High-Z after completing the last cycle glitch-free.

### 3.1.3. Sleep Mode

The Si50x output in Sleep mode is high-impedance, also known as High-Z (Hi-Z) or Tri-State. Sleep mode disables power to all circuitry except for low-leakage circuitry that retains the last device configuration. The output is stopped and is held at High-Z after completing the last cycle glitch-free.

## 3.2. Output Rise and Fall Settings

The Si50x clock output is programmable. This enables reduction of electromagnetic interference (EMI) radiation from the clock output. The amount of EMI reduction is dependent on the output frequency, the harmonic of interest, and the board layout. Lab results using a 50 MHz FOUT and changing the clock tRise/tFall time from 0.7 ns to 8 ns show up to 14 dB of EMI reduction.

The tRise/tFall feature also allows the Si50x to match competing devices' rise and fall times. Crystal oscillator tRise/tFall behavior is largely dependent on the supply voltage. In crystal-based oscillators, a higher supply voltage will generally drive a more rapid tRise/tFall time. The Si50x configuration options allow the user to match the tRise/tFall to the supply voltage. The Si50x also provides a specified tRise/tFall with a given supply voltage and a 50 Ω trace impedance. See Table 3 for Si50x tRise/tFall specifications.

# 4. Pin Descriptions

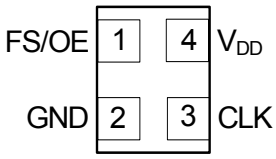



**Figure 9. Si501/2/3**

**Table 11. Pin Description**

| Pin | Name | Function |
|---|---|---|
| 1 | FS/OE | FS=Frequency Select. Si502 and Si503 only.<br>OE=Output Enable. Si501 and Si502 only. |
| 2 | GND | Ground. |
| 3 | CLK | Output clock. |
| 4 | $V_{DD}$ | Power supply.<br>Bypass with a 0.1μF capacitor placed as close to the $V_{DD}$ pin as possible. |

## 5. Ordering Guide

The Si50x family of CMEMS oscillators are highly configurable. Each orderable part number must be specified according to the guidelines below. Each customized part's performance is guaranteed to operate within the data sheet specifications. An on-line configuration and ordering tool is available at www.siliconlabs.com/cmems.

### 5.1. Si501 Ordering Guide and Part Number Syntax

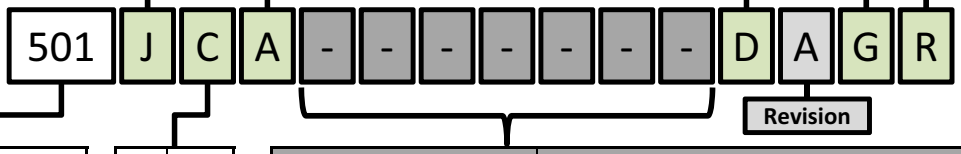
| | VDD | Jitter vs Power | TYP $T_R/T_F$ |
|---|---|---|---|
| A | 1.7-3.6 | Low Power | 0.7 ns[1] |
| B | 3.3V | | 1.3 ns[2] |
| C | 2.5V | | 1.3 ns[2] |
| D | 1.8V | | 1.3 ns[2] |
| E | 1.7-3.6 | | 3 ns[3] |
| F | 1.7-3.6 | | 5 ns[3] |
| G | 1.7-3.6 | | 8 ns[3] |
| H | 1.7-3.6 | Low Jitter | 0.7 ns[1] |
| J | 3.3V | | 1.3 ns[2] |
| K | 2.5V | | 1.3 ns[2] |
| L | 1.8V | | 1.3 ns[2] |
| M | 1.7-3.6 | | 3 ns[3] |
| N | 1.7-3.6 | | 5 ns[3] |
| P | 1.7-3.6 | | 8 ns[3] |

| | OE High | OE Low | Internal Pull Resistor |
|---|---|---|---|
| A | Enable | Stop | Pull-Up |
| B | Enable | Doze | Pull-Up |
| C | Enable | Sleep | Pull-Up |
| D | Stop | Enable | Pull-Down |
| E | Doze | Enable | Pull-Down |
| F | Sleep | Enable | Pull-Down |
| G | Enable | Stop | None |
| H | Enable | Doze | None |
| J | Enable | Sleep | None |
| K | Stop | Enable | None |
| L | Doze | Enable | None |
| M | Sleep | Enable | None |

| | Package Dimension |
|---|---|
| B | 3.2 x 5 mm[4] |
| C | 2.5 x 3.2 mm |
| D | 2 x 2.5 mm |

| | Temp Range |
|---|---|
| F | -20 to 70 °C |
| G | -40 to 85 °C |

| | Reel |
|---|---|
| R | Reel |
| | Cut Tape |




| OPN Prefix | Description |
|---|---|
| 501 | Single frequency |
| 502 | Dual frequency |
| 503 | Quad frequency |
| 504 | Any frequency |

| | Ppm |
|---|---|
| A | ± 50 |
| B | ± 30 |
| C | ± 20 |

| Frequency Code | Description |
|---|---|
| Mxxxxxx | $f_{OUT}$ < 1 MHz |
| xMxxxxx | 1 MHz ≤ $f_{OUT}$ < 10 MHz |
| xxMxxxx | 10 MHz ≤ $f_{OUT}$ < 100 MHz |
| 100M000 | $f_{OUT}$ = 100 MHz |
| xxxxxx | 6-digit code for > 6 decimal resolution |

**Note:**

1. Series termination resistor ($R_S$) is recommended for this configuration. See Table 3 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

**Figure 10. Si501 Part Number Syntax**

## 5.2. Si502 Ordering Guide and Part Number Syntax

| | VDD | Jitter vs Power | TYP $T_R/T_F$ |
|---|---|---|---|
| A | 1.7-3.6 | Low Power | 0.7 ns[1] |
| B | 3.3V | | 1.3 ns[2] |
| C | 2.5V | | 1.3 ns[2] |
| D | 1.8V | | 1.3 ns[2] |
| E | 1.7-3.6 | | 3 ns[3] |
| F | 1.7-3.6 | | 5 ns[3] |
| G | 1.7-3.6 | | 8 ns[3] |
| H | 1.7-3.6 | Low Jitter | 0.7 ns[1] |
| J | 3.3V | | 1.3 ns[2] |
| K | 2.5V | | 1.3 ns[2] |
| L | 1.8V | | 1.3 ns[2] |
| M | 1.7-3.6 | | 3 ns[3] |
| N | 1.7-3.6 | | 5 ns[3] |
| P | 1.7-3.6 | | 8 ns[3] |

| | OE Low[5] | Internal Pull Resistor |
|---|---|---|
| A | Stop | Pull-Up |
| B | Doze | Pull-Up |
| C | Sleep | Pull-Up |
| D | Stop | None |
| E | Doze | None |
| F | Sleep | None |

| | Package Dimension |
|---|---|
| B | 3.2 x 5 mm[4] |
| C | 2.5 x 3.2 mm |
| D | 2 x 2.5 mm |

| | Temp Range |
|---|---|
| F | -20 to 70 °C |
| G | -40 to 85 °C |

| | Reel |
|---|---|
| R | Reel |
| | Cut Tape |

| 502 | J | C | A | - | - | - | - | - | - | - | D | A | G | R |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Revision

| OPN Prefix | Description |
|---|---|
| 501 | Single frequency |
| 502 | Dual frequency |
| 503 | Quad frequency |
| 504 | Any frequency |

| | Ppm |
|---|---|
| A | ± 50 |
| B | ± 30 |
| C | ± 20 |

| Frequency Code | Description |
|---|---|
| xxxxxx | 6-digit code from Silicon Labs |

**Note:**

1. Series termination resistor ($R_S$) is recommended for this configuration. See Table 3 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.
5. The Si502 OE pin has three (3) states: OE High = Freq 1; OE Weak High = Freq 2; OE Low is configurable.

**Figure 11. Si502 Part Number Syntax**

## 5.3. Si503 Ordering Guide and Part Number Syntax

| | VDD | Jitter vs Power | TYP $T_R/T_F$ |
|---|---|---|---|
| A | 1.7-3.6 | Low Power | 0.7 ns[1] |
| B | 3.3V | | 1.3 ns[2] |
| C | 2.5V | | 1.3 ns[2] |
| D | 1.8V | | 1.3 ns[2] |
| E | 1.7-3.6 | | 3 ns[3] |
| F | 1.7-3.6 | | 5 ns[3] |
| G | 1.7-3.6 | | 8 ns[3] |
| H | 1.7-3.6 | Low Jitter | 0.7 ns[1] |
| J | 3.3V | | 1.3 ns[2] |
| K | 2.5V | | 1.3 ns[2] |
| L | 1.8V | | 1.3 ns[2] |
| M | 1.7-3.6 | | 3 ns[3] |
| N | 1.7-3.6 | | 5 ns[3] |
| P | 1.7-3.6 | | 8 ns[3] |

| | Internal Pull Resistor |
|---|---|
| A | Pull-Up |
| B | None |

| | Package Dimension |
|---|---|
| B | 3.2 x 5 mm[4] |
| C | 2.5 x 3.2 mm |
| D | 2 x 2.5 mm |

| | Temp Range |
|---|---|
| F | -20 to 70 °C |
| G | -40 to 85 °C |

| | Reel |
|---|---|
| R | Reel |
| | Cut Tape |

503 J C A - - - - - - - D A G R

Revision

| OPN Prefix | Description |
|---|---|
| 501 | Single frequency |
| 502 | Dual frequency |
| 503 | Quad frequency |
| 504 | Any frequency |

| | Ppm |
|---|---|
| A | ± 50 |
| B | ± 30 |
| C | ± 20 |

| Frequency Code | Description |
|---|---|
| xxxxxx | 6-digit code from Silicon Labs |

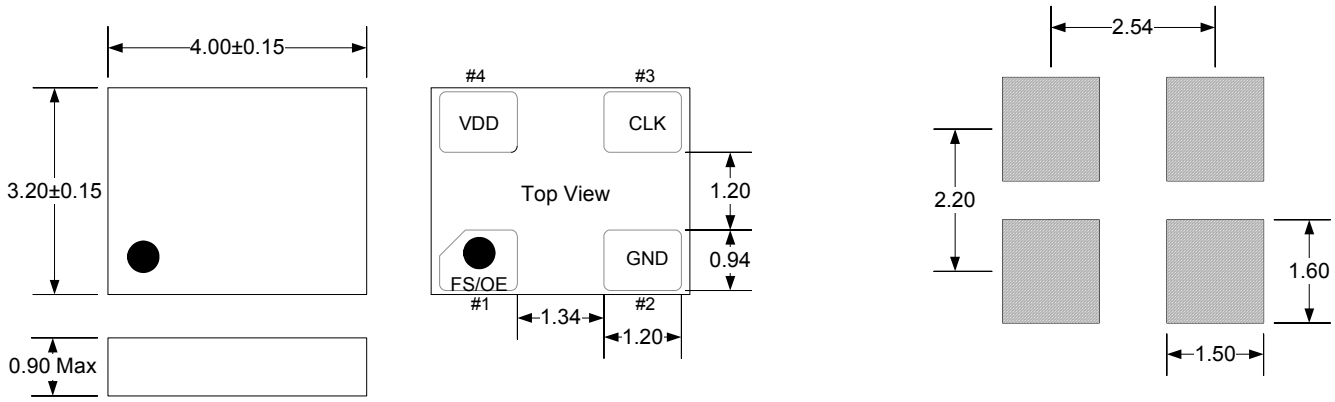
**Note:**

1. Series termination resistor ($R_S$) is recommended for this configuration. See Table 3 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

**Figure 12. Si503 Part Number Syntax**

# 6. Package Dimensions and Land Patterns

## 6.1. Package Outline: 3.2 x 5 mm 4-pin DFN




**Note: Layout and pin-compatible with industry-standard 3.2 x 5 mm footprint.**

**Figure 13. 3.2 x 5 mm 4-pin DFN**

## 6.2. Package Outline: 2.5 x 3.2 mm 4-pin DFN

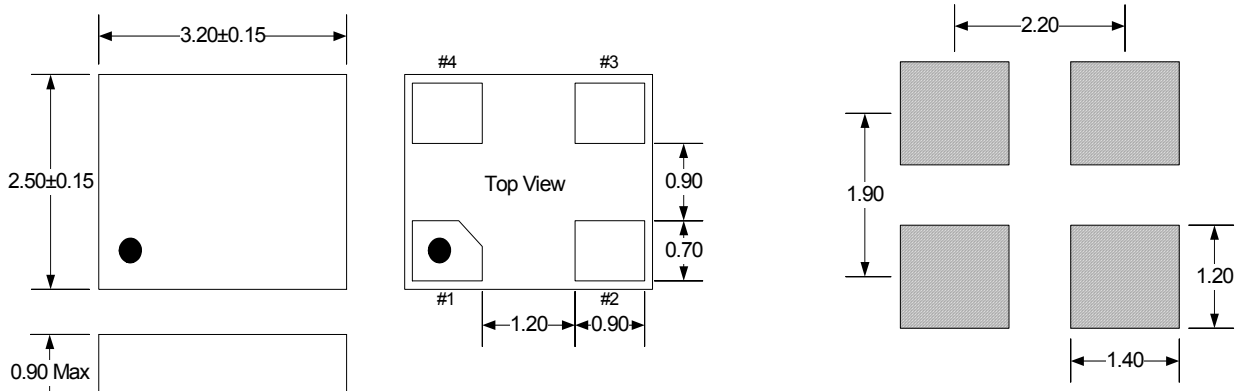



**Figure 14. 2.5 x 3.2 mm 4-pin DFN**

## 6.3. Package Outline: 2 x 2.5 mm 4-pin DFN

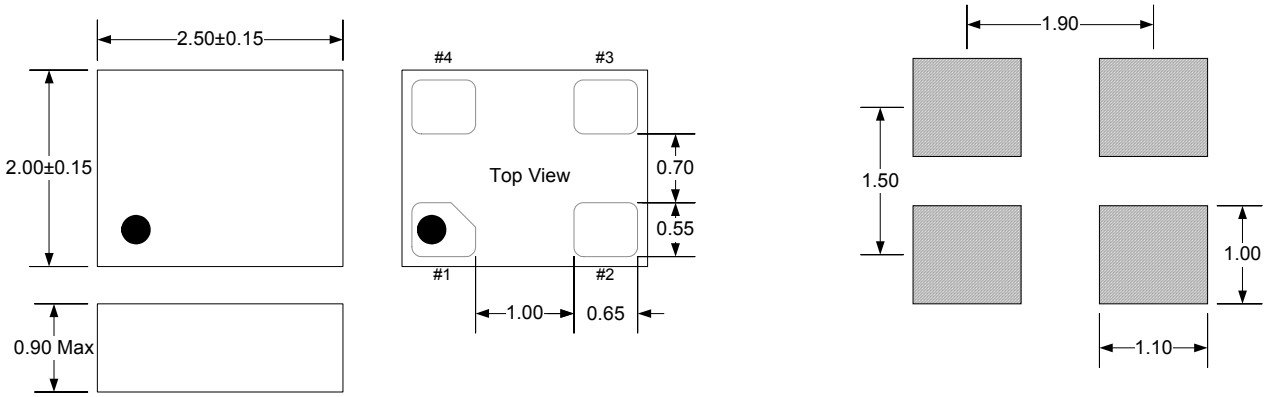
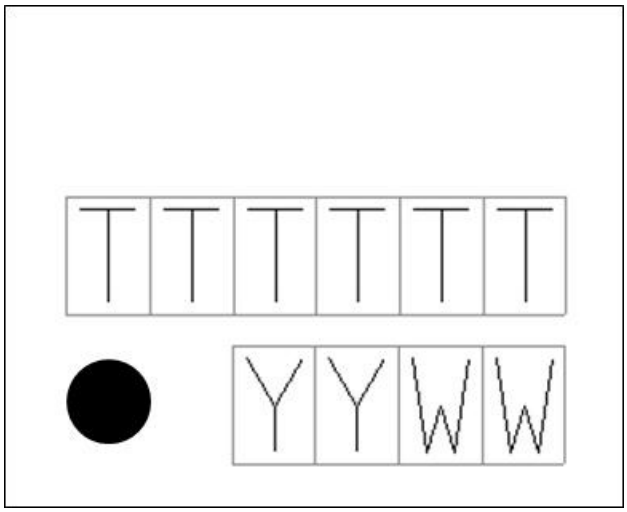



**Figure 15. 2 x 2.5 mm 4-pin DFN**

# 7. Top Markings

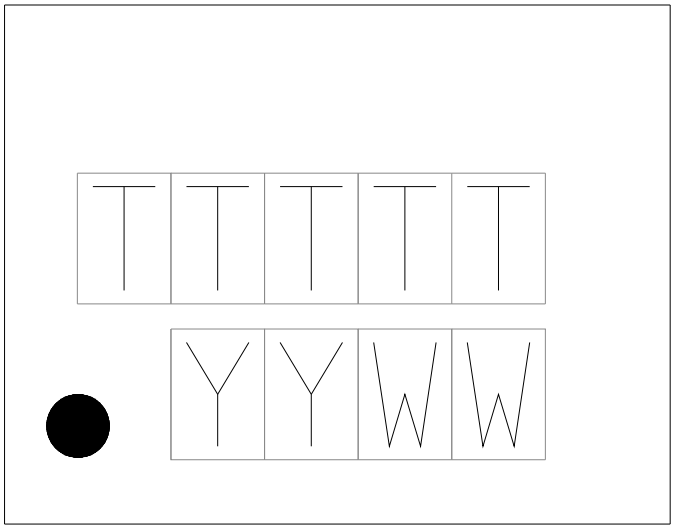
## 7.1. 3.2 x 5 mm Top Marking




## 7.2. 3.2 x 5 mm Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font Size:** | 0.60 mm<br>Right-Justified | |
| **Line 1 Marking:** | TTTTTT=Trace Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 2 Marking** | Circle=0.5 mm<br>Diameter<br>Left-Justified | Pin 1 Indicator |
| | YY=Year<br>WW=Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

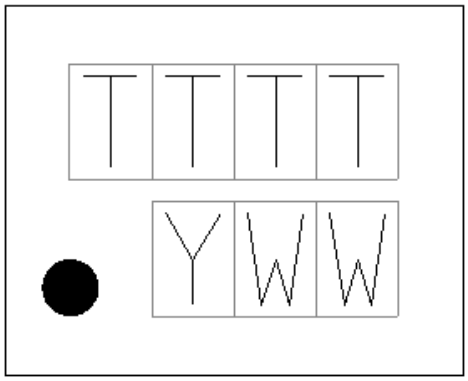
## 7.3. 2.5 x 3.2 mm Top Marking




## 7.4. 2.5 x 3.2 mm Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font Size:** | 0.50 mm<br>Right-Justified | |
| **Line 1 Marking:** | TTTTT=Trace Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 2 Marking:** | Circle=0.3 mm Diameter<br>Left-Justified | Pin 1 Indicator |
| | Y=Year<br>WW=Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

## 7.5. 2 x 2.5 mm Top Marking




## 7.6. 2 x 2.5 mm Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font Size:** | 0.50 mm<br>Right-Justified | |
| **Line 1 Marking:** | TTTT=Trace Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 2 Marking:** | Circle=0.3 mm Diameter<br>Left-Justified | Pin 1 Indicator |
| | Y=Year<br>WW=Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

# Document Change List

## Revision 0.2 to Revision 0.3

- Combined Si501/2/3 data sheets.
- Modified title page.
- Modified Table 2.
- Modified Table 4.
- Modified Section 2.
- Modified Section 3.
- Modified Section 4.
- Modified Section 5.

## Revision 0.3 to Revision 0.4

- Modified title page.
- Modified Table 1.
- Modified Table 2.
- Modified Table 3.
- Modified Table 4.
- Modified Table 5.
- Modified Table 6.
- Modified Table 7.
- Modified Section 2.
- Modified Section 4.
- Modified Section 5.
- Modified Section 6.

## Revision 0.4 to Revision 0.41

- Modified Table 4.

## Revision 0.41 to Revision 0.7

- Revised supported frequency range.
- Added MIN/MAX figures to all relevant tables.

## Revision 0.7 to Revision 0.71

- Revised Table 3.
- Revised Section 5.

## Revision 0.71 to Revision 0.72

- Revised Table 1.
- Revised Table 2.
- Revised Table 3.
- Revised Table 5.
- Modified Section 2.
- Added Section 3.
- Modified Section 4.

## Revision 0.72 to Revision 1.0

- Updated Table 3.
- Updated Section 6.

# CONTACT INFORMATION

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