



## LVDS 4x4 CROSSPOINT SWITCH

 Check for Samples: [SN65LVDT125A](#), [SN65LVDS125A](#)

### FEATURES

- Signaling Rates >1.5 Gbps per Channel
- Supports Telecom/Datacom and HDTV Video Switching
- Non-Blocking Architecture Allows Each Output to be Connected to Any Input
- Compatible With ANSI TIA/EIA-644-A LVDS Standard
- 25 mV of Input Voltage Threshold Hysteresis
- Propagation Delay Times, 900 ps Typical
- Inputs Electrically Compatible With LVPECL, CML and LVDS Signal Levels
- Operates From a Single 3.3-V Supply
- Integrated 110- $\Omega$  Line Termination Resistors Available With SN65LVDT125A

### APPLICATIONS

- Clock Buffering/Clock Muxing
- Wireless Base Stations
- High-Speed Network Routing
- HDTV Video Switching

### DESCRIPTION

The SN65LVDS125A and SN65LVDT125A are 4x4 nonblocking crosspoint switches. Low-voltage differential signaling (LVDS) is used to achieve signaling rates of 1.5 Gbps per channel. Each output driver includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVDT125A incorporates 110- $\Omega$  termination resistors for those applications where board space is a premium.

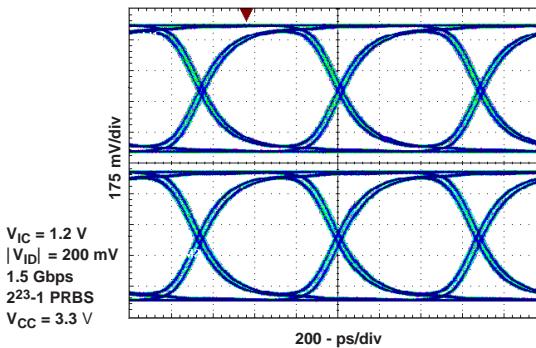
Designed to support signaling rates up to 1.5 Gbps for OC-12 clocks (622 MHz). The 1.5-Gbps signaling rate allows use in HDTV systems, including SMPTE 292 video applications requiring signaling rates of 1.485 Gbps.

The SN65LVDS125A and SN65LVDT125A are characterized for operation from -40°C to 85°C.

**SN65LVDS125ADBT (Marked as LVDS125A)  
SN65LVDT125ADBT (Marked as LVDT125A)**  
(TOP VIEW)

S10	1	38	VCC
S11	2	37	GND
1A	3	36	1Y
1B	4	35	1Z
S20	5	34	1DE
S21	6	33	2Y
2A	7	32	2Z
2B	8	31	2DE
GND	9	30	GND
VCC	10	29	VCC
GND	11	28	GND
3A	12	27	3Y
3B	13	26	3Z
S30	14	25	3DE
S31	15	24	4Y
4A	16	23	4Z
4B	17	22	4DE
S40	18	21	GND
S41	19	20	VCC

Eye Pattern of Two Outputs  
Operating Simultaneously

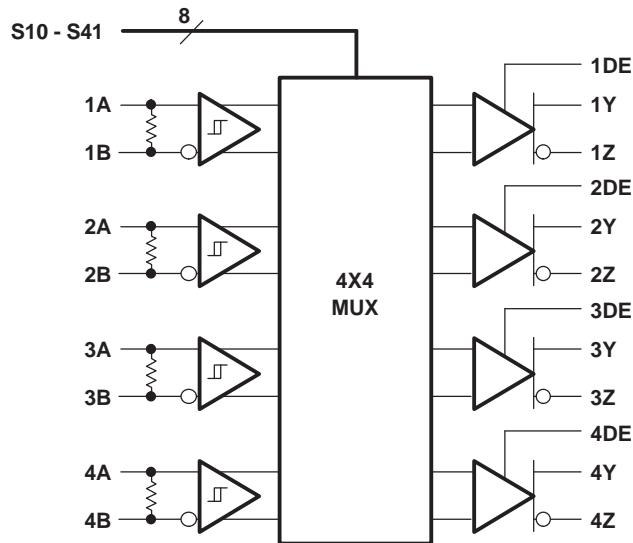


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### LOGIC DIAGRAM



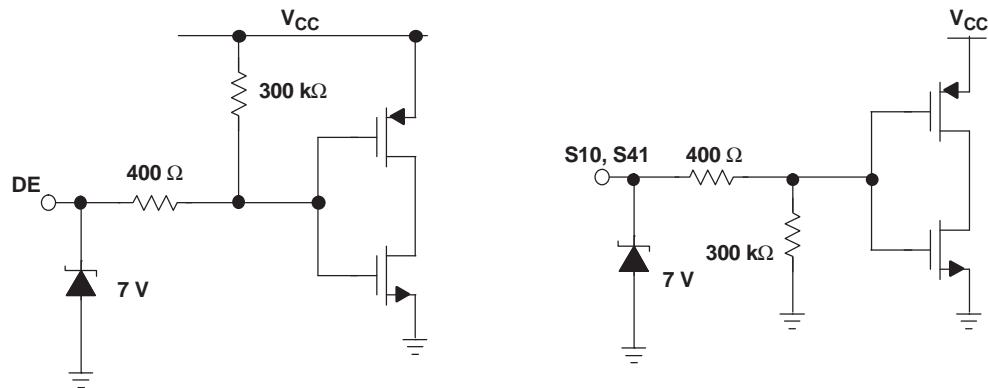
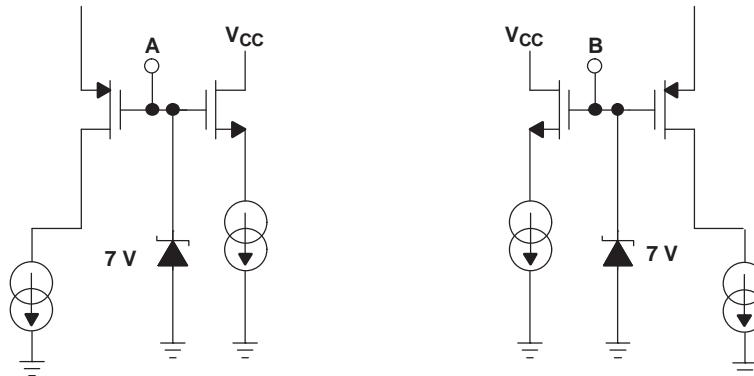
Integrated 110- $\Omega$  Termination on LVDT Only

### SN65LVDS125A Pin Description

Pin Numbers	Pin Description
S10 - S41	Inputs; Input channel to out output channel selection control pins
1A, 2A, 3A, 4A	Inputs; Positive leg of LVDS data input
1B, 2B, 3B, 4B	Inputs; Negative leg of LVDS data input
1Y, 2Y, 3Y, 4Y	Outputs; Positive leg of LVDS data output
1Z, 2Z, 3Z, 4Z	Outputs; Negative leg of LVDS data output
1DE, 2DE, 3DE, 4DE	Inputs; Output port disable
V <sub>CC</sub>	Input Voltage
GND	Ground

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS125A



OUTPUT LVDS125A

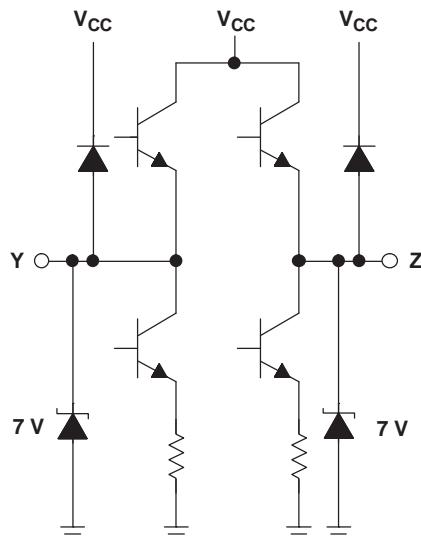


Table 1. CROSSPOINT LOGIC TABLES

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS	INPUT SELECTED	CONTROL PINS	INPUT SELECTED	CONTROL PINS	INPUT SELECTED	CONTROL PINS	INPUT SELECTED	CONTROL PINS	INPUT SELECTED	CONTROL PINS	INPUT SELECTED
<b>S10</b>	<b>S11</b>	<b>1Y/1Z</b>	<b>S20</b>	<b>S21</b>	<b>2Y/2Z</b>	<b>S30</b>	<b>S31</b>	<b>3Y/3Z</b>	<b>S40</b>	<b>S41</b>	<b>4Y/4Z</b>
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

## PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 85°C POWER RATING
TSSOP (DBT)	High-K <sup>(2)</sup>	1772 mW	15.4 mW/°C	847 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounded and with no air flow.  
 (2) In accordance with the High-K thermal metric definitions of EIA/JESD51-6.

## THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		VALUE	UNITS
θ <sub>JB</sub>	Junction-to-board thermal resistance			40.3	°C/W
θ <sub>JC</sub>				8.5	
P <sub>D</sub>	Device power dissipation	Typical	V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C, 750 MHz	356	mW
		Maximum	V <sub>CC</sub> = 3.6 V, T <sub>A</sub> = 85°C, 750 MHz	522	

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

			UNITS
Supply voltage range, V <sub>CC</sub>			-0.5 V to 4 V
Voltage range <sup>(2)</sup>	S, DE		-0.5 V to 4 V
	(A, B)		-0.5 V to 4 V
	V <sub>A</sub> - V <sub>B</sub>   (LVDT only)		1 V
	(Y, Z)		-0.5 V to 4 V
Electrostatic discharge	Human body model <sup>(3)</sup>	All pins	±3 kV
	Charged-device model <sup>(4)</sup>	All pins	±500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range			-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.  
 (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.  
 (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.  
 (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		3	3.3	3.6	V
High-level input voltage, $V_{IH}$	S10-S41, 1DE-4DE	2			V
Low-level input voltage, $V_{IL}$	S10-S41, 1DE-4DE			0.8	V
Magnitude of differential input voltage $ V_{ID} $	LVDS	0.1			V
	LVDT	0.1	0.8	0.8	V
Input voltage (any combination of common-mode or input signals)		0	3.3		V
Junction temperature, $T_J$				140	°C
Operating free-air temperature, $T_A$ <sup>(1)</sup>		-40	85		°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

## TIMING SPECIFICATIONS

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{SET}$	Input to select setup time		0.6		ns
$t_{HOLD}$			0.2		ns
$t_{SWITCH}$		1.2	1.6		ns

## INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$	Positive-going differential input voltage threshold	See Figure 1		100		mV
$V_{IT-}$	Negative-going differential input voltage threshold	See Figure 1	-100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis			25		mV
$I_{IH}$	High-level input current	$V_{IH} = 2$ V		-10		$\mu$ A
				20		$\mu$ A
$I_{IL}$	Low-level input current	$V_{IL} = 0.8$ V		-10		$\mu$ A
				20		$\mu$ A
$I_I$	Input current	$V_I = 0$ V or 3.3 V, Second input at 1.2 V (other input open for LVDT)	-20	20		$\mu$ A
$I_{I(OFF)}$	Input current	$V_{CC} \leq 1.5$ V, $V_I = 0$ V or 3.3 V, Second input at 1.2 V (other input open for LVDT)	-20	20		$\mu$ A
$I_{IO}$	Input offset current ( $ I_{IA} - I_{IB} $ ) ('LVDS)	$V_{IA} = V_{IB}$ , $0 \leq V_{IA} \leq 3.3$ V	-6	6		$\mu$ A
$R_T$	Termination resistance ('LVDT)	$V_{ID} = 300$ mV, $V_{IC} = 0$ V to 3.3 V	90	110	132	$\Omega$
	Termination resistance ('LVDT with power-off)	$V_{ID} = 300$ mV, $V_{IC} = 0$ V to 3.3 V, $V_{CC} = 1.5$ V	90	110	132	
$C_T$	Differential input capacitance			0.6		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

## OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Differential output voltage magnitude See Figure 2, V <sub>ID</sub> = ±100 mV	247	350	454	mV
Δ V <sub>OD</sub>		-50	50	50	mV
V <sub>OC(ss)</sub>	Steady-state common-mode output voltage See Figure 3	1.125	1.375	1.375	V
ΔV <sub>OC(ss)</sub>		-50	50	50	mV
V <sub>OC(pp)</sub>		50	150	150	mV
I <sub>CC</sub>	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 1 pF	107	145	145	mA
I <sub>OS</sub>	V <sub>OY</sub> or V <sub>OZ</sub> = 0 V	-27	27	27	mA
I <sub>OSD</sub>	V <sub>OD</sub> = 0 V	-12	12	12	mA
I <sub>OZ</sub>	V <sub>O</sub> = 0 V or V <sub>CC</sub>	-1	±1	±1	μA
C <sub>O</sub>		1.2		1.2	pF

(1) All typical values are at 25°C and with a 3.3 V supply.

## SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output See Figure 4	700	900	1200	ps
t <sub>PHL</sub>		700	900	1200	
t <sub>r</sub>		210	270	270	
t <sub>f</sub>		210	270	270	
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  ) <sup>(1)</sup>	0	50	50	ps
t <sub>sk(o)</sub>	Channel-to-channel output skew <sup>(2)</sup>			150	ps
t <sub>sk(pp)</sub>	Part-to-part skew <sup>(3)</sup>			300	ps
t <sub>jit(per)</sub>	Period jitter, rms (1 standard deviation) <sup>(4)</sup>	750 MHz clock input <sup>(5)</sup> (see Figure 6)	0.4	3	ps
t <sub>jit(cc)</sub>	Cycle-to-cycle jitter (peak) <sup>(4)</sup>	750 MHz clock input <sup>(6)</sup> (see Figure 6)	4.7	13	ps
t <sub>jit(pp)</sub>	Peak-to-peak jitter <sup>(4)</sup>	1.5 Gbps 2 <sup>23</sup> -1 PRBS input <sup>(7)</sup> (see Figure 6)	65	110	ps
t <sub>jit(det)</sub>	Deterministic jitter, peak-to-peak <sup>(4)</sup>	1.5 Gbps 2 <sup>7</sup> -1 PRBS input <sup>(8)</sup> (see Figure 6)	56	90	ps
t <sub>PHZ</sub>	Propagation delay, high-level-to-high-impedance output			6	ns
t <sub>PLZ</sub>	Propagation delay, low-level-to-high-impedance output			6	
t <sub>PZH</sub>	Propagation delay, high-impedance-to-high-level output			300	
t <sub>PZL</sub>	Propagation delay, high-impedance-to-low-level output			300	

(1) t<sub>sk(p)</sub> is the magnitude of the time difference between the t<sub>PLH</sub> and t<sub>PHL</sub> of any output of a single device.

(2) t<sub>sk(o)</sub> is the maximum delay time difference between drivers over temperature, V<sub>CC</sub>, and process.

(3) t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) Jitter specifications are based on design and characterization. Stimulus system jitter of 1.9 ps t<sub>jit(per)</sub>, 16 ps t<sub>jit(cc)</sub>, 17 ps t<sub>jit(pp)</sub>, and 7.2 ps t<sub>jit(det)</sub> have been subtracted from the values.

(5) Input voltage = V<sub>ID</sub> = 200 mV, 50% duty cycle at 750 MHz, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%), measured over 1000 samples.

(6) Input voltage = V<sub>ID</sub> = 200 mV, 50% duty cycle at 750 MHz, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%).

(7) Input voltage = V<sub>ID</sub> = 200 mV, 2<sup>23</sup>-1 PRBS pattern at 1.5 Gbps, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%), measured over 200k samples.

(8) Input voltage = V<sub>ID</sub> = 200 mV, 2<sup>7</sup>-1 PRBS pattern at 1.5 Gbps, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%).

## PARAMETER MEASUREMENT INFORMATION

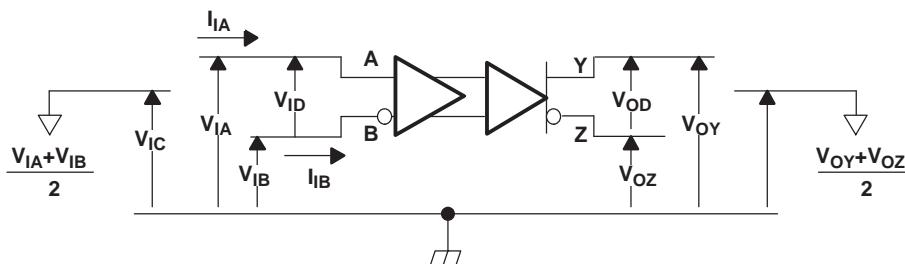


Figure 1. Voltage and Current Definitions

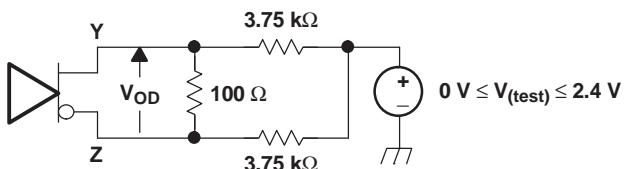
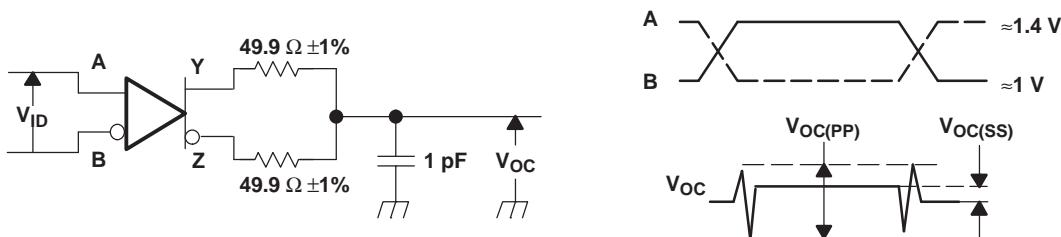
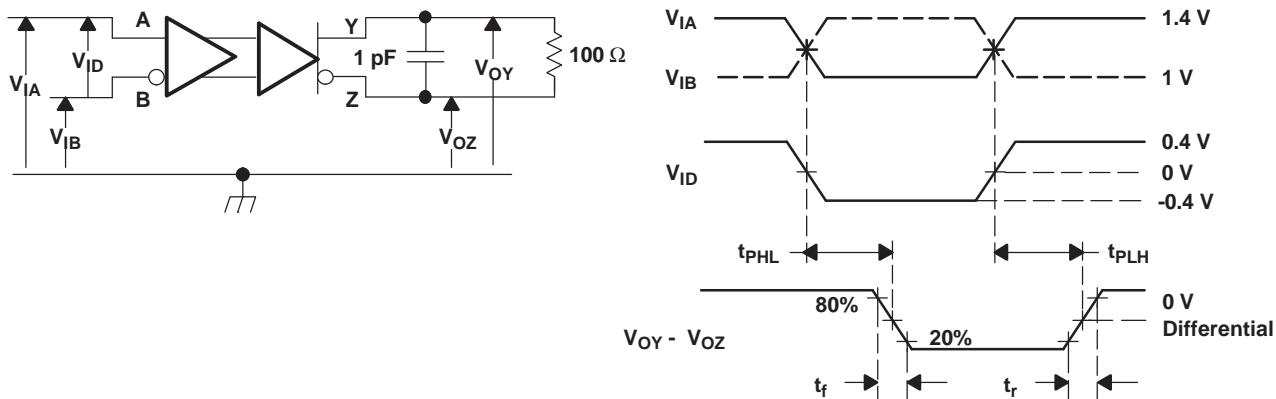


Figure 2. Differential Output Voltage ( $V_{OD}$ ) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns;  $R_L = 100\Omega$ ;  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of  $V_{OC(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

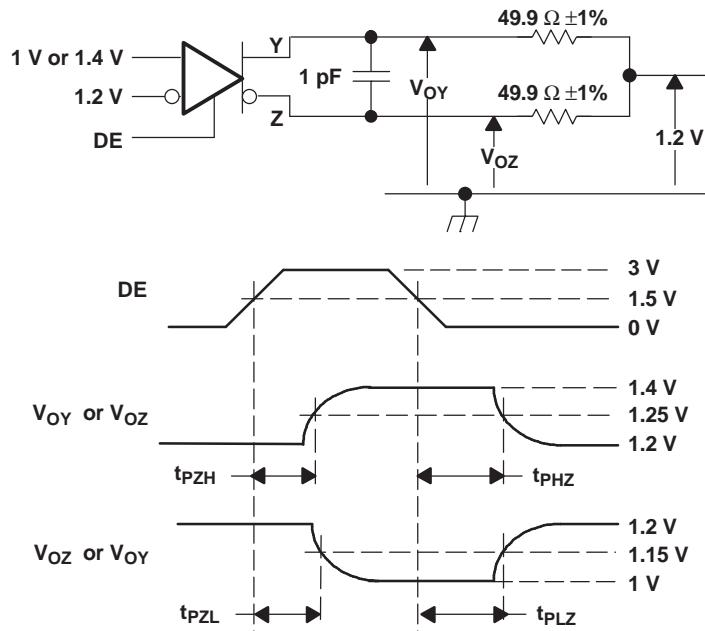
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq .25$  ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

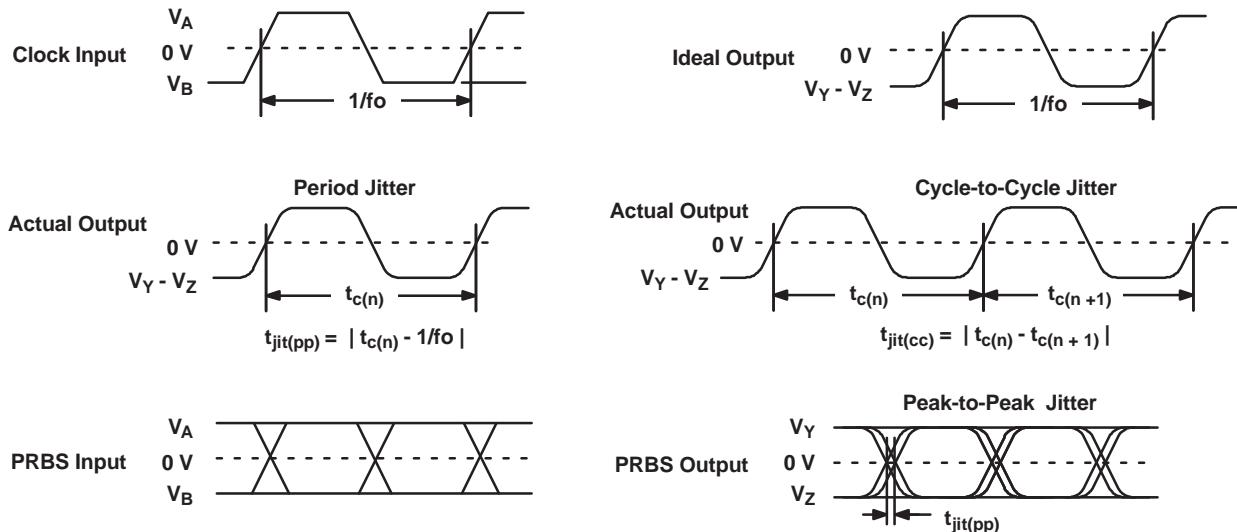
Figure 4. Timing Test Circuit and Waveforms

## PARAMETER MEASUREMENT INFORMATION (continued)



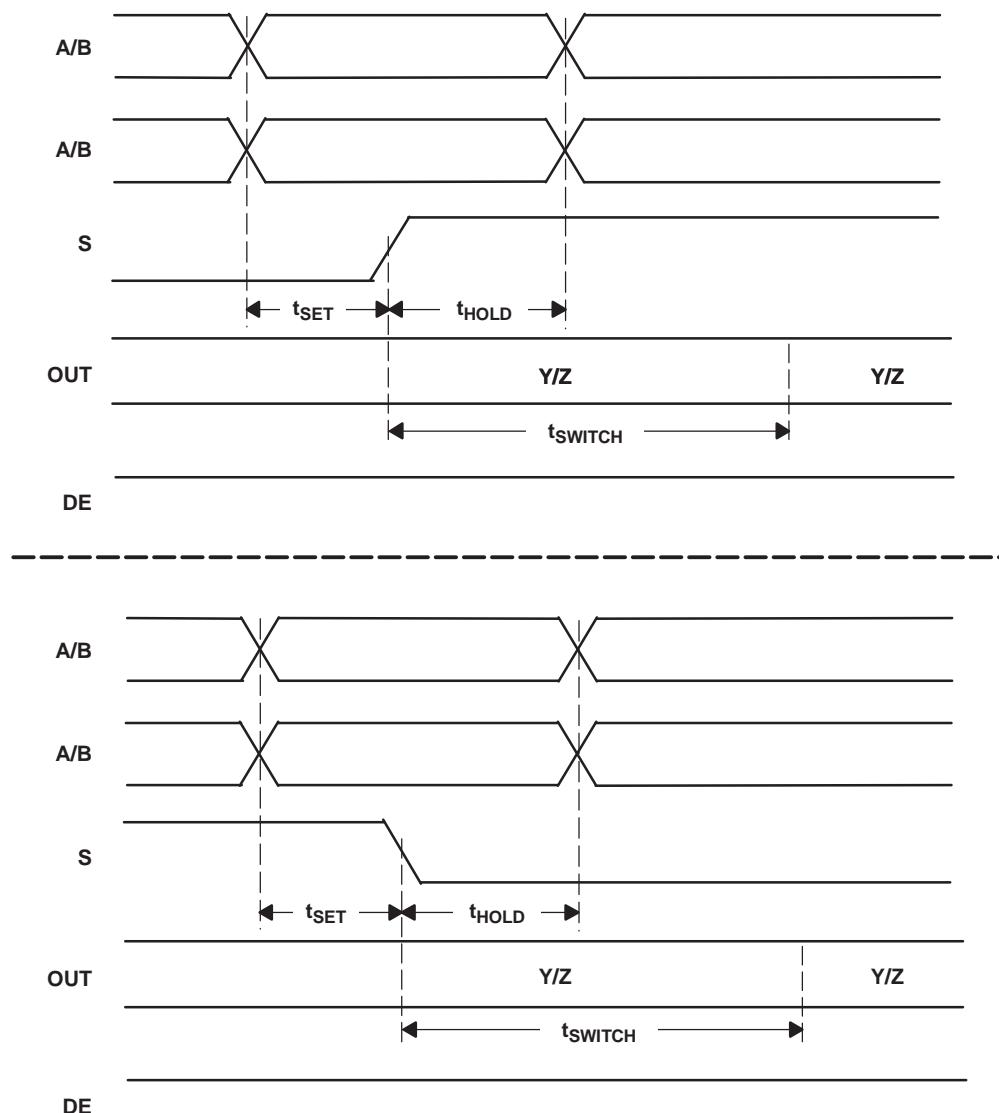
NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions



NOTE: All input pulses are supplied by an Agilent 81250 Stimulus System. The measurement is made on a TEK TDS6604 running TDSJIT3 application software.

Figure 6. Driver Jitter Measurement Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)**


NOTE:  $t_{SET}$  and  $t_{HOLD}$  times specify that data must be in a stable state before and after mux control switches.

**Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times**

## TYPICAL CHARACTERISTICS

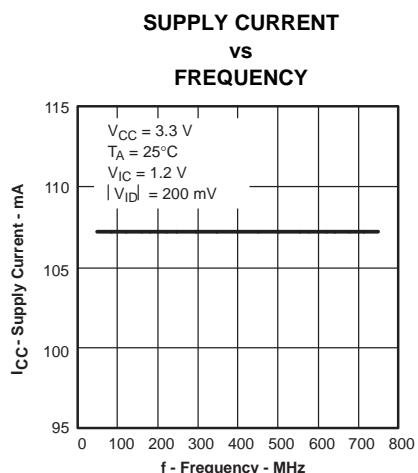


Figure 8.

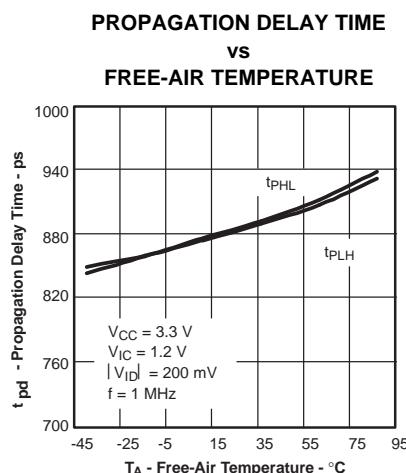


Figure 9.

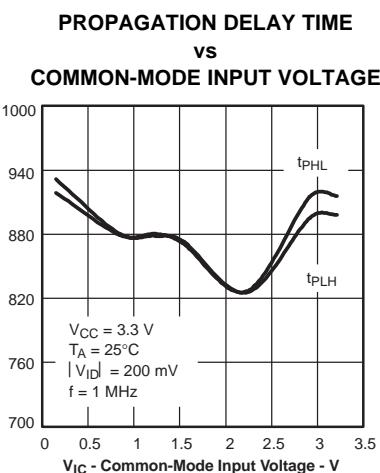


Figure 10.

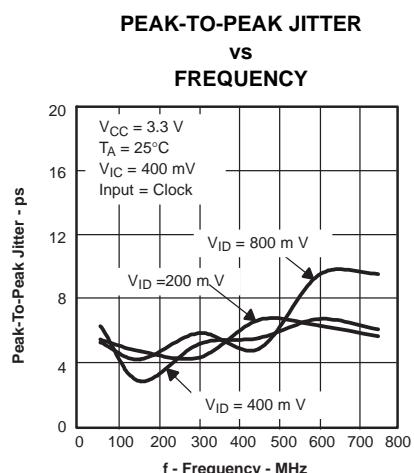


Figure 11.

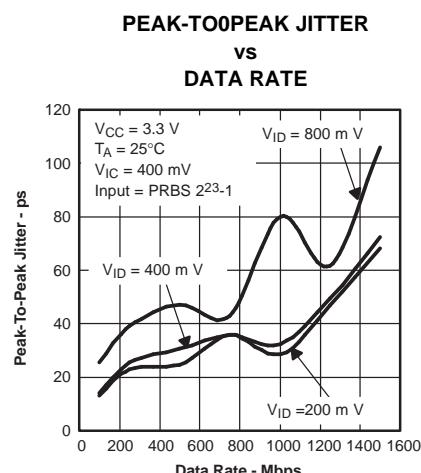


Figure 12.

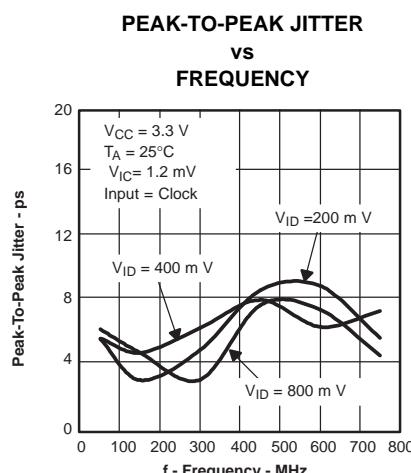


Figure 13.

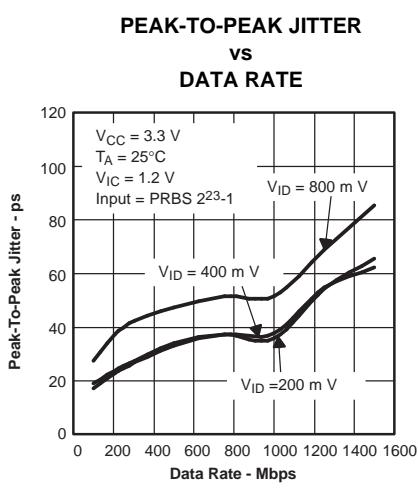


Figure 14.

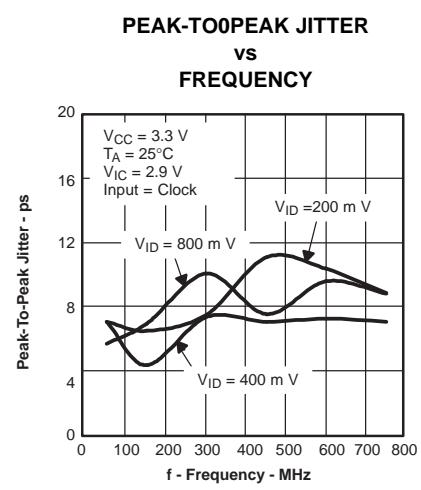


Figure 15.

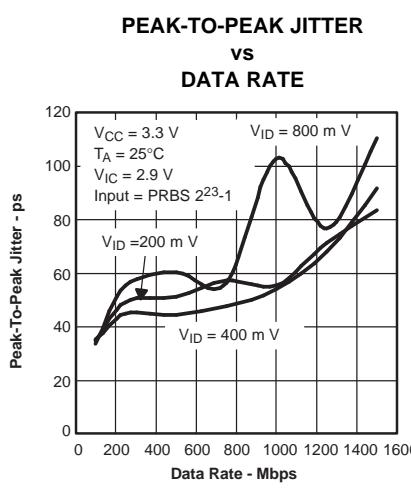
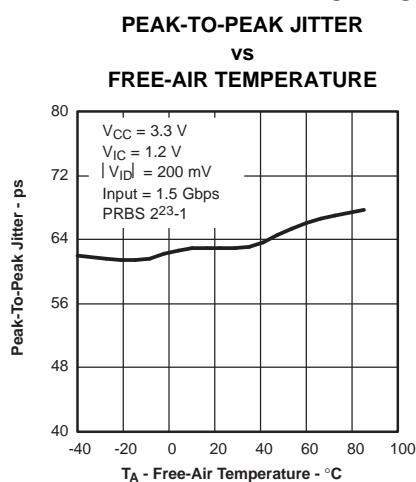
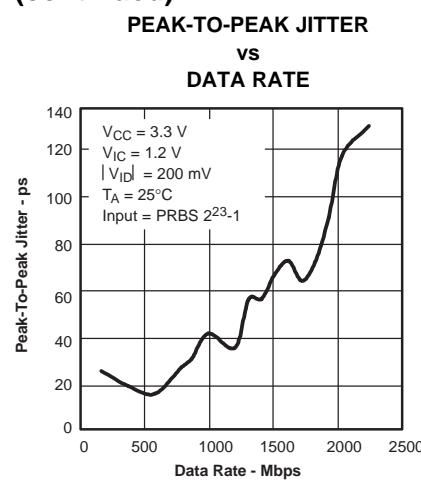


Figure 16.

**TYPICAL CHARACTERISTICS (continued)**



**Figure 17.**



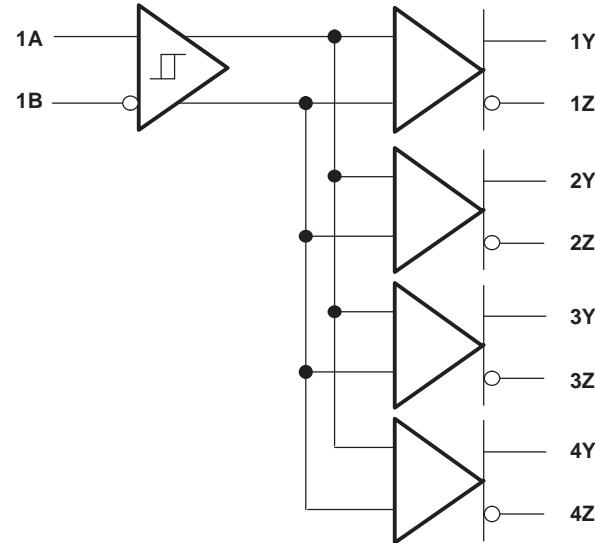
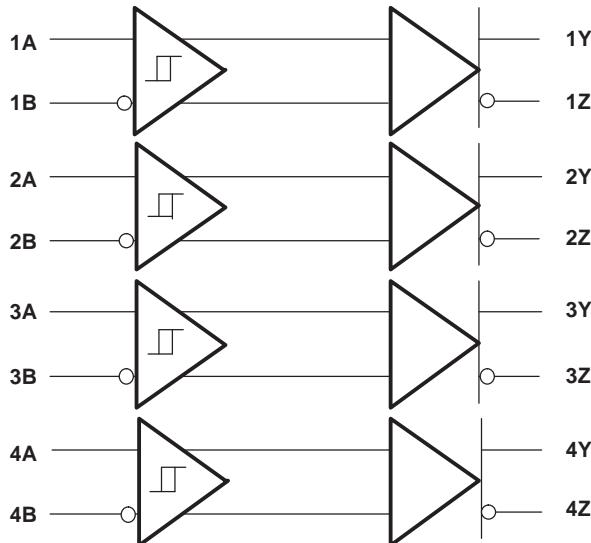
**Figure 18.**

## APPLICATION INFORMATION

### CONFIGURATION EXAMPLES

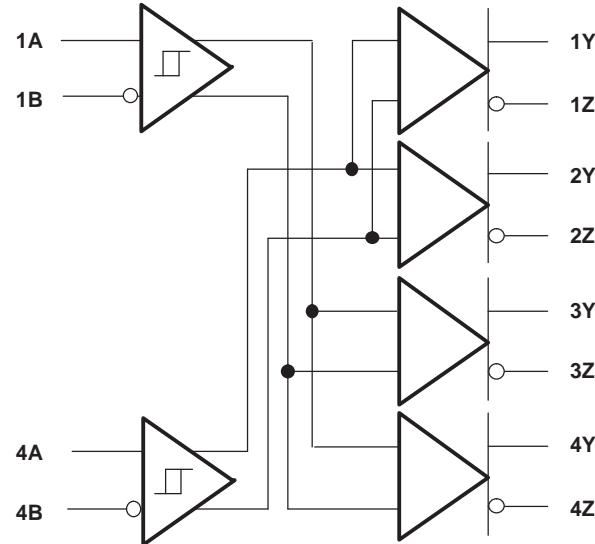
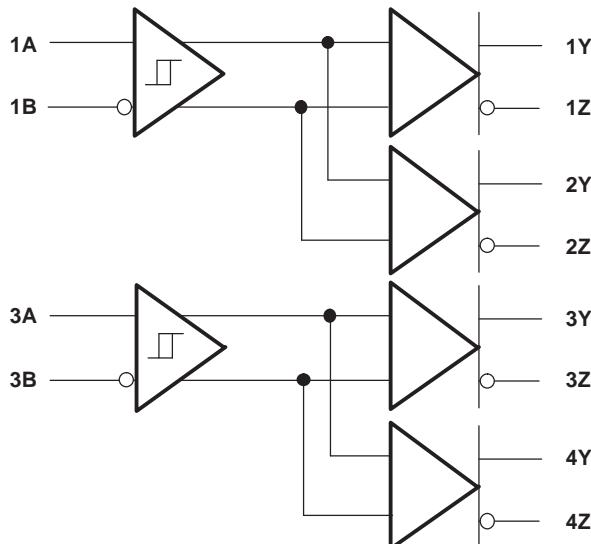
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1

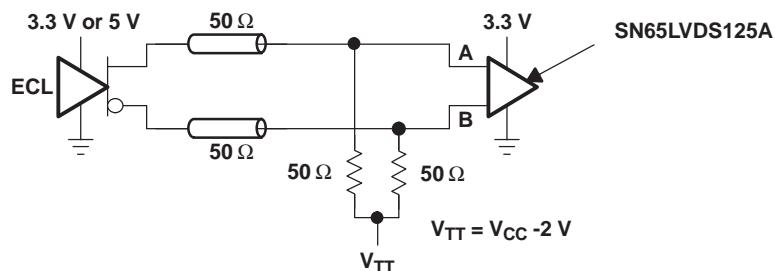
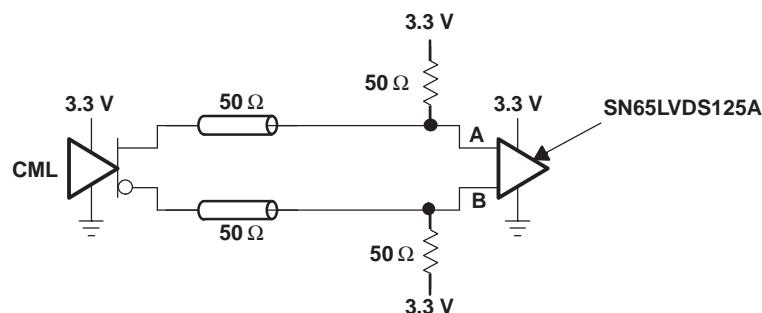
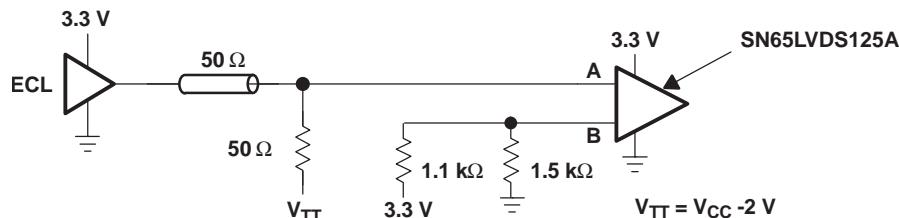
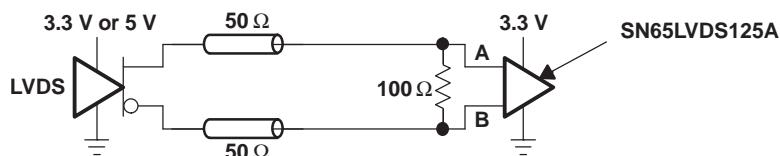
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0

S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



**TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)**

**Figure 20. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)**

**Figure 21. Current-Mode Logic (CML)**

**Figure 22. Single-Ended (LVPECL)**

**Figure 23. Low-Voltage Differential Signaling (LVDS)**

See the EVM Users Guide ([SLLU064](#)) for example board layout and schematics examples.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65LVDS125ADBT</a>	Active	Production	TSSOP (DBT)   38	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A
SN65LVDS125ADBT.B	Active	Production	TSSOP (DBT)   38	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A
<a href="#">SN65LVDS125ADBTR</a>	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A
SN65LVDS125ADBTR.B	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A
SN65LVDS125ADBTRG4	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A
SN65LVDS125ADBTRG4.B	Active	Production	TSSOP (DBT)   38	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A
<a href="#">SN65LVDT125ADBT</a>	Active	Production	TSSOP (DBT)   38	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT125A
SN65LVDT125ADBT.B	Active	Production	TSSOP (DBT)   38	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT125A
SN65LVDT125ADBTG4	Active	Production	TSSOP (DBT)   38	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT125A
SN65LVDT125ADBTG4.B	Active	Production	TSSOP (DBT)   38	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT125A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

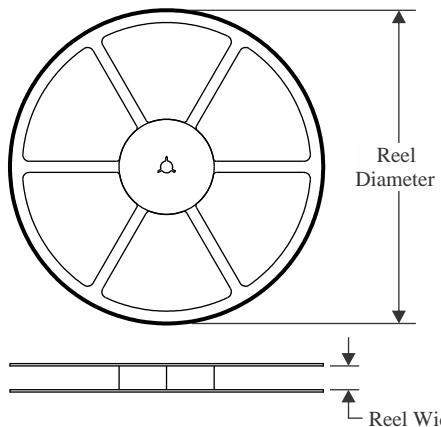
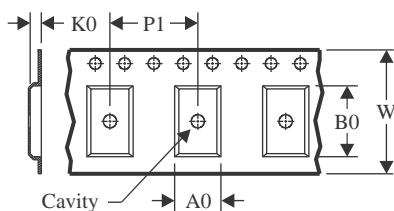
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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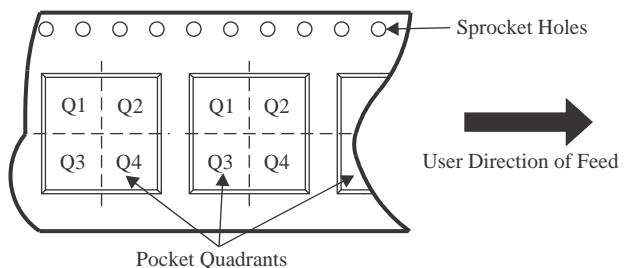
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


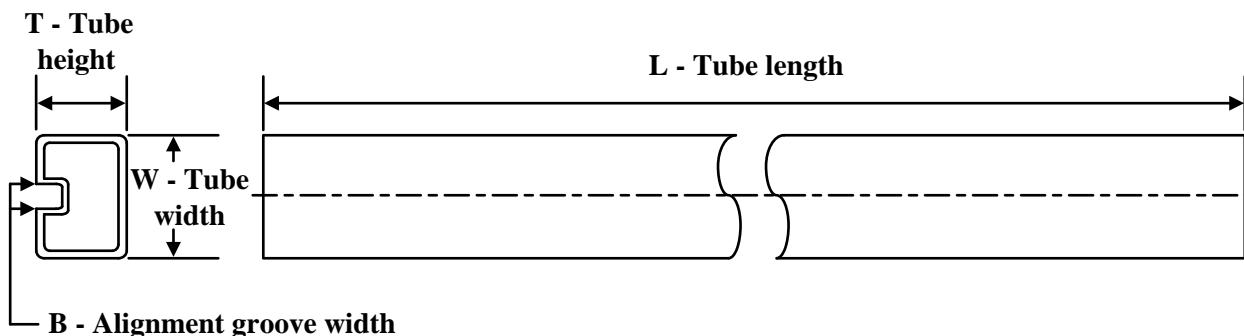
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS125ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDS125ADBTRG4	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS125ADBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0
SN65LVDS125ADBTRG4	TSSOP	DBT	38	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

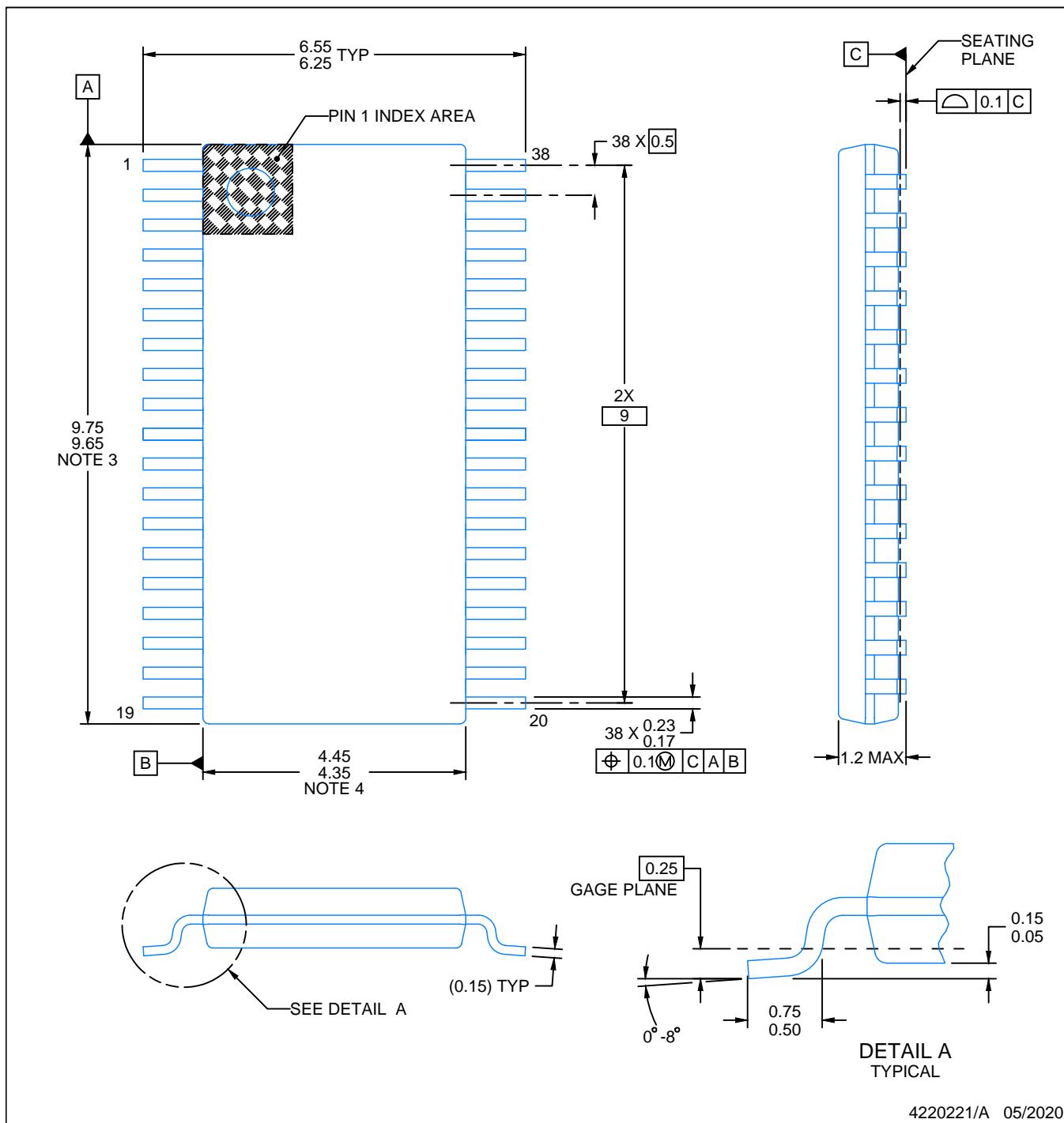
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
SN65LVDS125ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDS125ADBT.B	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT125ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT125ADBT.B	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT125ADBTG4	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT125ADBTG4.B	DBT	TSSOP	38	50	530	10.2	3600	3.5

# PACKAGE OUTLINE

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

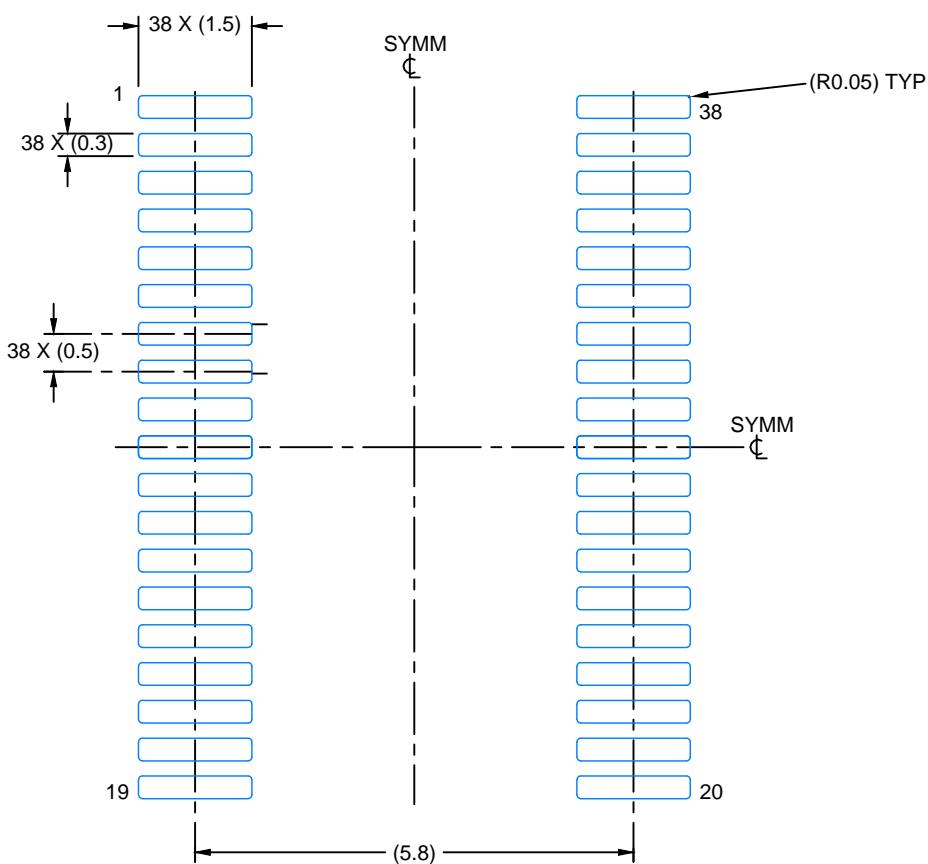
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

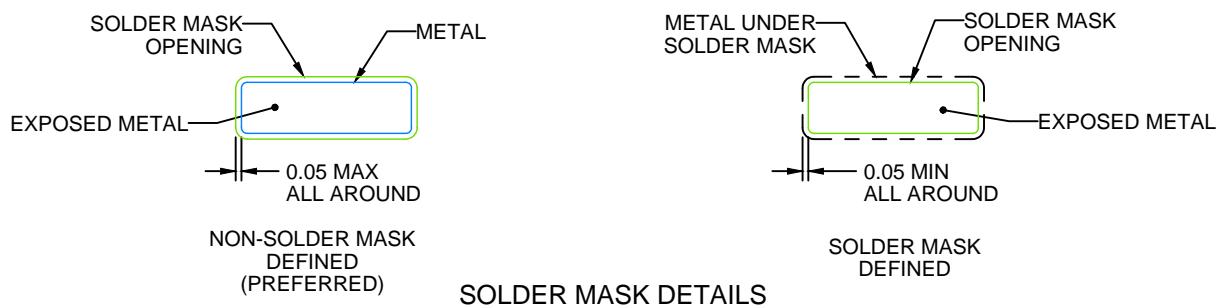
DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

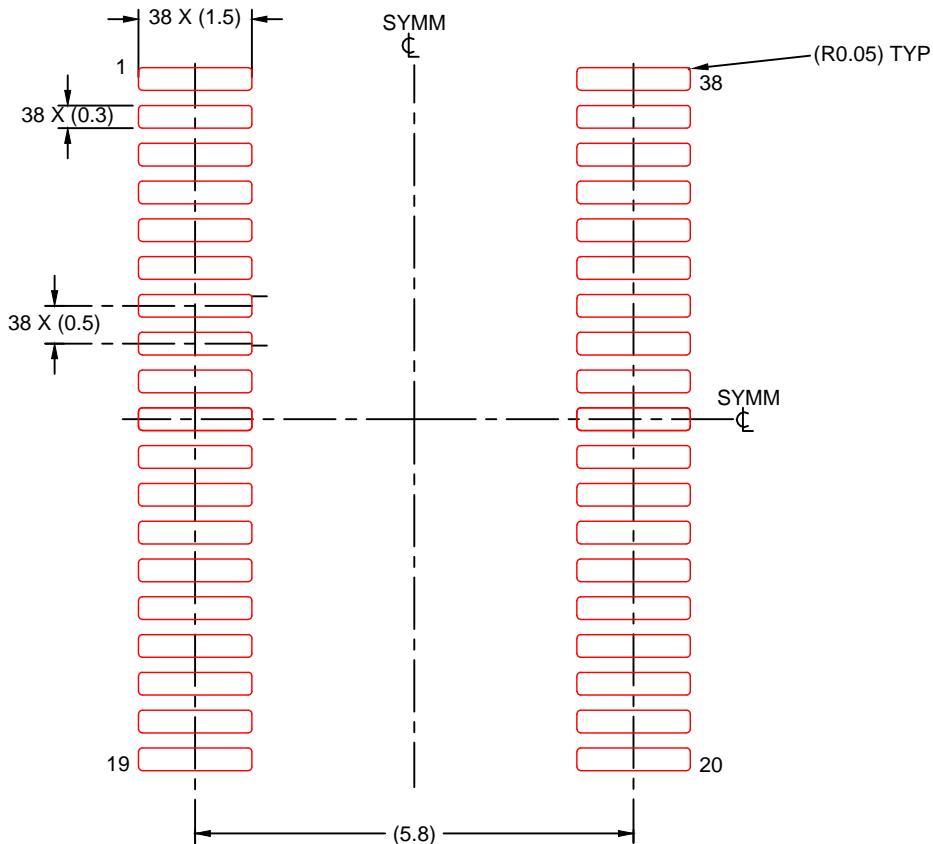
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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