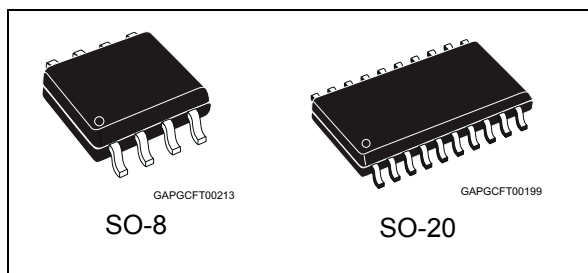


Automotive low drop voltage regulator

Datasheet - production data



Description

The L4993 is a monolithic integrated 5 V Voltage regulator with a low drop voltage at currents up to 150 mA. The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40 V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4993 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4993 watchdog is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

Features

Max DC supply voltage	V_S	40 V
Max output voltage tolerance	ΔV_0	+/-2%
Max dropout voltage	V_{dp}	400 mV
Output current	I_O	150 mA
Quiescent current	I_{qn}	79 μA ⁽¹⁾

1. Typical value with watchdog disabled.

- AEC-Q100 qualified
- Operating DC supply voltage range 5.6 V to 31 V
- Reset circuit sensing the output voltage down to 1 V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range ($T_j = -40^\circ C$ to $150^\circ C$)



Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
SO-8	—	L4993DTR
SO-20 (16+2+2)	L4993MD	L4993MDTR

Contents

1	Block diagram and pins description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	7
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	11
2.5	Test circuit and waveforms plot	14
2.5.1	Load regulation	14
3	Application information	16
3.1	Voltage regulator	16
3.2	Reset	17
3.3	Watchdog	18
4	Package and PCB thermal data	19
4.1	SO-8 thermal data	19
4.2	SO-20 thermal data	22
5	Package and packing information	25
5.1	ECOPACK®	25
5.2	SO-8 package information	25
5.3	SO-20 package information	27
5.4	SO-8 packing information	28
5.5	SO-20 packing information	29
6	Revision history	30

List of tables

Table 1.	Device summary	1
Table 2.	Pins description	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data	7
Table 5.	General	8
Table 6.	Reset	9
Table 7.	Watchdog	9
Table 8.	Watchdog Enable	10
Table 9.	SO-8 thermal parameter	21
Table 10.	SO-20 thermal parameter	24
Table 11.	SO-8 mechanical data	25
Table 12.	SO-20 mechanical data	27
Table 13.	Document revision history	30

List of figures

Figure 1.	Block diagram	5
Figure 2.	Pins configuration	6
Figure 3.	Output voltage vs. T_j	11
Figure 4.	Output voltage vs. V_s	11
Figure 5.	Drop Voltage vs. Output Current	11
Figure 6.	Current consumption vs. Output Current	11
Figure 7.	Current consumption vs. Input Voltage	11
Figure 8.	Current limitation vs. T_j	11
Figure 9.	Current limitation vs. Input Voltage	12
Figure 10.	Short Circuit Current vs. T_j	12
Figure 11.	Short Circuit Current vs. Input Voltage	12
Figure 12.	V_{WEn_high} vs. T_j	12
Figure 13.	V_{WEn_LOW} vs. T_j	12
Figure 14.	V_{rhth} vs. T_j	12
Figure 15.	V_{rlth} vs. T_j	13
Figure 16.	V_{whth} vs. T_j	13
Figure 17.	V_{wlth} vs. T_j	13
Figure 18.	I_{cr} & I_{cwc} vs. T_j	13
Figure 19.	I_{dr} & I_{cwd} vs. T_j	13
Figure 20.	T_{wop} vs. T_j	13
Figure 21.	PSRR	14
Figure 22.	Load regulation test circuit	14
Figure 23.	Maximum load variation response	15
Figure 24.	L4993 application schematic	16
Figure 25.	Behavior of output current versus regulated voltage V_o	17
Figure 26.	Reset timing diagram	18
Figure 27.	Watchdog timing diagram	18
Figure 28.	SO-8 PC board	19
Figure 29.	$R_{thj-amb}$ Vs. PCB copper area in open box free air condition	19
Figure 30.	SO-8 thermal impedance junction ambient single pulse	20
Figure 31.	Thermal fitting model of V_{reg} in SO-8	20
Figure 32.	SO-20 PC board	22
Figure 33.	$R_{thj-amb}$ Vs. PCB copper area in open box free air condition	22
Figure 34.	SO-20 thermal impedance junction ambient single pulse	23
Figure 35.	Thermal fitting model of V_{reg} in SO-20	23
Figure 36.	SO-8 package dimensions	25
Figure 37.	SO-20 package dimensions	27
Figure 38.	SO-8 tape and reel shipment (suffix "TR")	28
Figure 39.	SO-20 tube shipment (no suffix)	29
Figure 40.	SO-20 tape and reel shipment (suffix "TR")	29

1 Block diagram and pins description

Figure 1. Block diagram

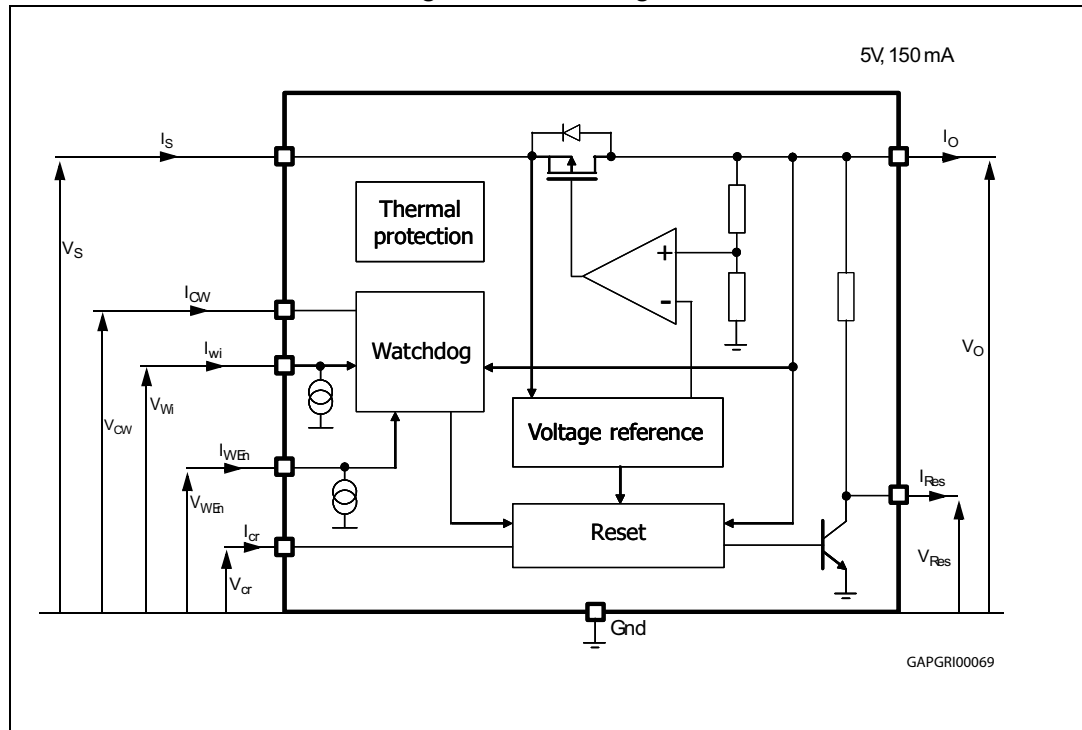
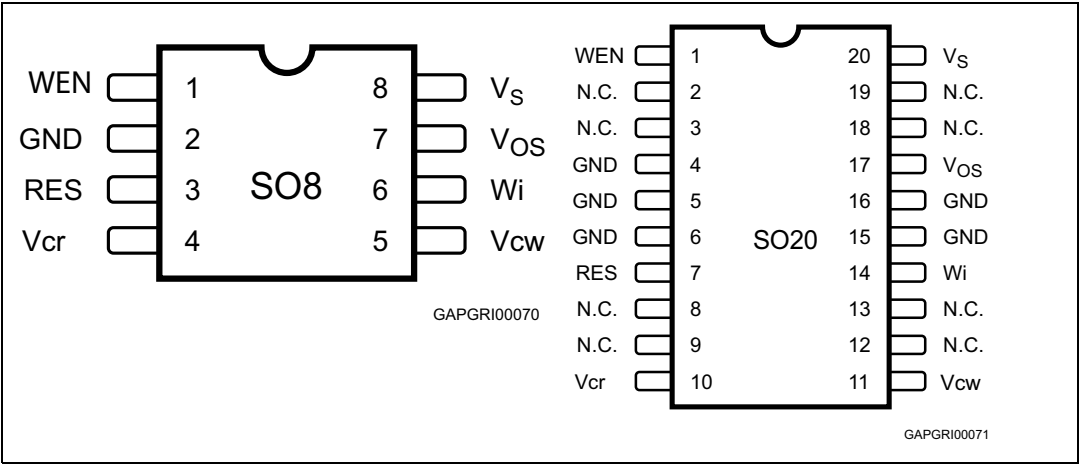


Table 2. Pins description

Pin name	SO-8 (D)	SO-20 (MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low. Leave floating if not used.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated. Connect to ground if not used
Vo_s	7	17	Voltage regulator output Block to ground with a capacitor >100 nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2. Pins configuration



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC supply voltage	-0.3 to 40	V
I_{VSDC}	Input current	Internally limited	
V_{VO}	DC output voltage	-0.3 to 6 ⁽¹⁾	V
I_{VO}	DC output current	Internally limited	
V_{WI}	Watchdog input voltage	-0.3 to $V_{VO} + 0.3$	V
V_{OD}	Open drain output voltage	-0.3 to $V_{VO} + 0.3$	V
I_{OD}	Open drain output current	Internally limited	
V_{CR}	Reset delay voltage	-0.3 to $V_{VO} + 0.3$	V
V_{CW}	Watchdog delay voltage	-0.3 to $V_{VO} + 0.3$	V
V_{WEN}	Watchdog Enable input voltage	-0.3 to $V_{VO} + 0.3$	V
T_J	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

1. Using the typical application schematic with $C_{out} = 10 \mu F$ and $I_{out} = 0 A$, when the regulator is switched-on, an overshoot exceeding 6 V could occur. This behavior does not impact the reliability of the regulator.

2.2 Thermal data

For details, please refer to [Section 4.1: SO-8 thermal data](#) and [Section 4.2: SO-20 thermal data](#).

Table 4. Thermal data⁽¹⁾

Symbol	Parameter	Value	Unit
$R_{th-jamb}$	Thermal resistance Junction to Ambient:		
	SO-8	130	°C/W
	SO-20	51	°C/W

1. The values quoted are for PCB FR4 area = 58mm x 58mm, PCB thickness = 2 mm, Cu thickness = 35 μm , Copper areas: SO-8 = 2 cm², SO-20 = 6 cm².

2.3 Electrical characteristics

Values specified in this section are for $V_s = 5.6 \text{ V}$ to 31 V , $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$ unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	V_{o_ref}	Output voltage	$V_s = 6 \text{ to } 31 \text{ V}$ $I_o = 1 \text{ to } 150 \text{ mA}$	4.9	5.0	5.1	V
Vo	I_{short}	Short circuit current	$V_s = 13.5 \text{ V}^{(1)}$	150	280	400	mA
Vo	$I_{lim}^{(2)}$	Output current limitation	$V_s = 13.5 \text{ V}^{(1)}$	150	320	500	mA
Vs, Vo	V_{line}	Line regulation voltage	$V_s = 6 \text{ to } 31 \text{ V}$ $I_o = 1 \text{ to } 150 \text{ mA}$			25	mV
Vo	V_{load}	Load regulation voltage	$I_o = 1 \text{ to } 150 \text{ mA}$			25	mV
Vs, Vo	$V_{dp}^{(3)}$	Drop voltage	$I_o = 150 \text{ mA}$		200	400	mV
Vs, Vo	SVR	Ripple rejection	$f_r = 100 \text{ Hz}^{(4)}$	55			dB
Vs, Vo	I_{qn_150}	Quiescent current	$V_s = 13.5 \text{ V}$, $I_o = 150 \text{ mA}$, $WEn = \text{high}$		1.25	2	mA
Vs, Vo	I_{qn_50}	Quiescent current	$V_s = 13.5 \text{ V}$, $I_o = 50 \text{ mA}$, $WEn = \text{high}$		470	1000	μA
Vs, Vo	I_{qn_1}	Quiescent current	$V_s = 13.5 \text{ V}$, $I_o < 1 \text{ mA}$, $WEn = \text{high}$		100	180	μA
Vs, Vo	I_{qs}	Quiescent current with watchdog regulator disabled	$V_s = 13.5 \text{ V}$, $I_o < 1 \text{ mA}$, $WEn = \text{low}$		79	125	μA
	T_w	Thermal protection temperature		150		190	$^\circ\text{C}$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^\circ\text{C}$

1. See [Figure 25](#).
2. Measured output current when the output voltage has dropped 100 mV from its nominal value obtained at $V_s = 13.5 \text{ V}$ and $I_o = 75 \text{ mA}$.
3. V_s - V_o measured when the output voltage has dropped 100mV from its nominal value obtained at $V_s = 13.5 \text{ V}$ and $I_o = 75 \text{ mA}$.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	$R_{ext} = 5\text{ k}\Omega$ to V_o , $V_o > 1\text{ V}$			0.4	V
Res	I_{Res_h}	Reset output high leakage current	$V_{Res} = 5\text{ V}$			1	μA
Res	R_p_u	Pull up internal resistance	With respect to V_o	12	25	50	$\text{k}\Omega$
Res	V_{o_th}	V_o out of regulation threshold	$V_s = 6$ to 31 V , $I_o = 1$ to 150 mA	6%	8%	10%	Below V_{o_ref}
Vcr	Vrlth	Reset delay circuit low threshold	$V_s = 13.5\text{ V}$	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset delay circuit high threshold	$V_s = 13.5\text{ V}$	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	$V_s = 13.5\text{ V}$	8	17.6	30	μA
Vcr	Idr	Discharge current	$V_s = 13.5\text{ V}$	8	17.6	30	μA
Res	Trr_2	Reset reaction time ⁽¹⁾	$V_o = V_{o_th} - 100\text{ mV}$	100	275	1000	μs
Res	Trd	Reset delay time	$V_s = 13.5\text{ V}$, $C_{tr} = 1\text{ nF}$	65		150	ms

1. When V_o becomes lower than 4 V, the reset reaction time decreases down to 2 μs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	Vih	Input high voltage	$V_s = 13.5\text{ V}$	3.5			V
Wi	Vil	Input low voltage	$V_s = 13.5\text{ V}$			1.5	V
Wi	Vih_hyst	Input hysteresis	$V_s = 13.5\text{ V}$		500		mV
Wi	li	Pull down current	$V_s = 13.5\text{ V}$		10	20	μA
Vcw	Vwhth	High threshold	$V_s = 13.5\text{ V}$	44%	47%	50%	V_{o_ref}
Vcw	Vwlth	Low threshold	$V_s = 13.5\text{ V}$	10%	13%	16%	V_{o_ref}
Vcw	Icwc	Charge current	$V_s = 13.5\text{ V}$, $V_{cw} = 0.1\text{ V}$	4	8	14	μA

Table 7. Watchdog (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vcw	Icwd	Discharge current	Vs = 13.5 V, Vcw = 2.5 V	1.0	2.13	4.5	μA
Vcw	Twop	Watchdog period	Vs = 13.5 V, Ctw = 47 nF	25	50	90	ms
Res	twol	Watchdog output low time	Vs = 13.5 V, Ctw = 47 nF	6	10.5	22	ms

Table 8. Watchdog Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WEn	W _{En_low}	Enable input low voltage				1	V
WEn	W _{En_high}	Enable input high voltage		3			V
WEn	W _{En_hyst}	Enable input hysteresis		500	800	1100	mV
WEn	I _{leak}	Pull down current	WEn = 5 V	2	8	20	μA

2.4 Electrical characteristics curves

Figure 3. Output voltage vs. Tj

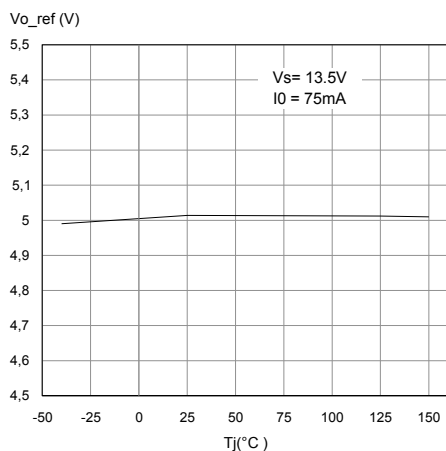


Figure 4. Output voltage vs. Vs

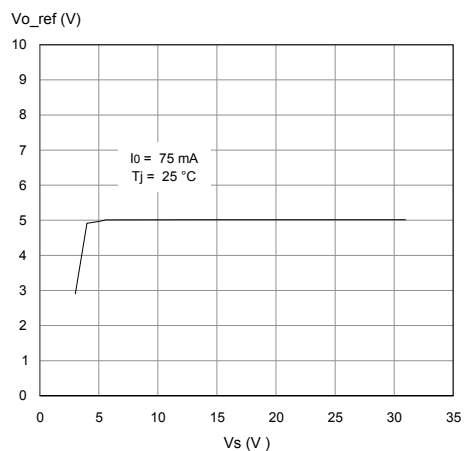


Figure 5. Drop Voltage vs. Output Current

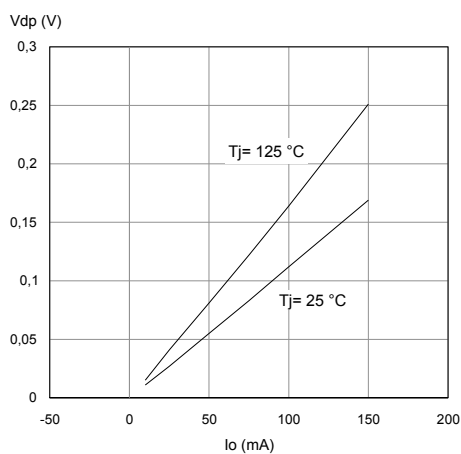


Figure 6. Current consumption vs. Output Current

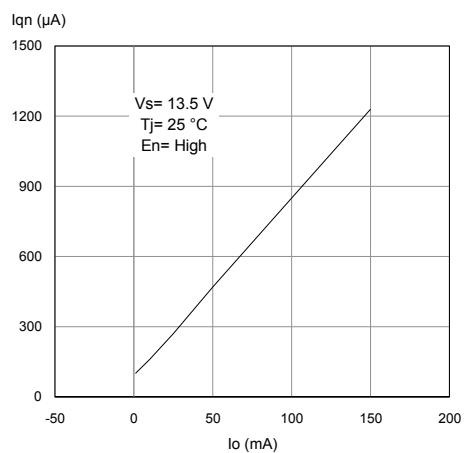


Figure 7. Current consumption vs. Input Voltage

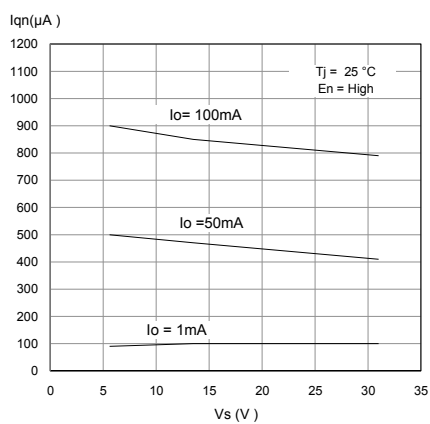


Figure 8. Current limitation vs. Tj

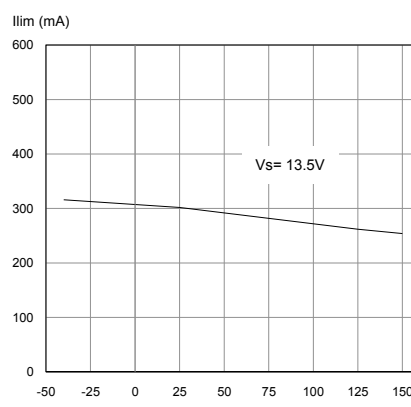


Figure 9. Current limitation vs. Input Voltage

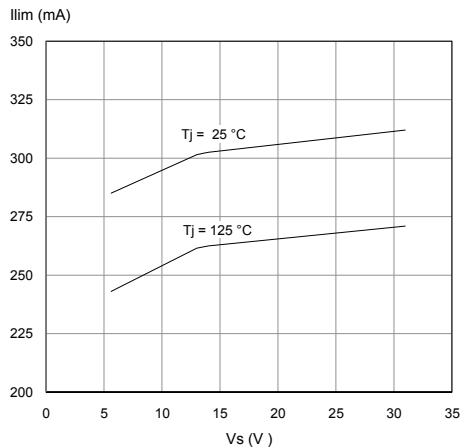


Figure 10. Short Circuit Current vs. Tj

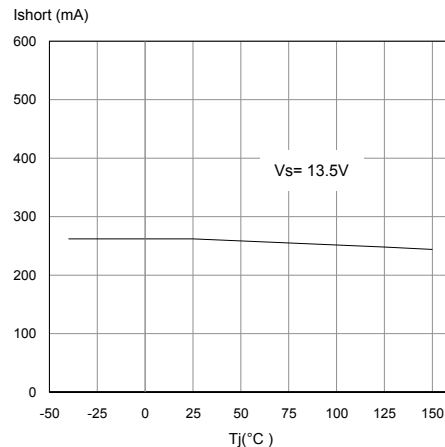


Figure 11. Short Circuit Current vs. Input Voltage

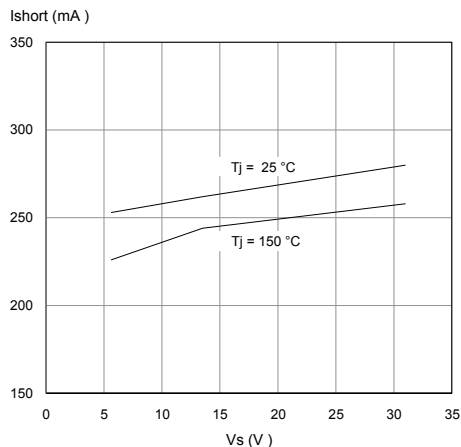


Figure 12. V_{WEn_high} vs. Tj

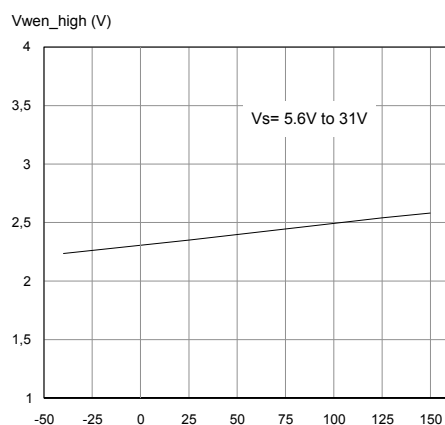


Figure 13. V_{WEn_LOW} vs. Tj

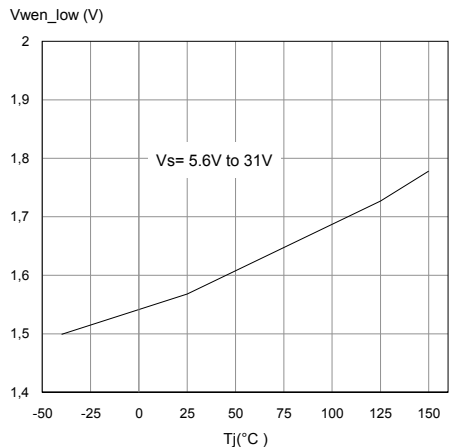


Figure 14. V_{rhth} vs. Tj

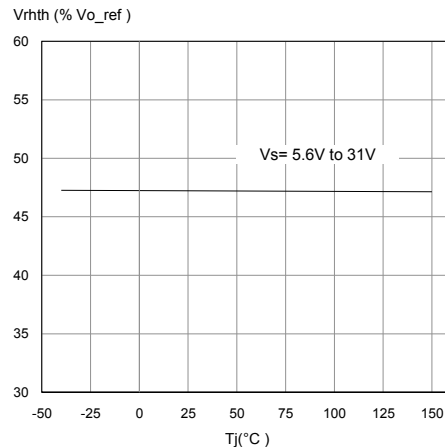


Figure 15. V_{rlth} vs. T_j

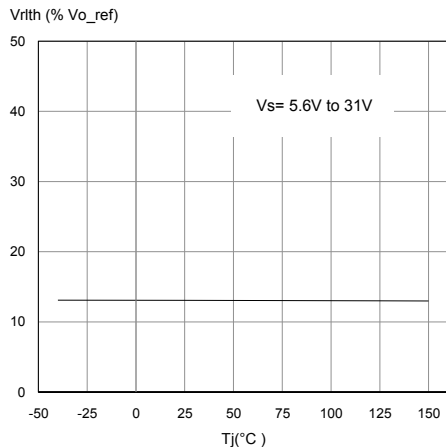


Figure 16. V_{whth} vs. T_j

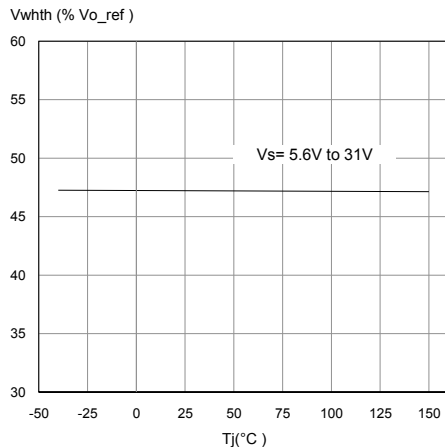


Figure 17. V_{wlth} vs. T_j

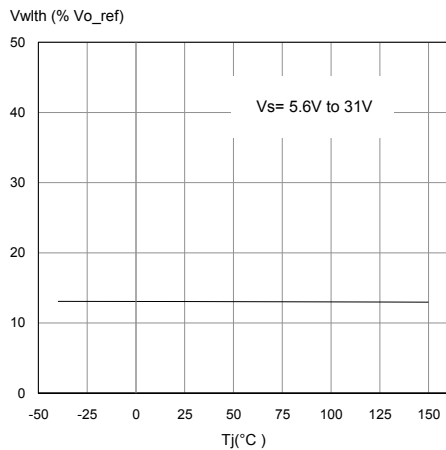


Figure 18. I_{cr} & I_{cwc} vs. T_j

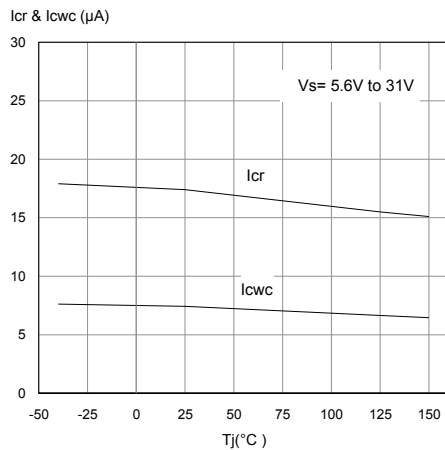


Figure 19. I_{dr} & I_{cwd} vs. T_j

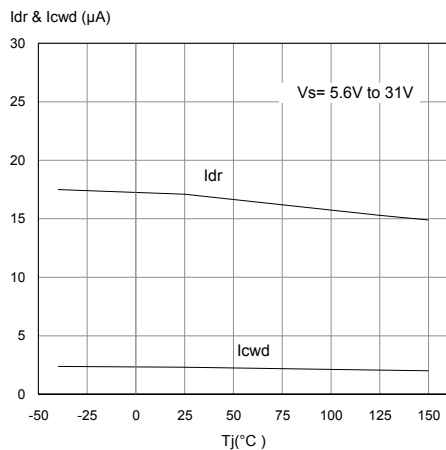


Figure 20. T_{wop} vs. T_j

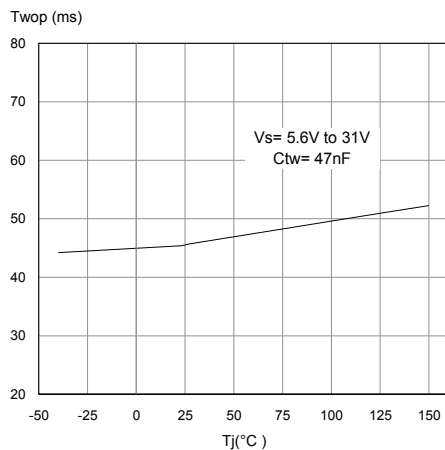
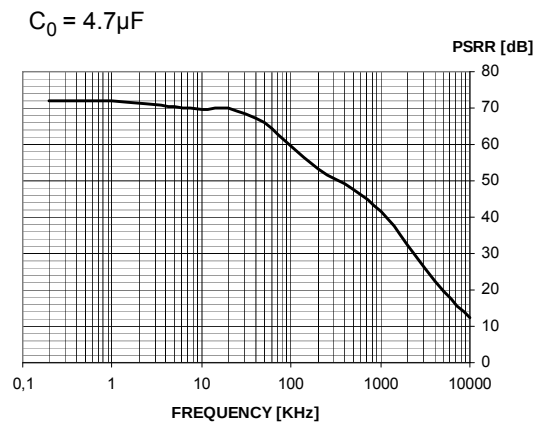


Figure 21. PSRR



2.5 Test circuit and waveforms plot

2.5.1 Load regulation

Figure 22. Load regulation test circuit

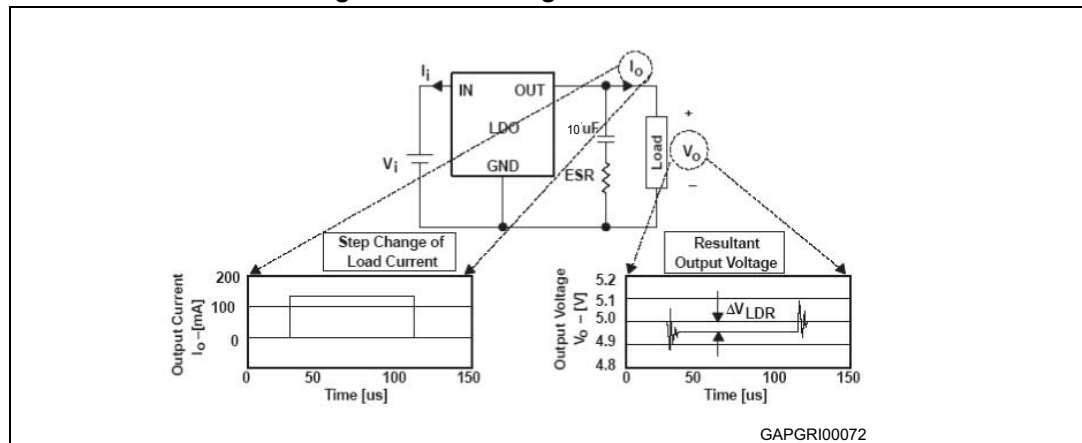
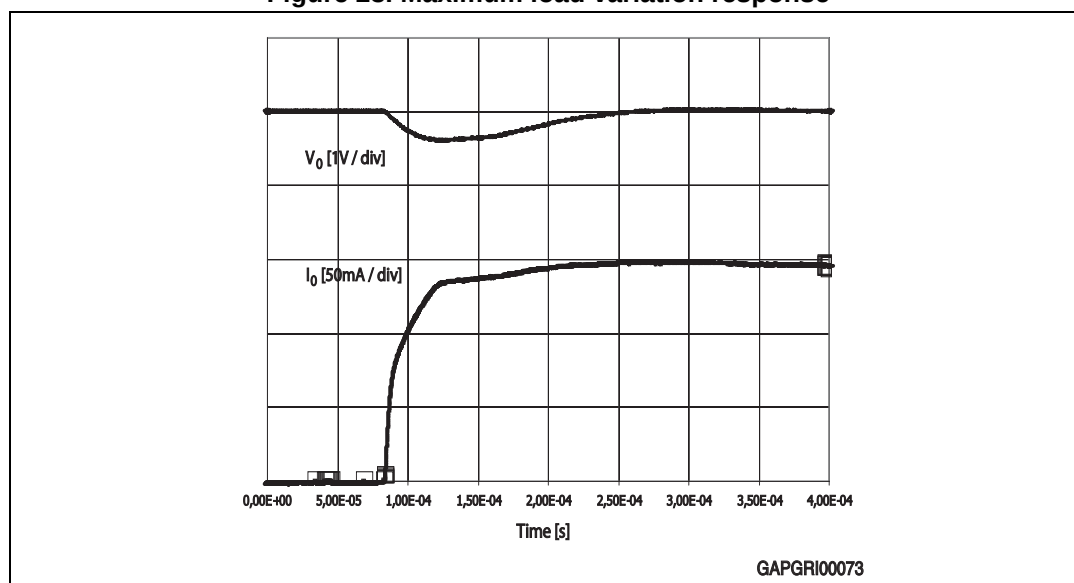
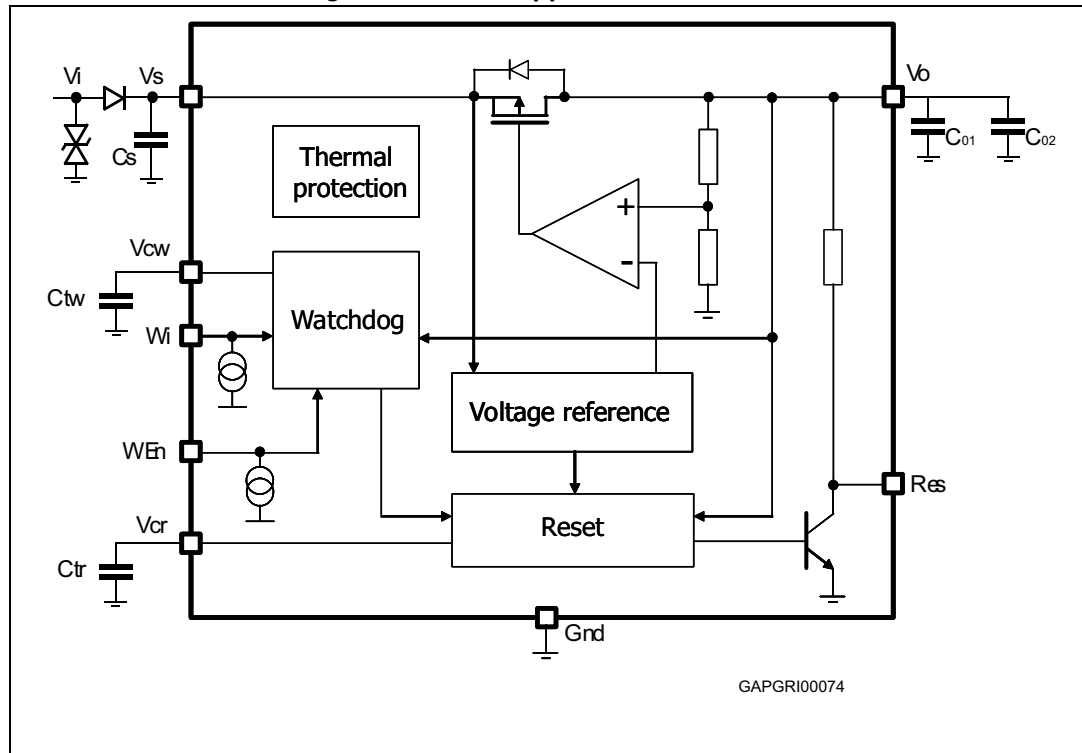


Figure 23. Maximum load variation response



3 Application information

Figure 24. L4993 application schematic

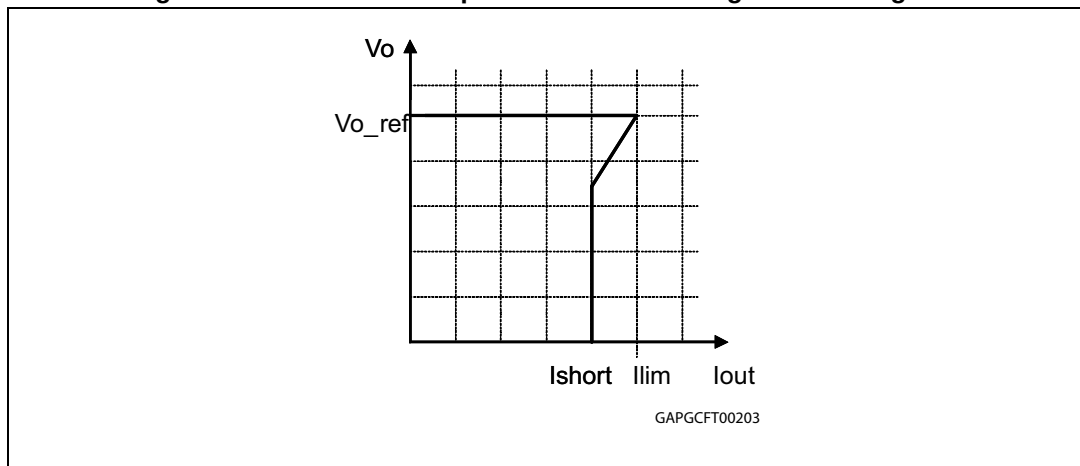


Note: The input capacitor $C_s > 200 \text{ nF}$ is necessary for the smoothing of line disturbances. The output capacitor $C_{01} > 100 \text{ nF}$ is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended put an additional electrolytic capacitor $C_{02} > 10 \text{ }\mu\text{F}$ at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500 mA is obtained. The output voltage is regulated up to transient input supply voltage of 40 V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided. The voltage regulator watchdog functionality can be disabled by putting WEn low.

Figure 25. Behavior of output current versus regulated voltage Vo



3.2 Reset

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then Res goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1 V.

When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

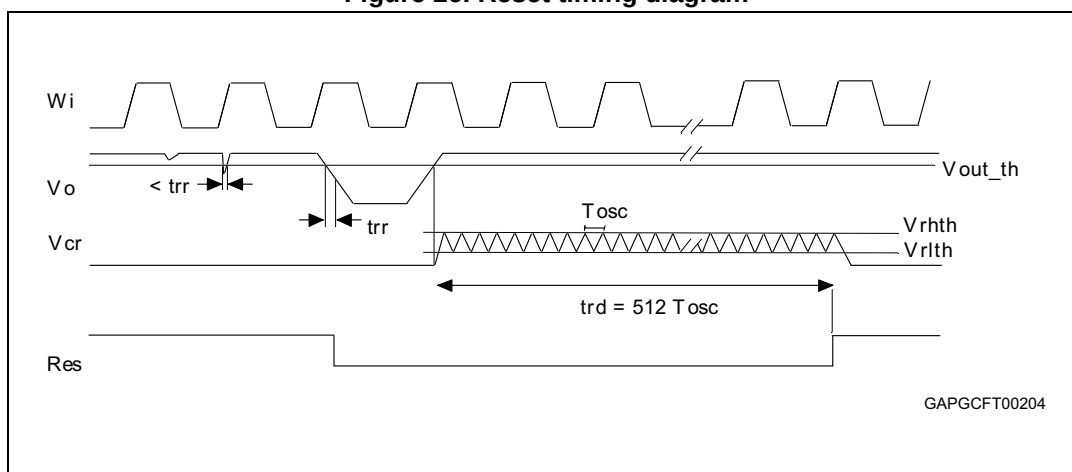
- I_{cr} : is an internally generated charge current
- I_{dr} : is an internally generated discharge current
- V_{rhth} , V_{rlth} : are two voltages defined with the output voltage and a resistor output divider
- C_{tr} : is an external capacitance.

t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

Reset is active when En is high.

Figure 26. Reset timing diagram



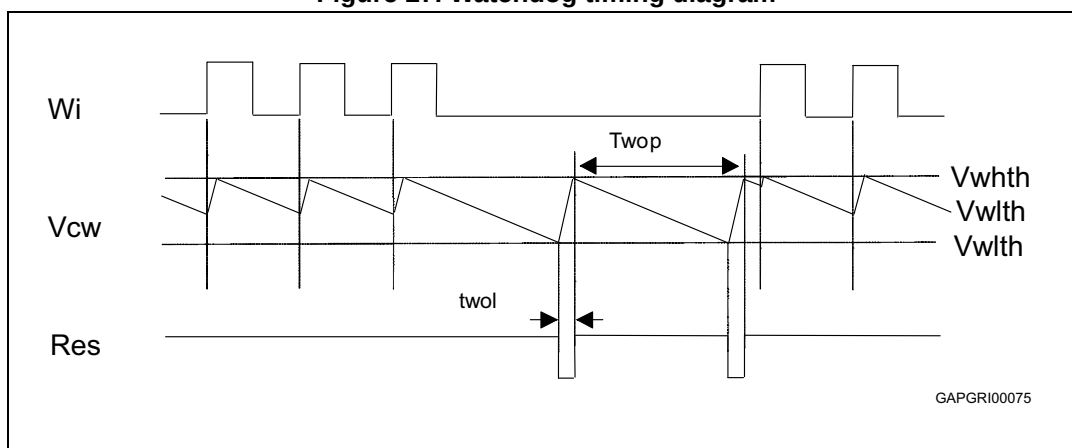
3.3 Watchdog

A connected microcontroller is monitored by the watchdog input Wi. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, Ctw. The watchdog circuit discharges the capacitor Ctw, with the constant current I_{cwd}. If the lower threshold V_{lwth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{lwth}. In order to calculate the minimum time t, during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth} - V_{lwth}) \times C_{tw} = I_{cwd} \times t$$

Every Wi positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth}, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor Ctw.

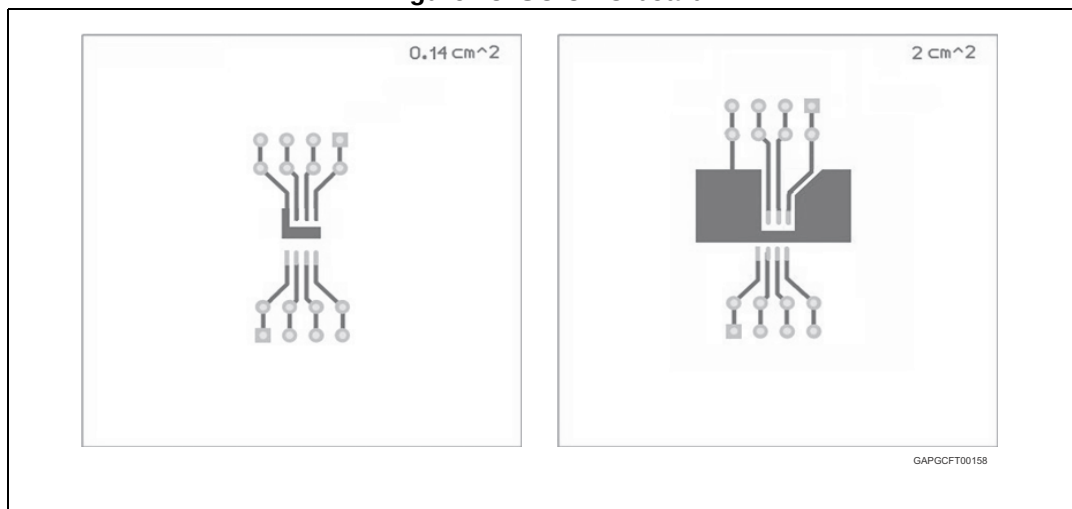
Figure 27. Watchdog timing diagram



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 28. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad lay-out to 2 cm²).

Figure 29. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

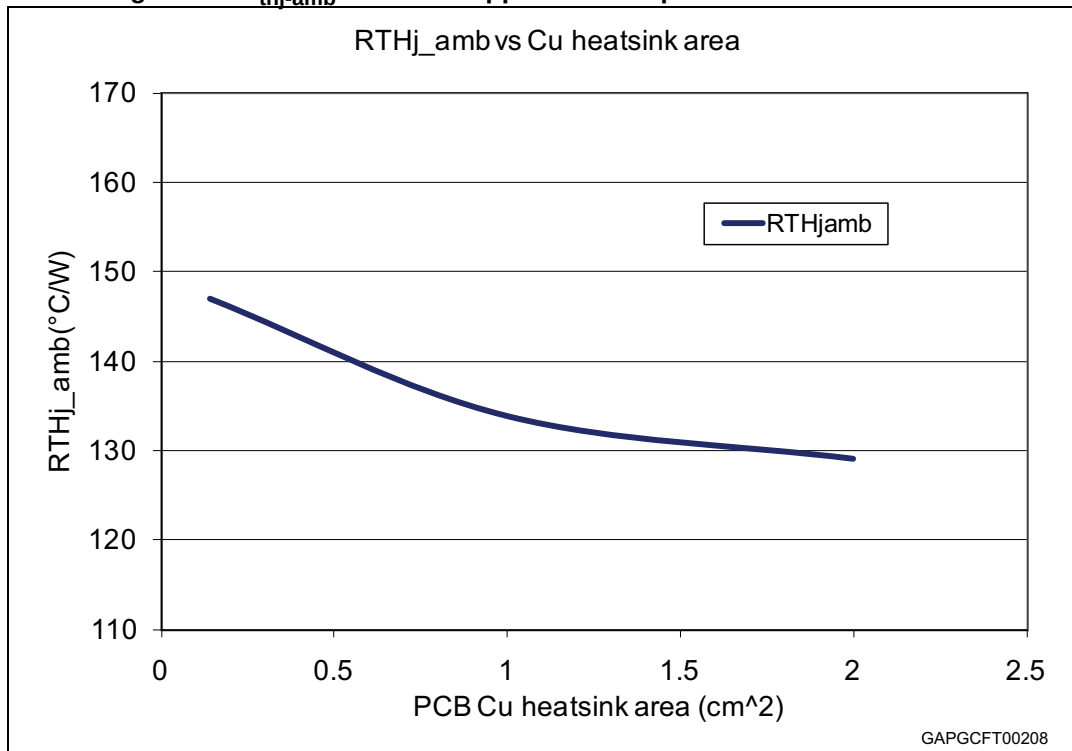
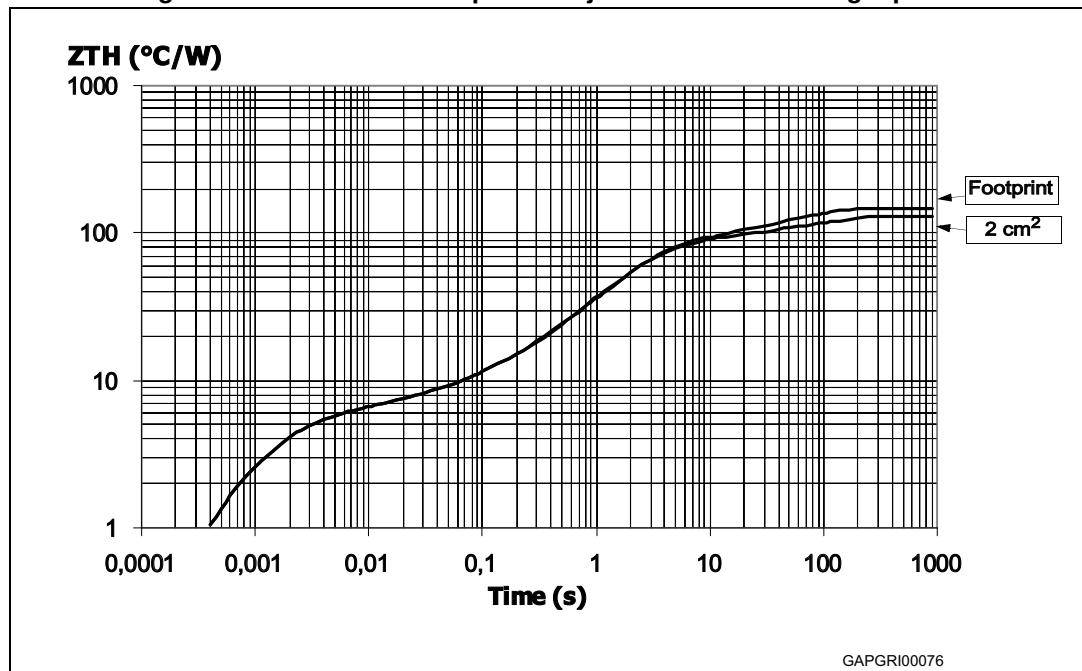


Figure 30. SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31. Thermal fitting model of Vreg in SO-8

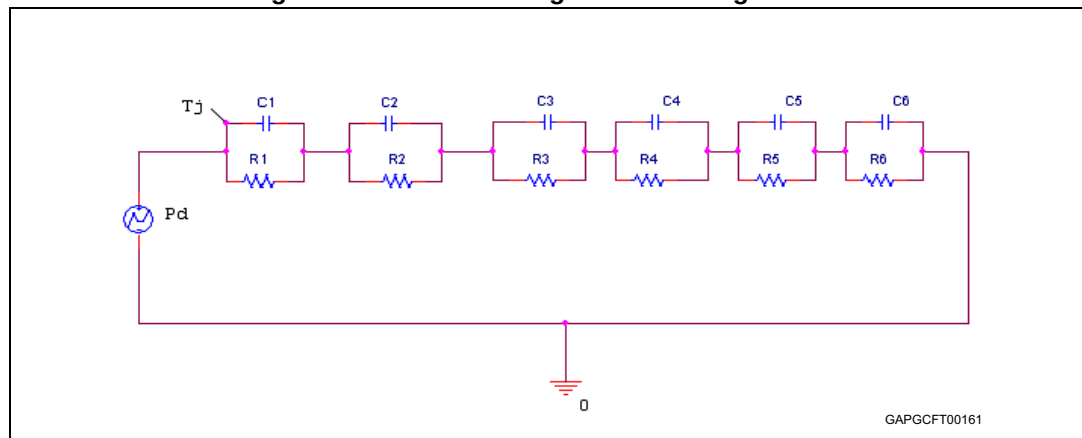
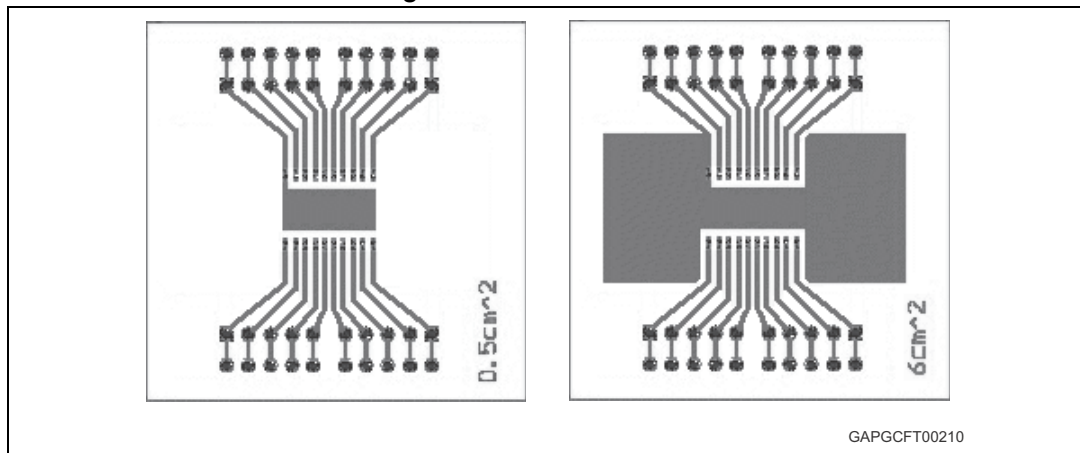


Table 9. SO-8 thermal parameter

Area/island (cm ²)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

4.2 SO-20 thermal data

Figure 32. SO-20 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2 mm, Cu thickness=35 μ m, Copper areas: from minimum pad lay-out to 6 cm²).

Figure 33. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

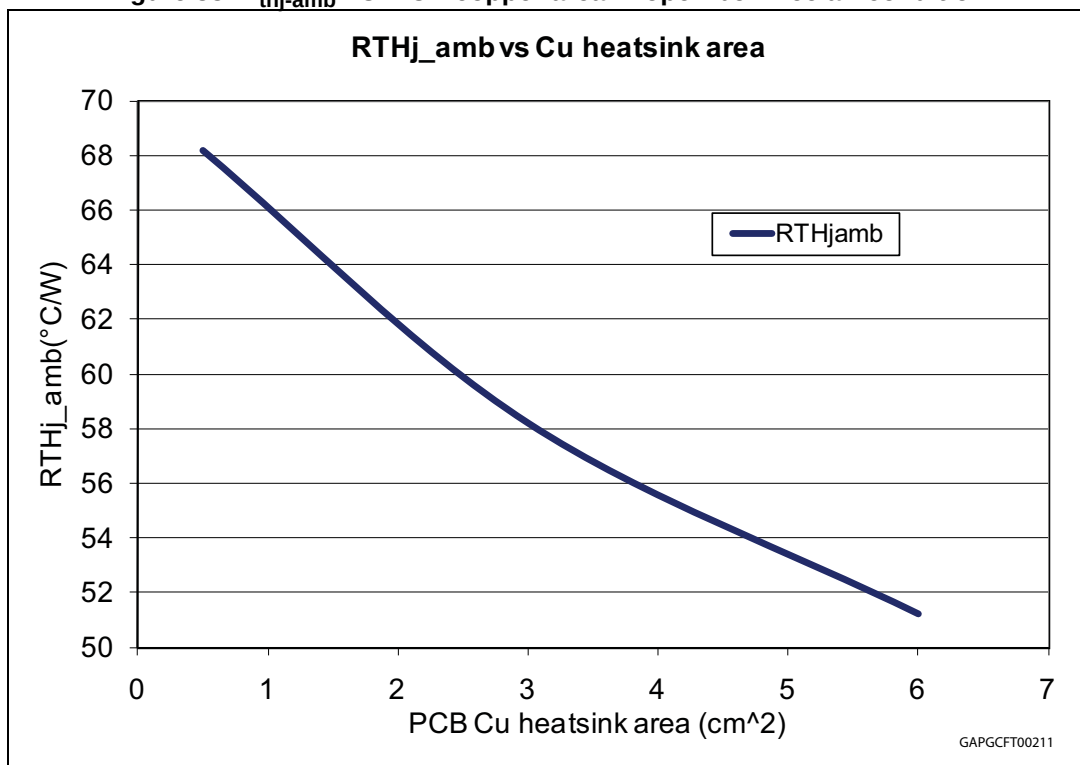
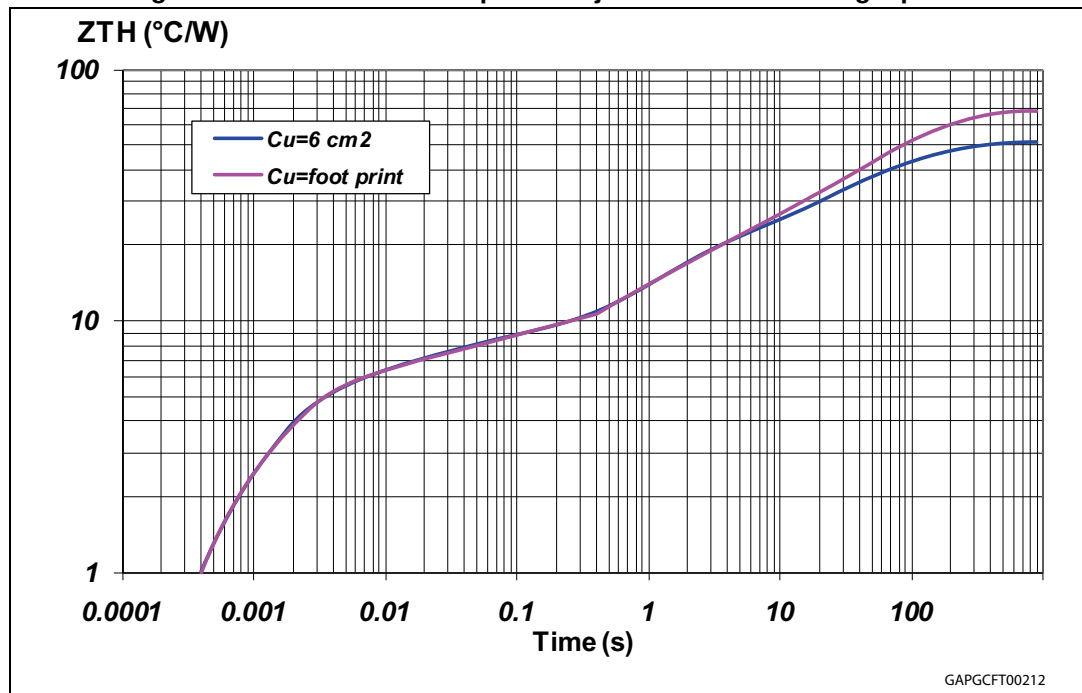


Figure 34. SO-20 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. Thermal fitting model of Vreg in SO-20

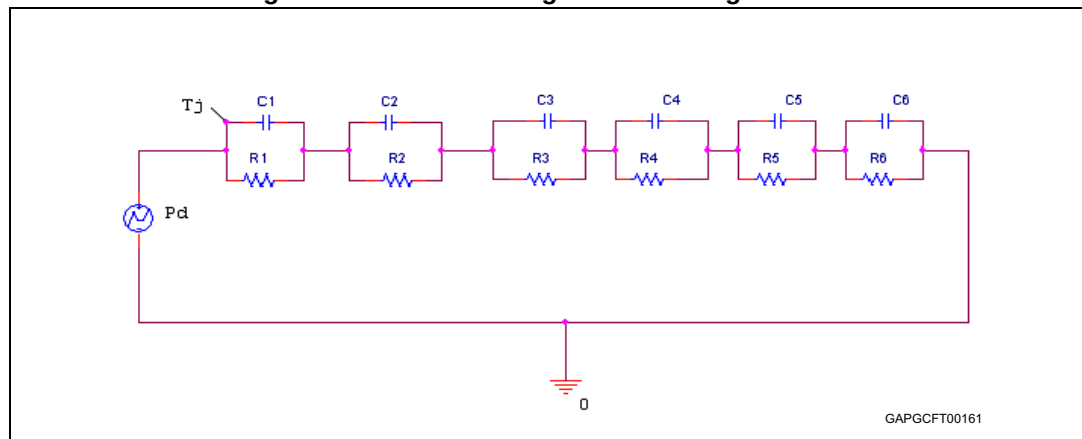


Table 10. SO-20 thermal parameter

Area/island (cm ²)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SO-8 package information

Figure 36. SO-8 package dimensions

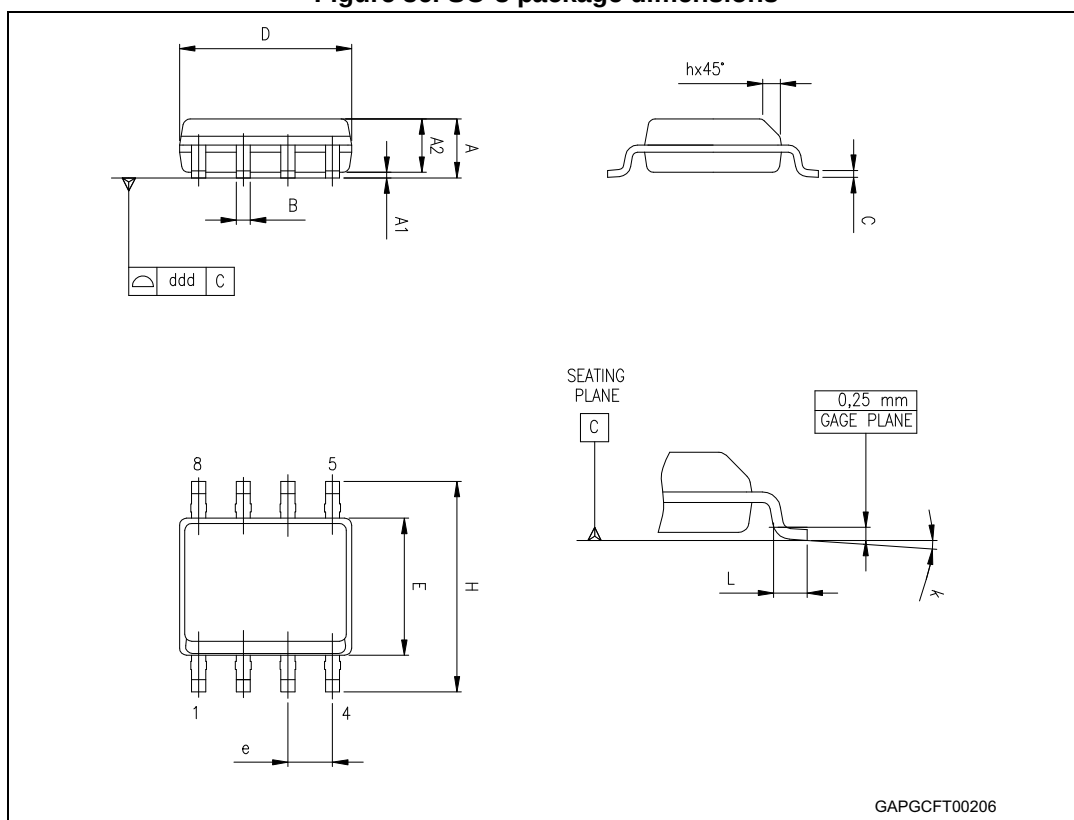


Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48

Table 11. SO-8 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.3 SO-20 package information

Figure 37. SO-20 package dimensions

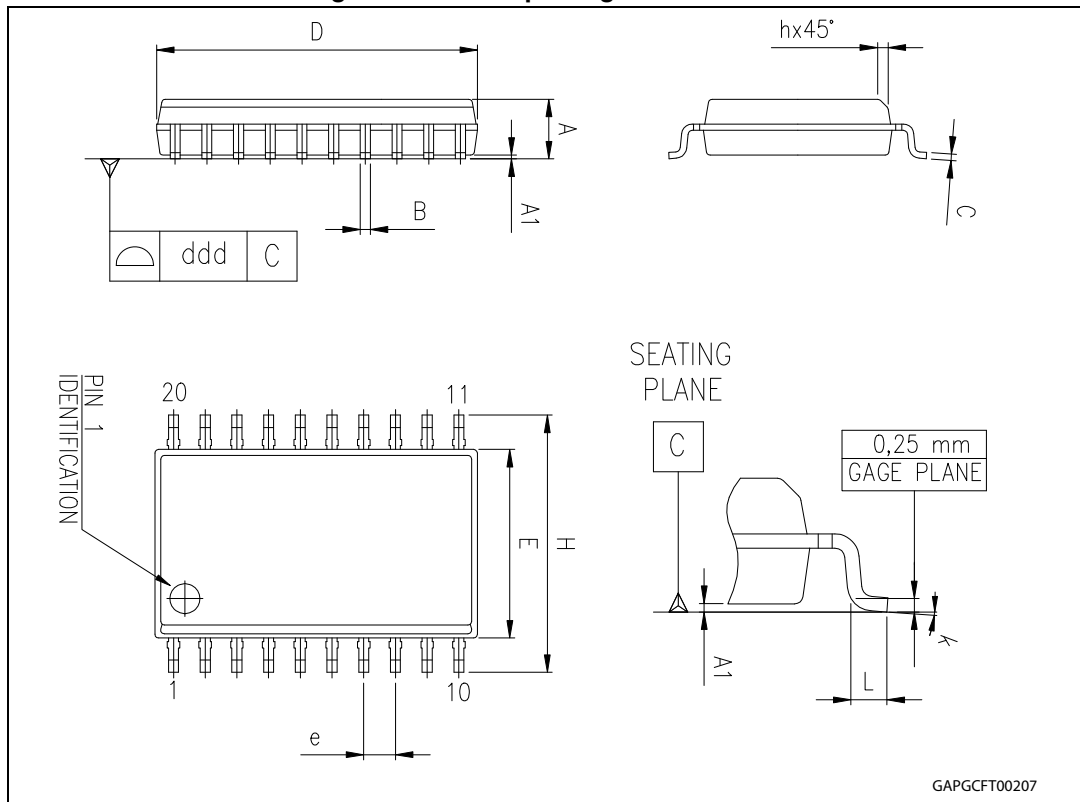


Table 12. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D ⁽¹⁾	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27

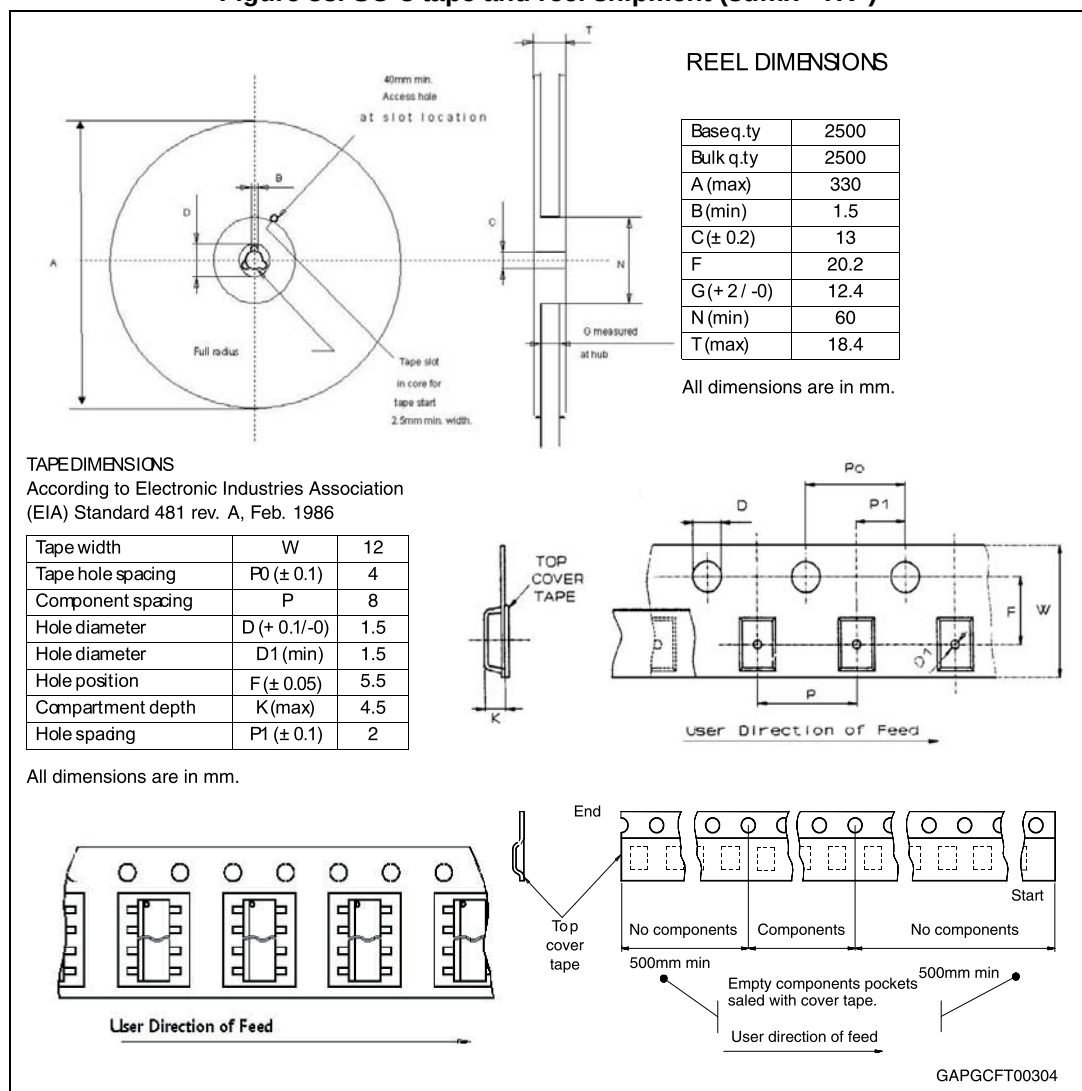
Table 12. SO-20 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
k	0°		8°
ddd			0.10

1. "D" dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

5.4 SO-8 packing information

Figure 38. SO-8 tape and reel shipment (suffix "TR")



5.5 SO-20 packing information

Figure 39. SO-20 tube shipment (no suffix)

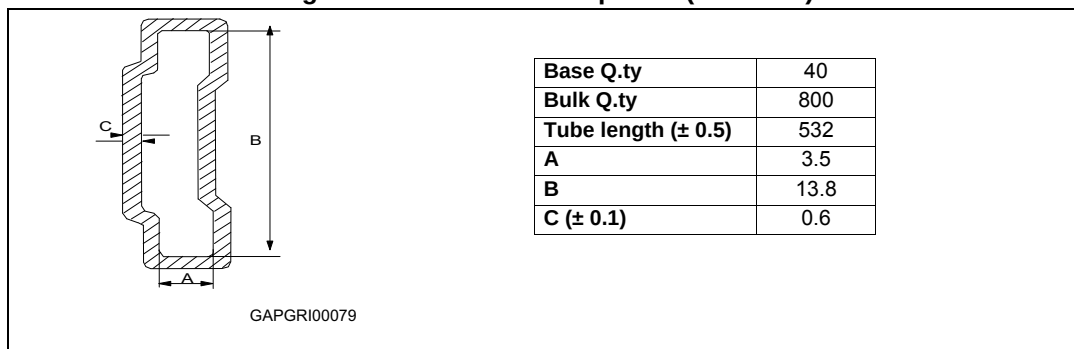
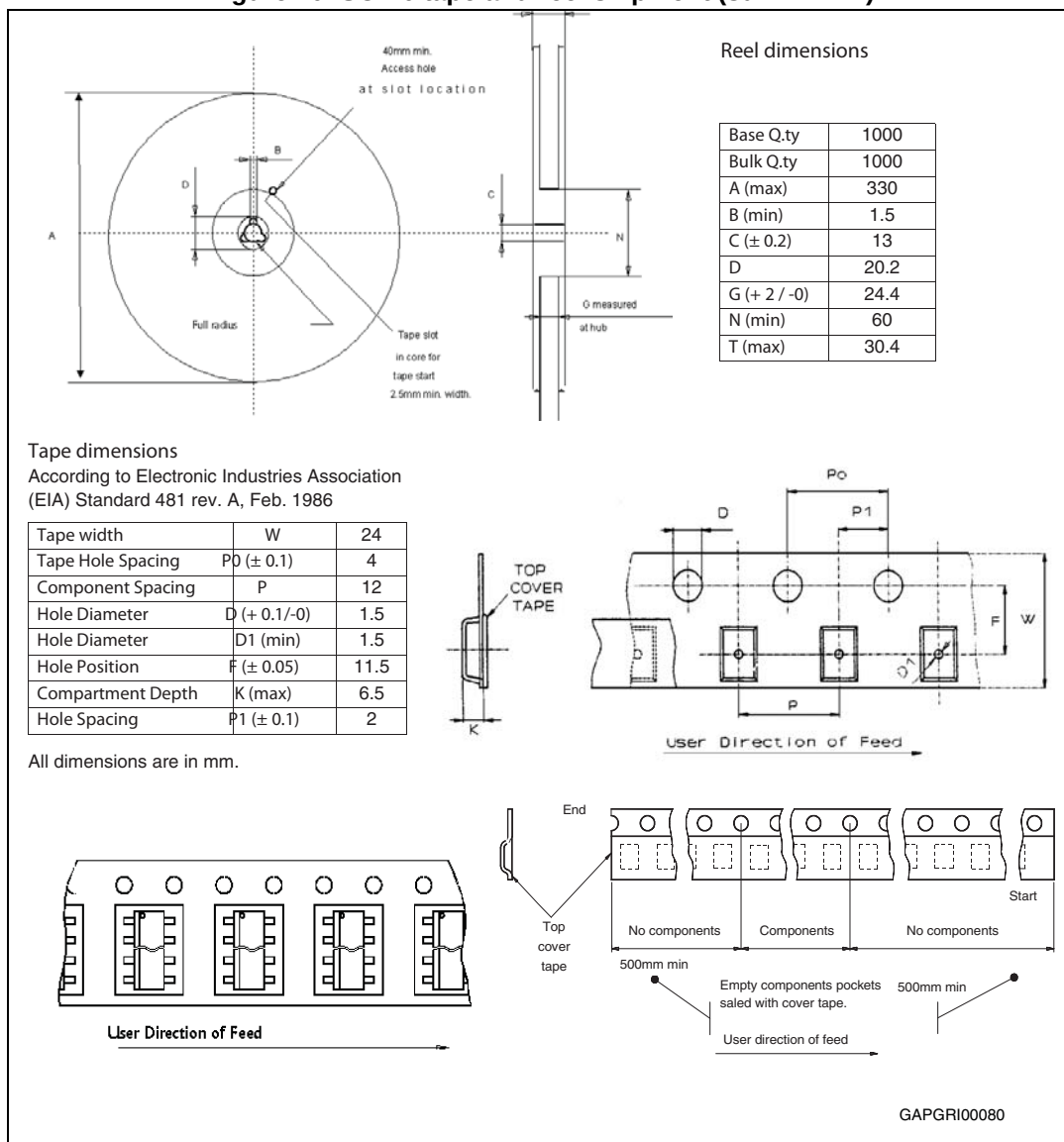


Figure 40. SO-20 tape and reel shipment (suffix "TR")



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
June-2004	1	Initial release.
18-Jan-2007	2	Updated Table 5 , 6 , 7 and 8 .
01-Jun-2007	3	Document put in corporate technical literature template. Updated Table 4 .
22-Aug-2007	4	Table 5: General : updated I_{short} , I_{lim} , I_q , T_{rr2} , V_{th_hist} parameters.
29-Aug-2007	5	Added list of tables and figures. Added Section 4: Package and PCB thermal data .
08-Apr-2008	6	Document restructured. Changed Figure 1: Block diagram . Updated Table 5: General : – changed I_{short} max value from 4000 mA to 400 mA – changed I_{qn_150} typ. value from 1.45 mA to 1.25 mA – changed I_{qn_50} typ. value from 538 μA to 470 μA – changed I_{qn_1} typ. value from 120 μA to 100 μA. Updated Table 6: Reset : – corrected trd formula. Updated Table 7: Watchdog : – changed V_{wlth} values in V_{o_ref} percentages – changed V_{whth} values in V_{o_ref} percentages. Added Figure 24: L4993 application schematic . Added Section 2.4: Electrical characteristics curves . Added Section 2.5: Test circuit and waveforms plot .
09-Mar-2012	7	Updated Table 3: Absolute maximum ratings .
20-Sep-2013	8	Updated disclaimer.
01-Mar-2018	9	Updated template. Removed the tube version on the SO-8 package on the Table 1: Device summary . Updated Section 2.1: Absolute maximum ratings . Removed Figure “SO-8 tube shipment (no suffix)”.
19-Sep-2018	10	Typo errors.

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