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MOS FIELD EFFECT POWER TRANSISTOR 2SK1499/2SK1500

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK1499/2SK1500 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- **Low On-state Resistance**
 $R_{DS(on)} \leq 0.25 \text{ } \Omega / 0.27 \text{ } \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 13 \text{ A}$)
- **Low C_{iss}** $C_{iss} = 3 \text{ } 300 \text{ pF TYP.}$
- **Built-in G-S Gate Protection Diode**
- **High Avalanche Capability Ratings**

QUALITY GRADE

Standard

Please refer to “Quality grade on NEC Semiconductor Devices” (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

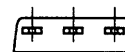
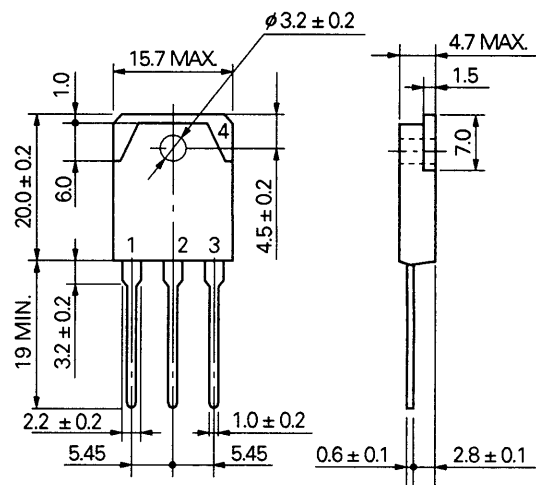
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V _{DSS}	450/500	V
		(2SK1499/2SK1500)	
Gate to Source Voltage	V _{GSS}	±30	V
Drain Current (DC)	I _{D(DC)}	±25	A
Drain Current (pulse)	I _{D(pulse)*}	±100	A
Total Power Dissipation (T _c = 25 °C)	P _T	160	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current	I _{AS**}	37.5	A
Single Avalanche Energy	E _{AS**}	907	mJ

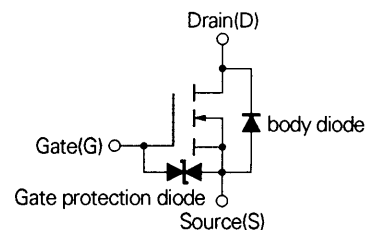
* PW $\leq 10 \mu\text{s}$, Duty Cycle $\leq 2 \%$

**** Starting $T_{ch} = 25\text{ }^{\circ}\text{C}$, $R_G = 25\text{ }\Omega$, $V_{GS} = 20\text{ V} \rightarrow 0$**

PACKAGE DIMENSIONS (in millimeters)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

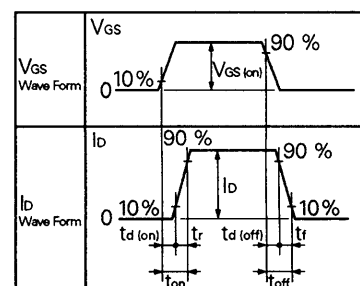
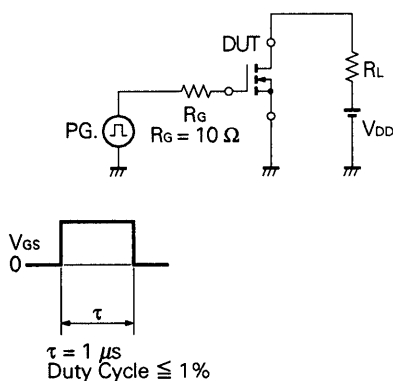
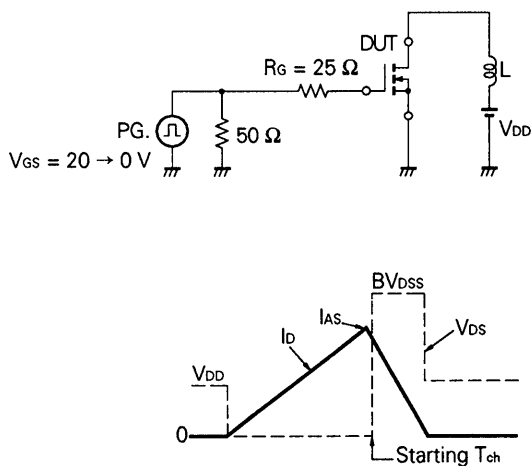


ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

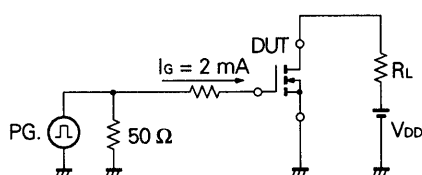
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1499)	$R_{DS(on)}$		0.20	0.25	Ω	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}$
Drain to Source On-state Resistance (2SK1500)	$R_{DS(on)}$		0.22	0.27	Ω	
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	8.0			S	$V_{DS} = 10\text{ V}, I_D = 13\text{ A}$
Drain Leakage Current (2SK1499)	I_{DSS}			100	μA	$V_{DS} = 450\text{ V}, V_{GS} = 0$
Drain Leakage Current (2SK1500)	I_{DSS}			100	μA	$V_{DS} = 500\text{ V}, V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0$
Input Capacitance	C_{iss}		3 300		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		1 100		pF	
Reverse Transfer Capacitance	C_{rss}		480		pF	
Turn-On Delay Time	$t_{d(on)}$		50		ns	$V_{GS} = 10\text{ V}$ $V_{DD} = 150\text{ V}$ $I_D = 13\text{ A}, R_G = 10\text{ }\Omega$ $R_L = 11.5\text{ }\Omega$
Rise Time	t_r		130		ns	
Turn-Off Delay Time	$t_{d(off)}$		180		ns	
Fall Time	t_f		70		ns	
Total Gate Charge	Q_G		115		nC	$V_{GS} = 10\text{ V}$ $I_D = 25\text{ A}$ $V_{DD} = 400\text{ V}$
Gate to Source Charge	Q_{GS}		20		nC	
Gate to Drain Charge	Q_{GD}		70		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	$I_D = 25\text{ A}, V_{GS} = 0$
Reverse Recovery Time	t_{rr}		670		ns	$I_D = 25\text{ A}, V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		7.0		μC	

Test Circuit 1: Avalanche Capability

Test Circuit 2: Switching Time

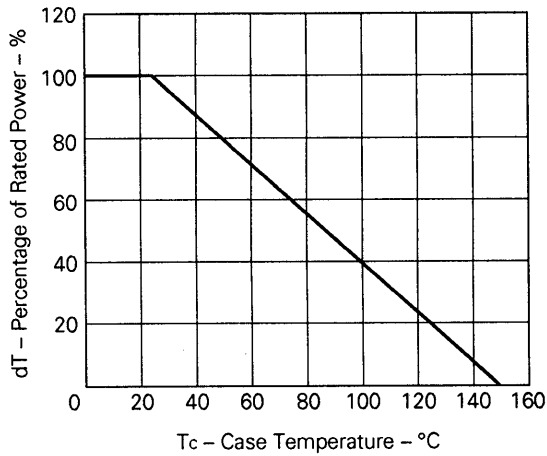


Test Circuit 3: Gate Charge

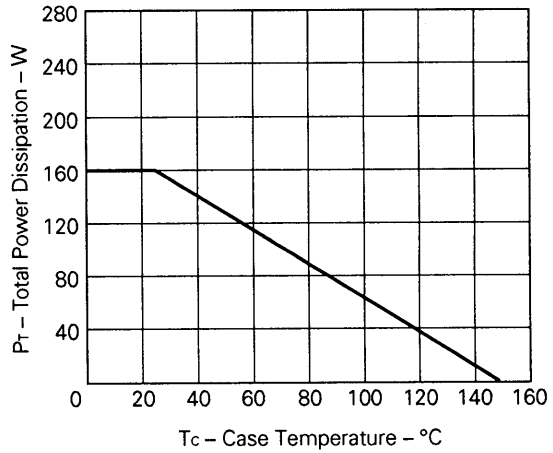


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

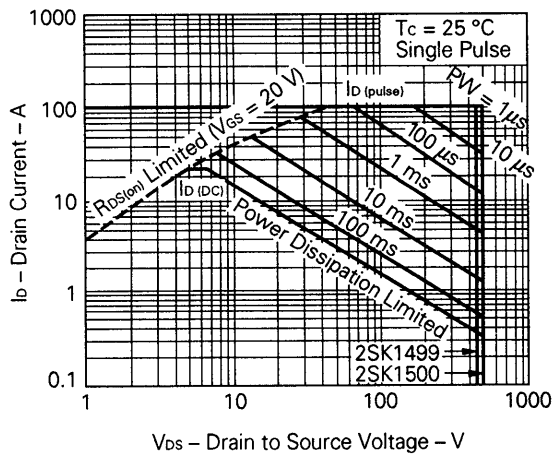
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



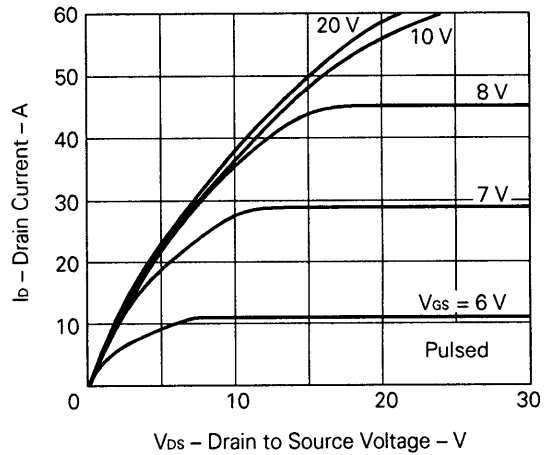
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



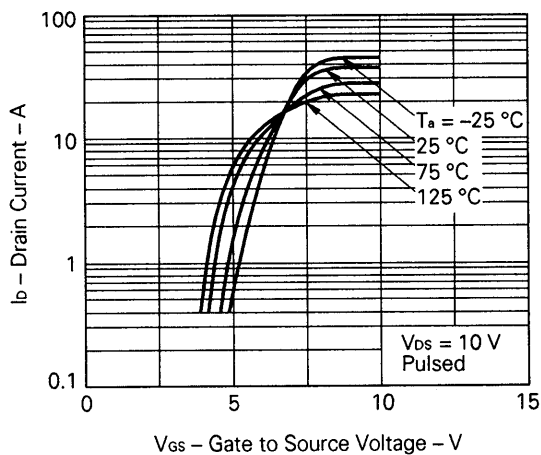
FORWARD BIAS SAFE OPERATING AREA



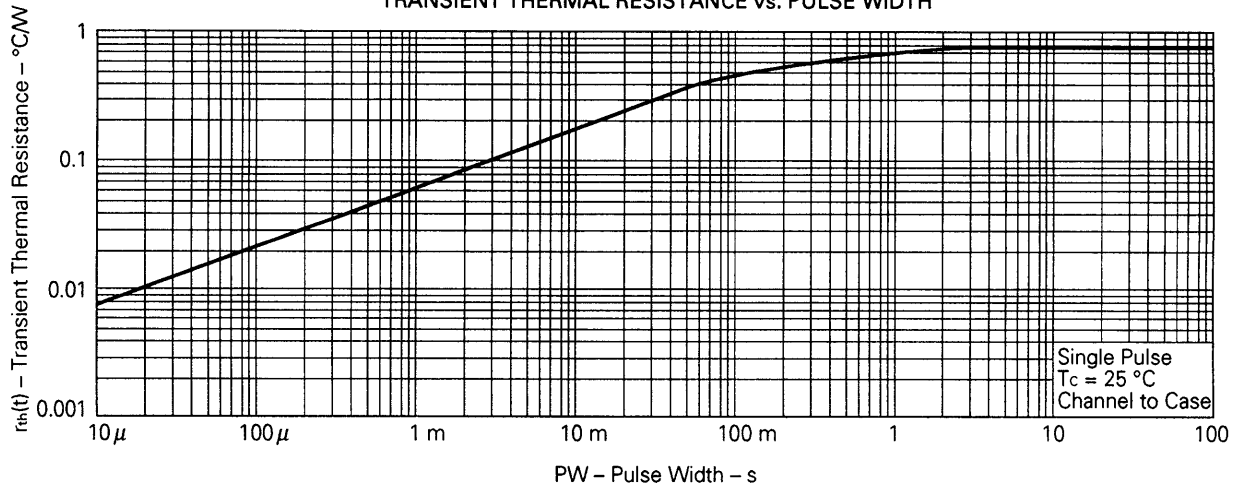
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



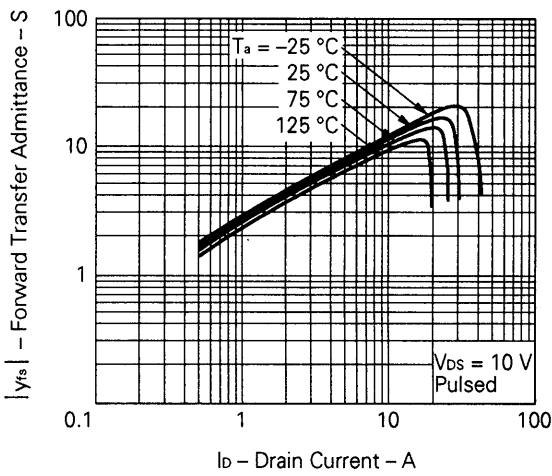
TRANSFER CHARACTERISTICS



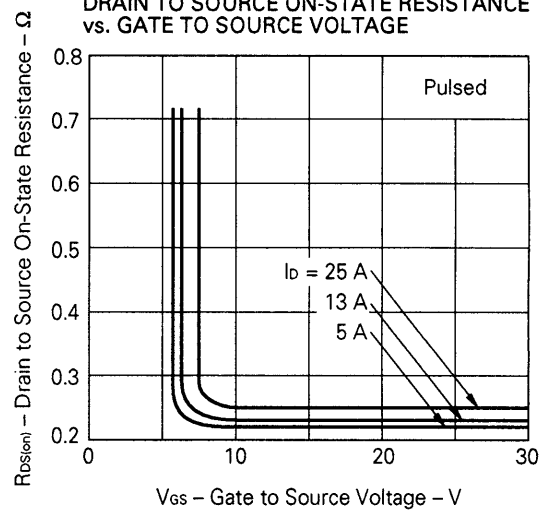
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



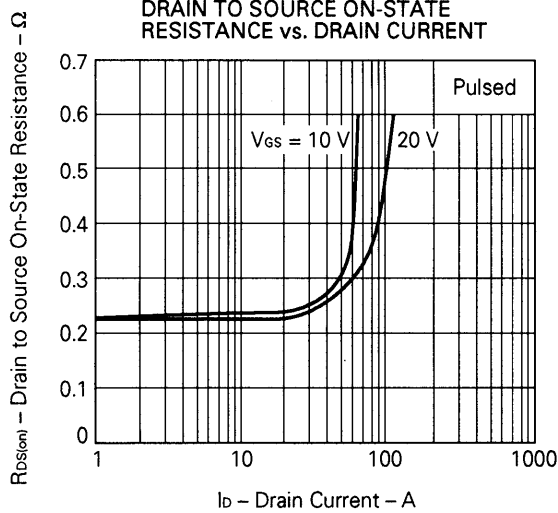
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



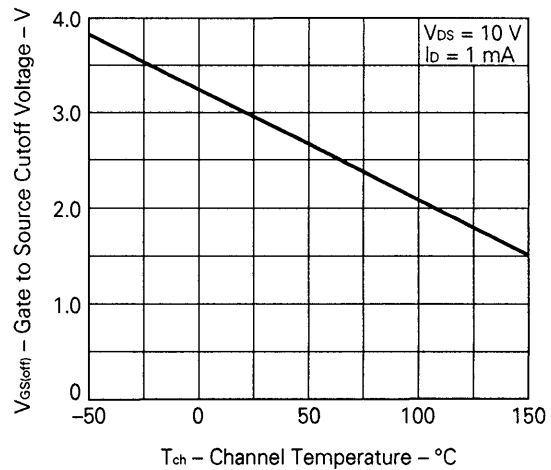
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

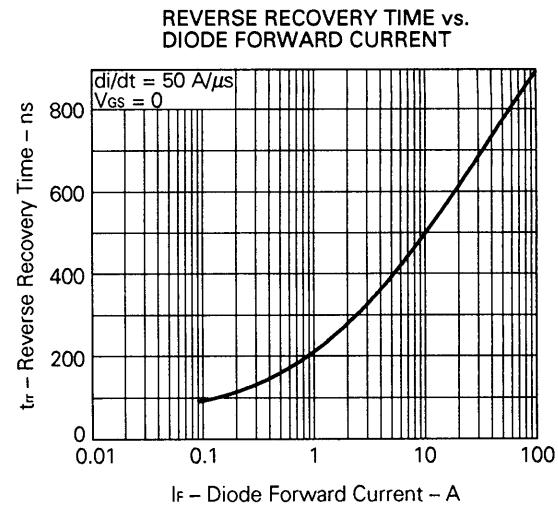
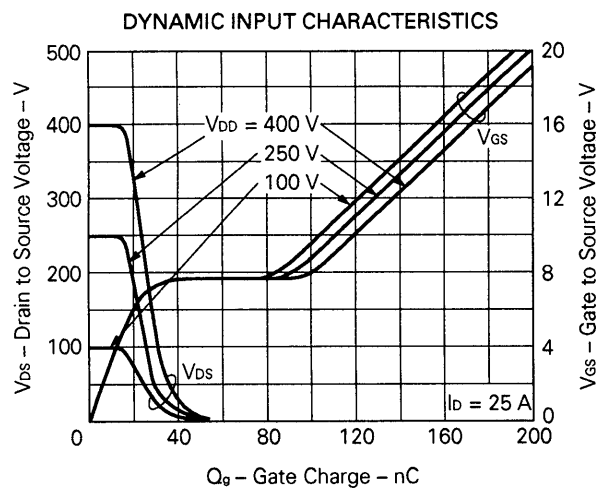
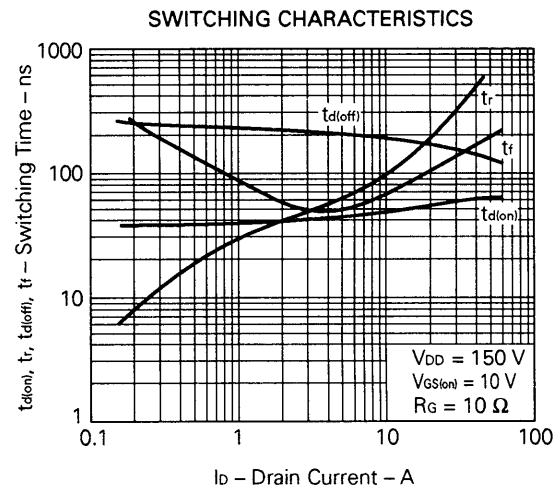
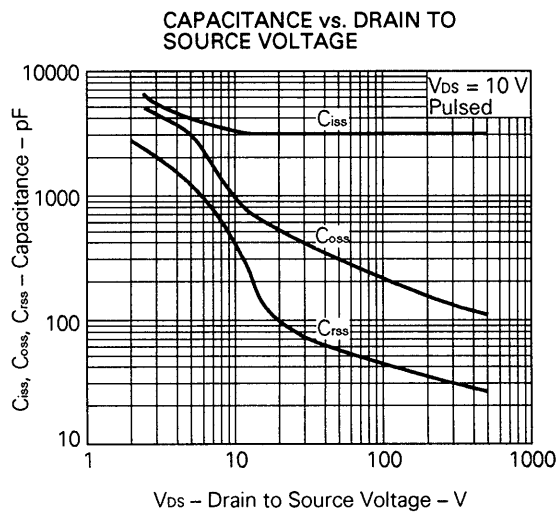
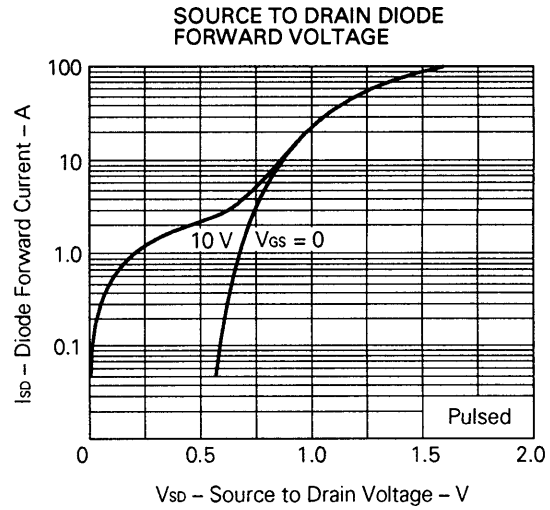
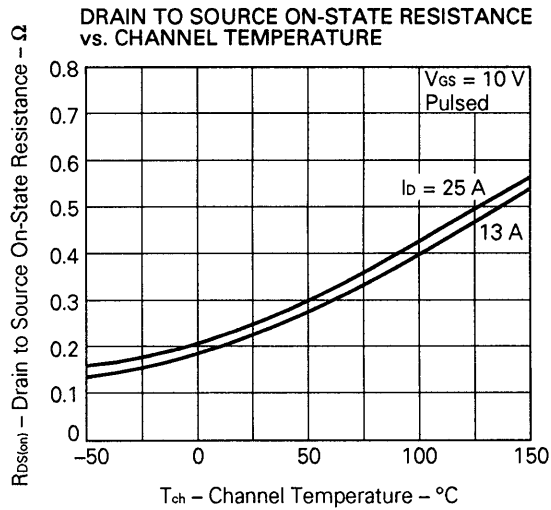


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

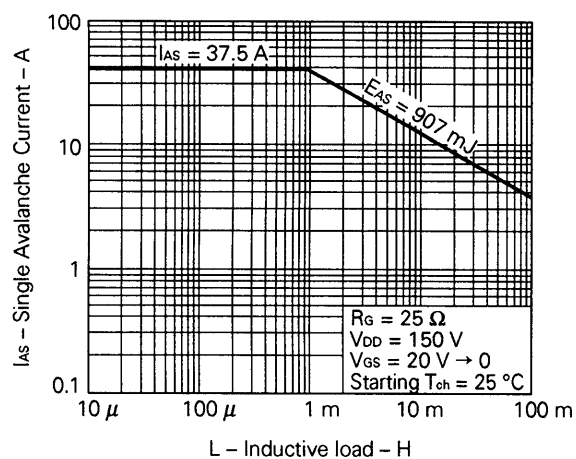


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

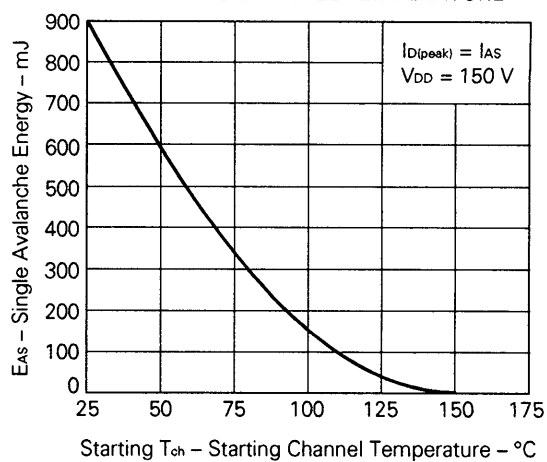




SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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