

HD74HC73

Dual J-K Flip-Flops (with Clear)

REJ03D0548-0200
(Previous ADE-205-420)
Rev.2.00
Oct 06, 2005

Description

The flip-flop is edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each flip-flop has independent, J, K, clock, and clear inputs and Q and $\bar{Q}$ outputs. Clear is independent of the clock and accomplished by a low level on the input.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 18 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC73P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74HC73FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74HC73RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

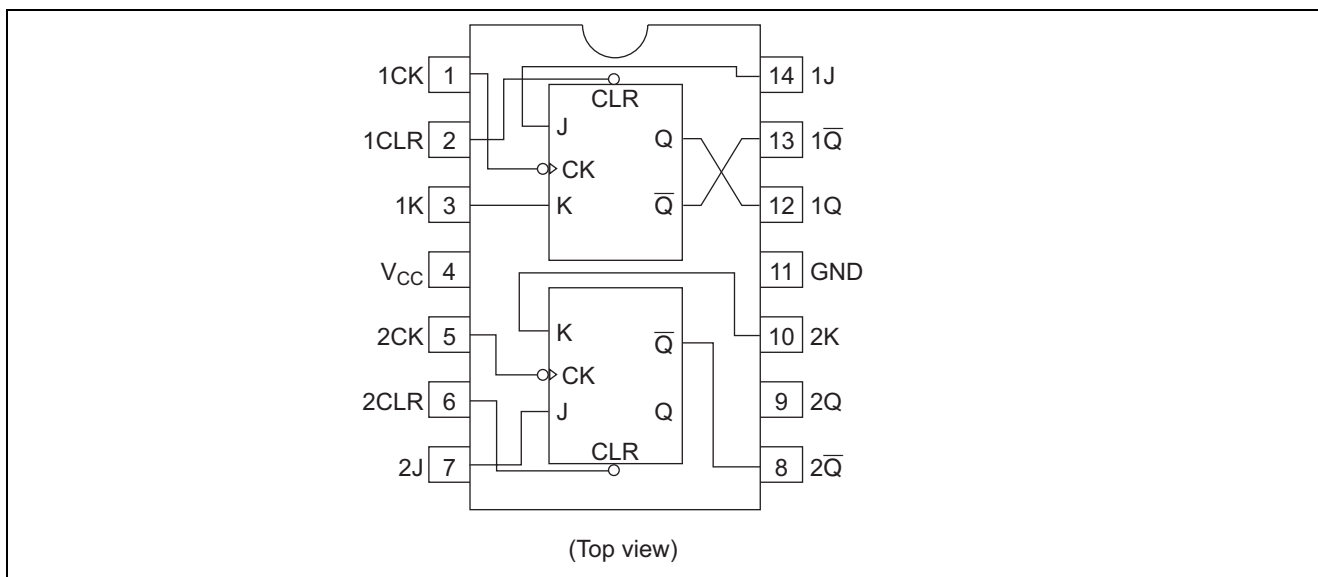
Note: Please consult the sales office for the above package availability.

Function Table

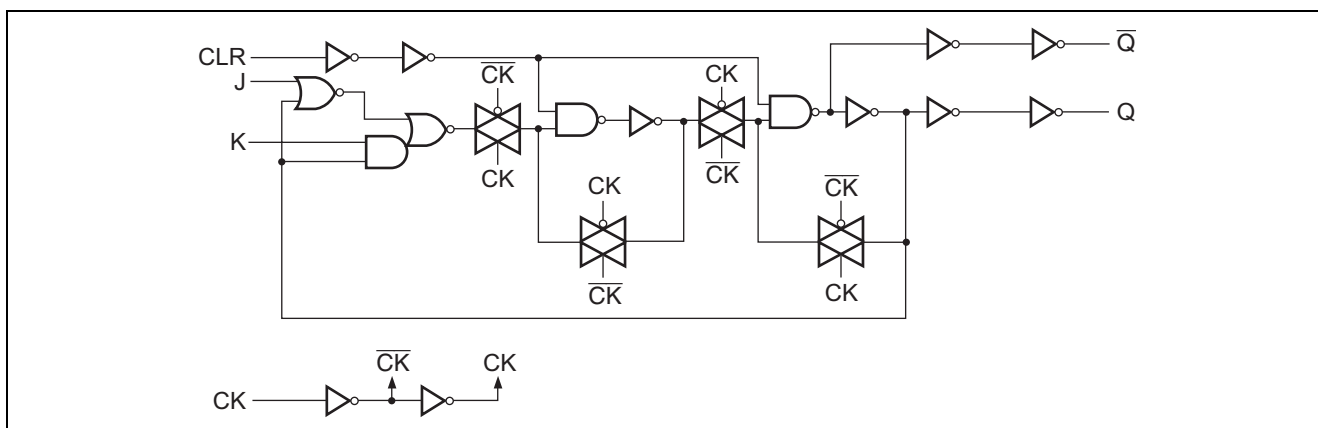
Inputs				Outputs	
Clear	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H		L	L	No change	
H		L	H	L	H
H		H	L	H	L
L		H	H	Toggle	
H	L	X	X	No change	
H	H	X	X	No change	
H		X	X	No change	

H : High level
L : Low level
X : Irrelevant

Pin Arrangement



Logic Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{in}, V_{out}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

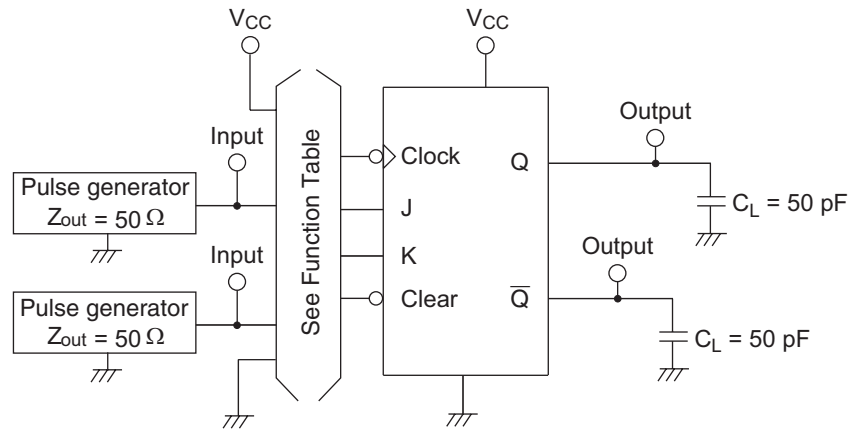
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA
		4.5	4.4	4.5	—	4.4	—	I _{OH} = -4 mA		
		6.0	5.9	6.0	—	5.9	—	I _{OH} = -5.2 mA		
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA		
		6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA		
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	2.0	—	20	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

Switching Characteristics ($C_L = 50\text{ pF}$, Input $t_r = t_f = 6\text{ ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz		
		4.5	—	—	30	—	24			
		6.0	—	—	35	—	28			
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	150	—	190	ns	Clock to Q or $\bar{Q}$	
		4.5	—	18	30	—	38			
		6.0	—	—	26	—	33			
		2.0	—	—	140	—	175	ns	Clear to Q or $\bar{Q}$	
		4.5	—	18	28	—	35			
		6.0	—	—	24	—	30			
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, Clear	
		4.5	16	8	—	20	—			
		6.0	14	—	—	17	—			

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

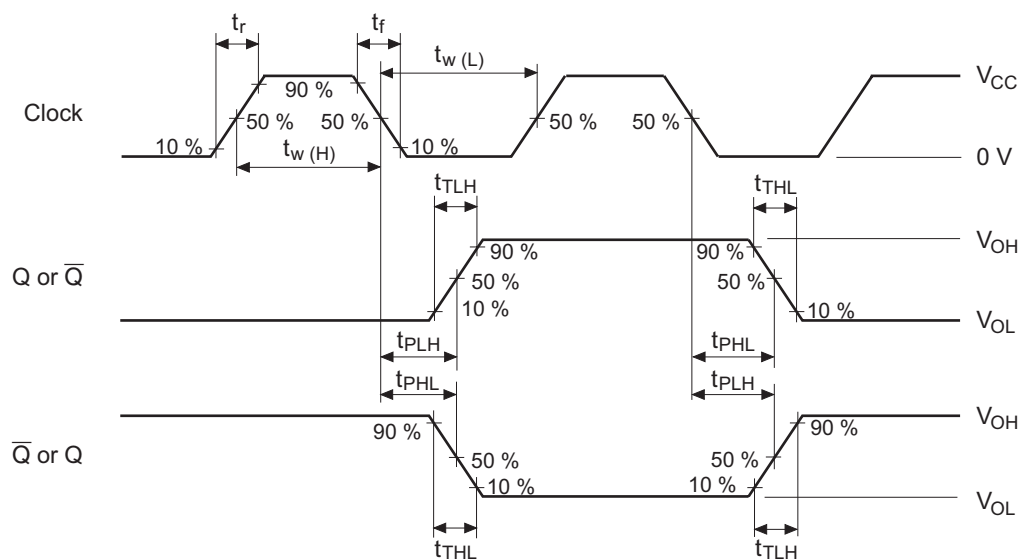
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to clock
		4.5	20	3	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to data
		4.5	5	-2	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	Clear to clock
		4.5	20	-3	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Test Circuit

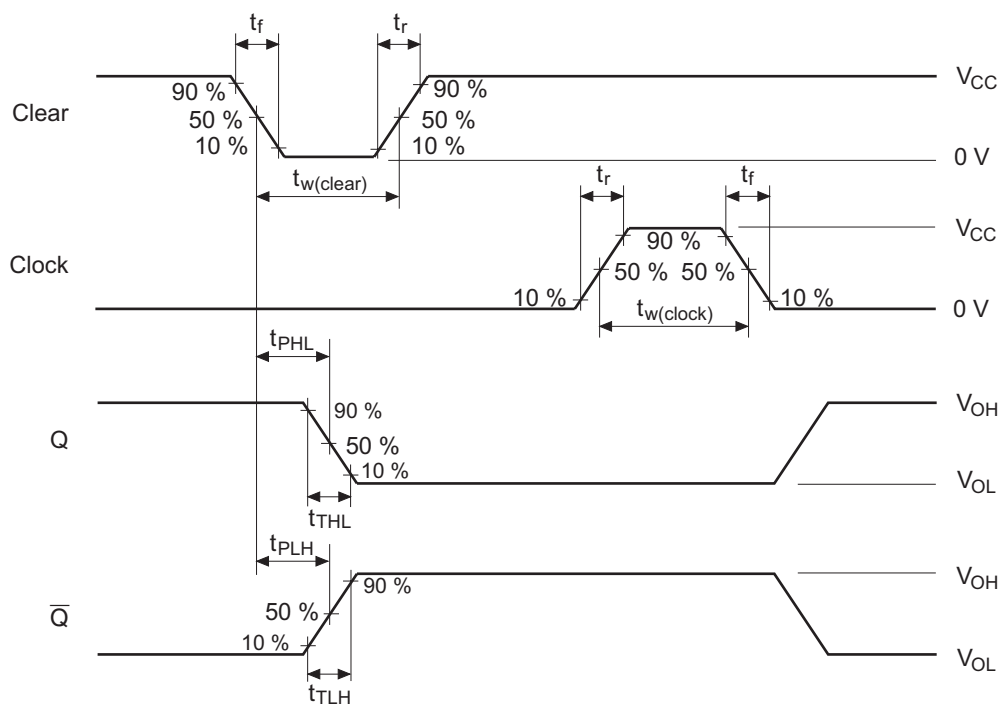
Note: C_L includes the probe and jig capacitance.

Waveforms

• Waveform – 1

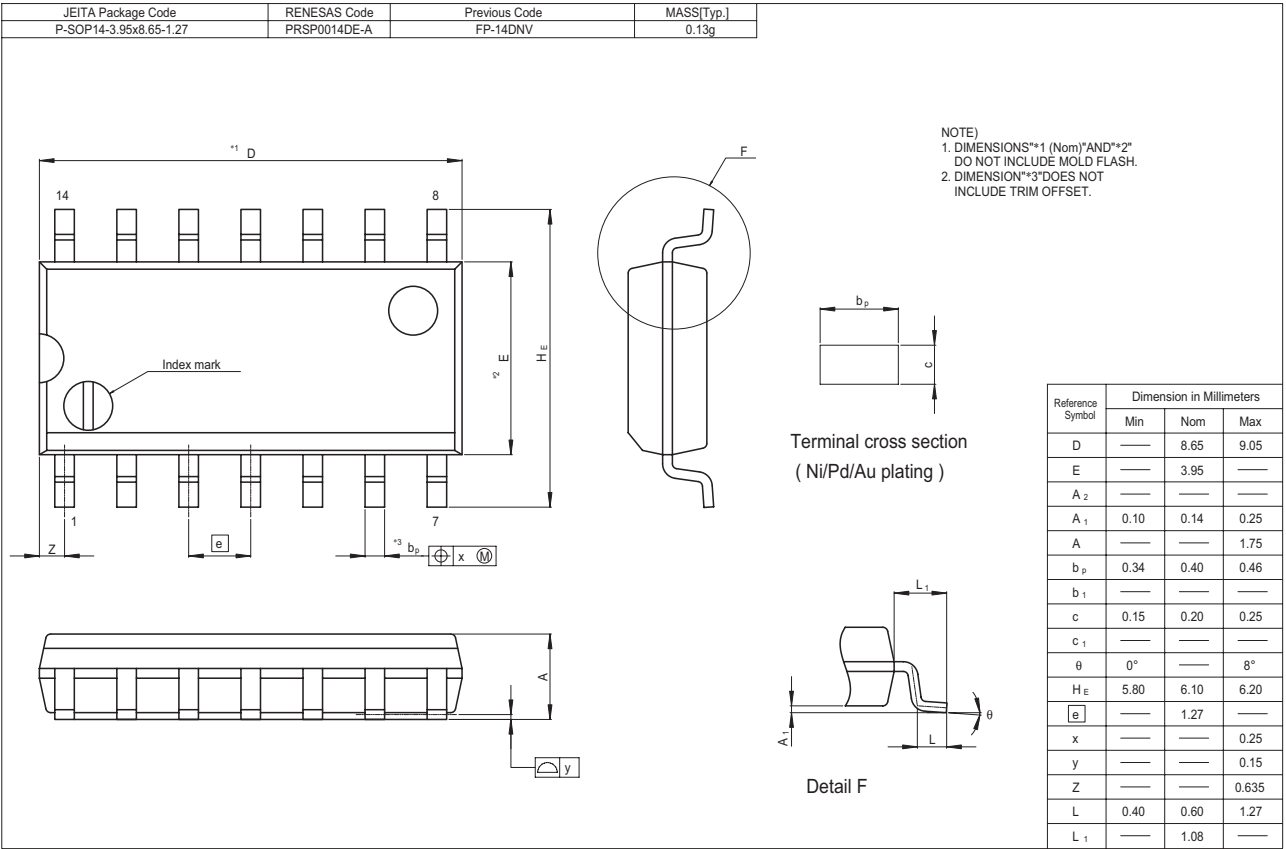
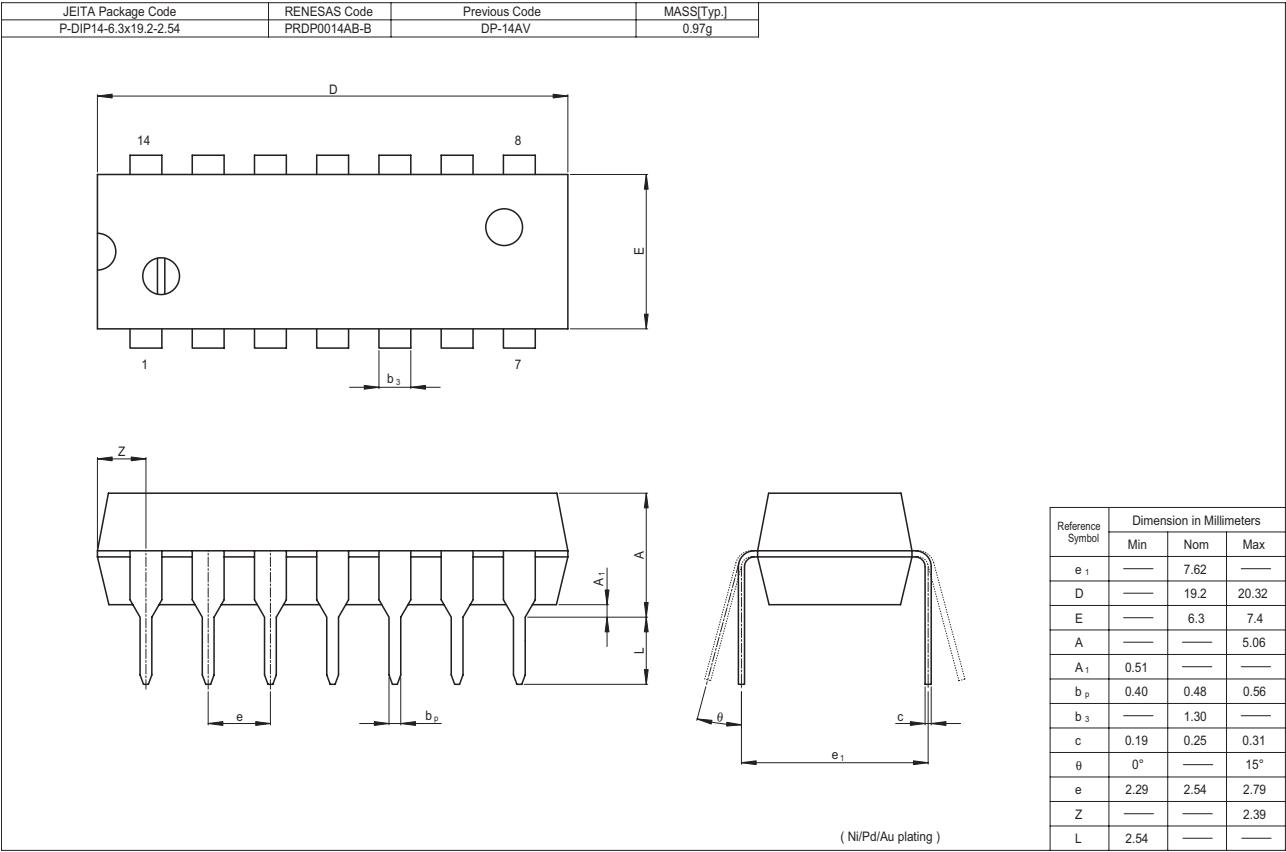


• Waveform – 2

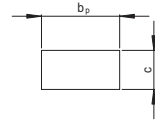
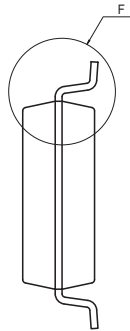
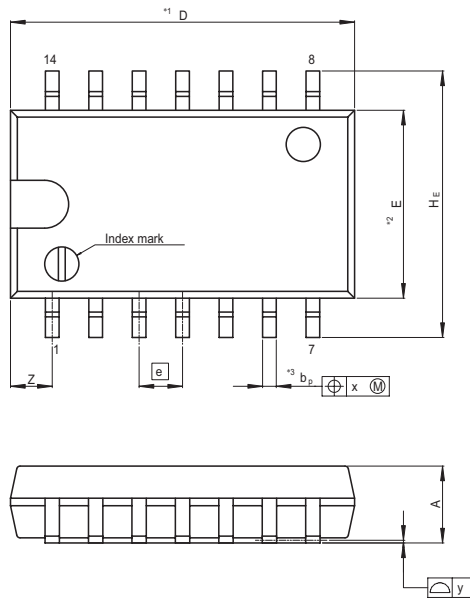


Notes: 1. Input waveform: $\text{PPR} \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

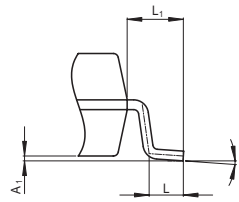
Package Dimensions



JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
z	—	—	1.42
L	0.50	0.70	0.90
L ₁	—	1.15	—

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