



74HC123; 74HCT123

Dual retriggerable monostable multivibrator with reset

Rev. 13 — 21 February 2024

Product data sheet

1. General description

The 74HC123; 74HCT123 is a dual retriggerable monostable multivibrator with reset. The basic output pulse width is programmed by selection of external components (R_{EXT} and C_{EXT}). Once triggered this basic pulse width may be extended by retriggering either of the edge triggered inputs ($n\bar{A}$ or $n\bar{B}$). By repeating this process, the output pulse period ($nQ = HIGH$, $nQ = LOW$) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\bar{RD}$. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Schmitt-trigger action in the $n\bar{A}$ and $n\bar{B}$ inputs, makes the circuit highly tolerant to slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC123: CMOS level
 - For 74HCT123: TTL level
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC123D 74HCT123D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC123PW 74HCT123PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC123BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

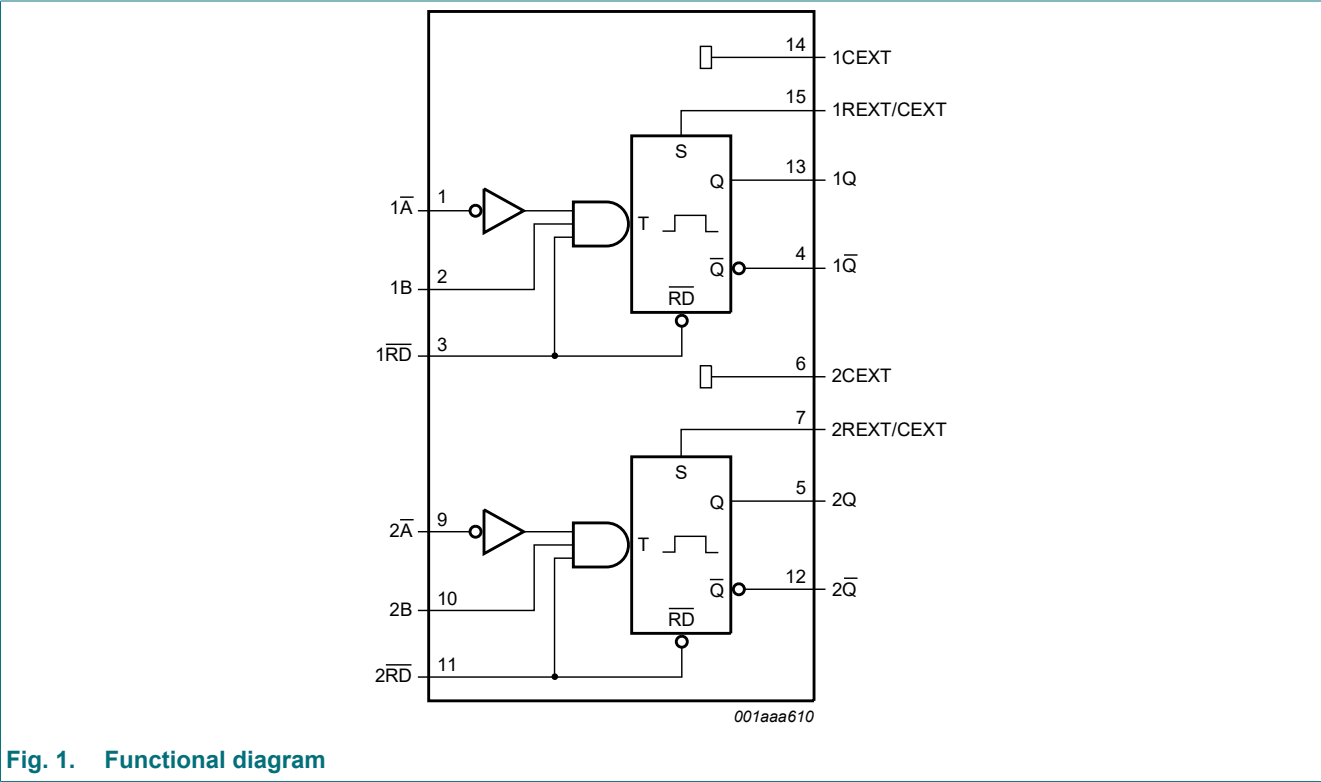


Fig. 1. Functional diagram

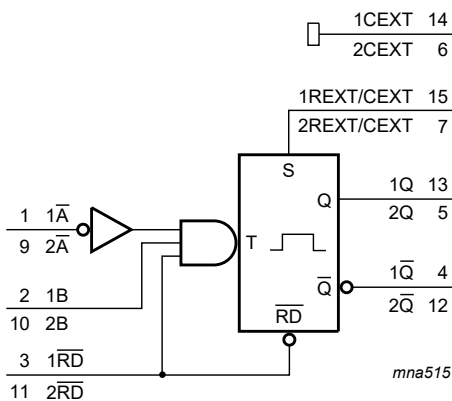


Fig. 2. Logic symbol

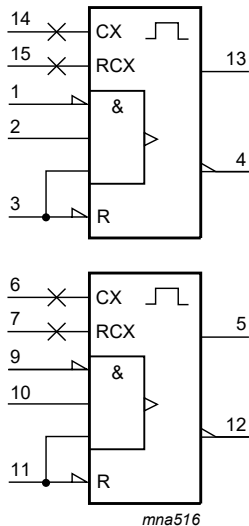


Fig. 3. IEC logic symbol

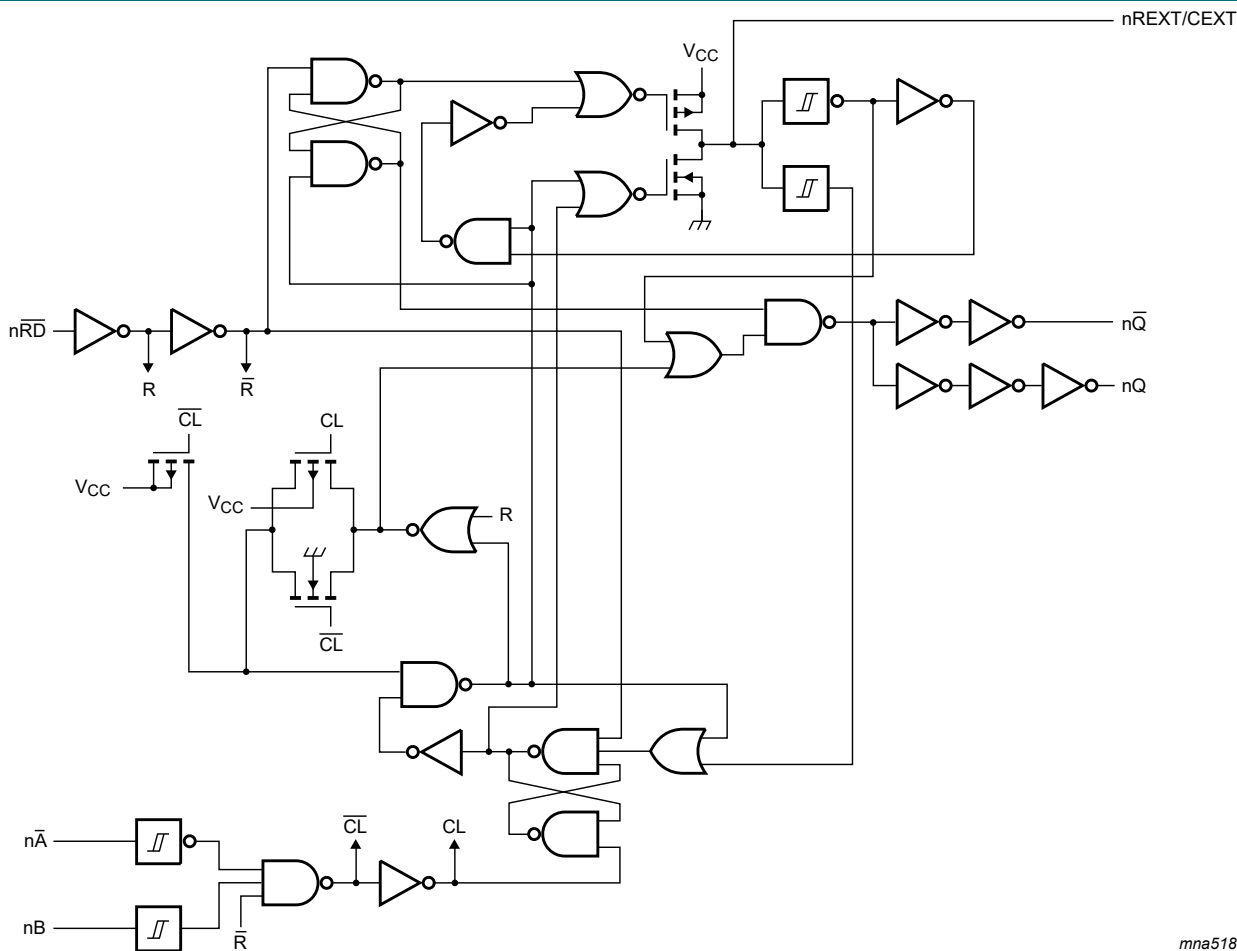
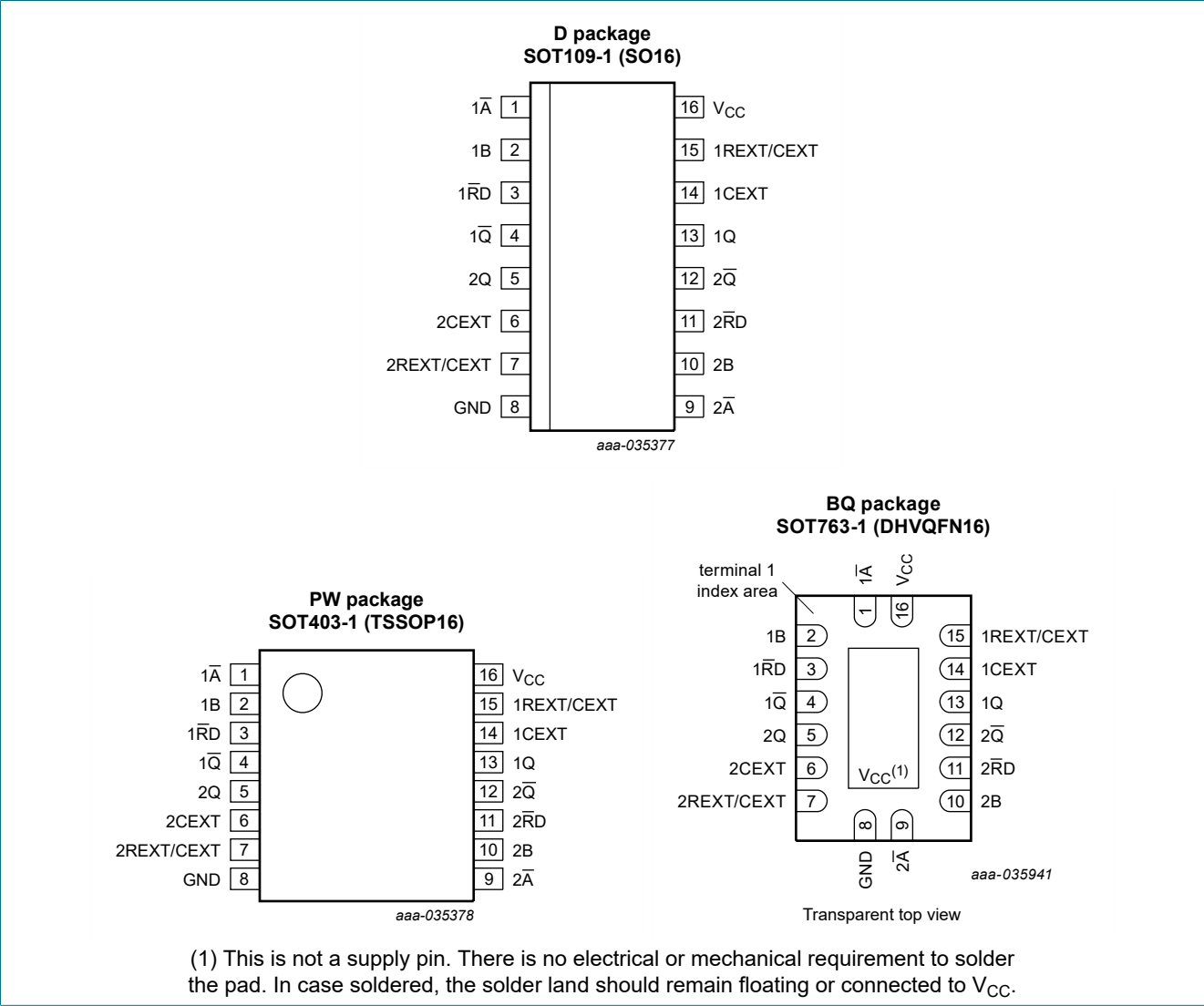


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1RD	3	direct reset LOW and positive-edge triggered input 1
1Q	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2A	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2RD	11	direct reset LOW and positive-edge triggered input 2
2Q	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;
 = one HIGH level output pulse;  = one LOW level output pulse.

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L [1]	H [1]
X	X	L	L [1]	H [1]
H	L	↑		
H	↓	H		
↑	L	H		

[1] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	except for pins nREXT/CEXT; V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC123			74HCT123			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	nRD input							
		V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC123										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Dual retriggerable monostable multivibrator with reset

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT123										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; I _O = 0 A; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pins nA, nB	-	35	125	-	160	-	170	µA
		pin nRD	-	50	180	-	225	-	245	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Fig. 10](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC123										
t _{pd}	propagation delay	nRD, nA, nB to nQ or nQ; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7 [1]								
		V _{CC} = 2.0 V	-	83	255	-	320	-	385	ns
		V _{CC} = 4.5 V	-	30	51	-	64	-	77	ns
		V _{CC} = 5 V; C _L = 15 pF	-	26	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	24	43	-	54	-	65	ns
		nRD (reset) to nQ or nQ; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7								
		V _{CC} = 2.0 V	-	66	215	-	270	-	325	ns
		V _{CC} = 4.5 V	-	24	43	-	54	-	65	ns
		V _{CC} = 5 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	19	37	-	46	-	55	ns
t _t	transition time	see Fig. 7 [1]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	nA LOW; see Fig. 8								
		V _{CC} = 2.0 V	100	8	-	125	-	150	-	ns
		V _{CC} = 4.5 V	20	3	-	25	-	30	-	ns
		V _{CC} = 6.0 V	17	2	-	21	-	26	-	ns
		nB HIGH; see Fig. 8								
		V _{CC} = 2.0 V	100	17	-	125	-	150	-	ns
		V _{CC} = 4.5 V	20	6	-	25	-	30	-	ns
		V _{CC} = 6.0 V	17	5	-	21	-	26	-	ns
		nRD LOW; see Fig. 9								
		V _{CC} = 2.0 V	100	14	-	125	-	150	-	ns
		V _{CC} = 4.5 V	20	5	-	25	-	30	-	ns
		V _{CC} = 6.0 V	17	4	-	21	-	26	-	ns
		nQ HIGH and nQ LOW; V _{CC} = 5.0 V; see Fig. 8 and Fig. 9 [2]								
		C _{EXT} = 100 nF; R _{EXT} = 10 kΩ	-	450	-	-	-	-	-	μs
C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	-	75	-	-	-	-	-	ns		
t _{trig}	retrigger time	nA, nB; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; V _{CC} = 5.0 V; see Fig. 8 [3] [4]	-	110	-	-	-	-	-	ns

Dual retriggerable monostable multivibrator with reset

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
R _{EXT}	external timing resistor	see Fig. 5								
		V _{CC} = 2.0 V	10	-	1000	-	-	-	-	kΩ
		V _{CC} = 5.0 V	2	-	1000	-	-	-	-	kΩ
C _{EXT}	external timing capacitor	V _{CC} = 5.0 V; see Fig. 5 [4]	-	-	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per monostable; V _I = GND to V _{CC} [5]	-	54	-	-	-	-	-	pF
74HCT123										
t _{PHL}	HIGH to LOW propagation delay	nRD, nA, nB to nQ or nQ; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7								
		V _{CC} = 4.5 V	-	30	51	-	64	-	77	ns
		V _{CC} = 5 V; C _L = 15 pF	-	26	-	-	-	-	-	ns
		nRD (reset) to nQ or nQ; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7								
		V _{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		V _{CC} = 5 V; C _L = 15 pF	-	23	-	-	-	-	-	ns
t _{PLH}	LOW to HIGH propagation delay	nRD, nA, nB to nQ or nQ; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7								
		V _{CC} = 4.5 V	-	28	51	-	64	-	77	ns
		V _{CC} = 5 V; C _L = 15 pF	-	26	-	-	-	-	-	ns
		nRD (reset) to nQ or nQ; C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7								
		V _{CC} = 4.5 V	-	23	46	-	58	-	69	ns
		V _{CC} = 5 V; C _L = 15 pF	-	23	-	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see Fig. 7 [1]	-	7	15	-	19	-	22	ns
t _w	pulse width	V _{CC} = 4.5 V								
		nA LOW; see Fig. 8	20	3	-	25	-	30	-	ns
		nB HIGH; see Fig. 8	20	5	-	25	-	30	-	ns
		nRD LOW; see Fig. 9	20	7	-	25	-	30	-	ns
		nQ HIGH and nQ LOW; V _{CC} = 5.0 V; see Fig. 8 and Fig. 9 [2]								
		C _{EXT} = 100 nF; R _{EXT} = 10 kΩ	-	450	-	-	-	-	-	μs
t _{trig}	retrigger time	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ	-	75	-	-	-	-	-	ns
		R _{EXT} = 5 kΩ; V _{CC} = 5.0 V; see Fig. 8 [3] [4]	-	110	-	-	-	-	-	ns
R _{EXT}	external timing resistor	V _{CC} = 5.0 V; see Fig. 5	2	-	1000	-	-	-	-	kΩ
C _{EXT}	external timing capacitor	V _{CC} = 5.0 V; see Fig. 5 [4]	-	-	-	-	-	-	-	pF

Dual retriggerable monostable multivibrator with reset

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	per monostable; V _I = GND to V _{CC} - 1.5 V	[5]	-	56	-	-	-	-	pF

- [1]

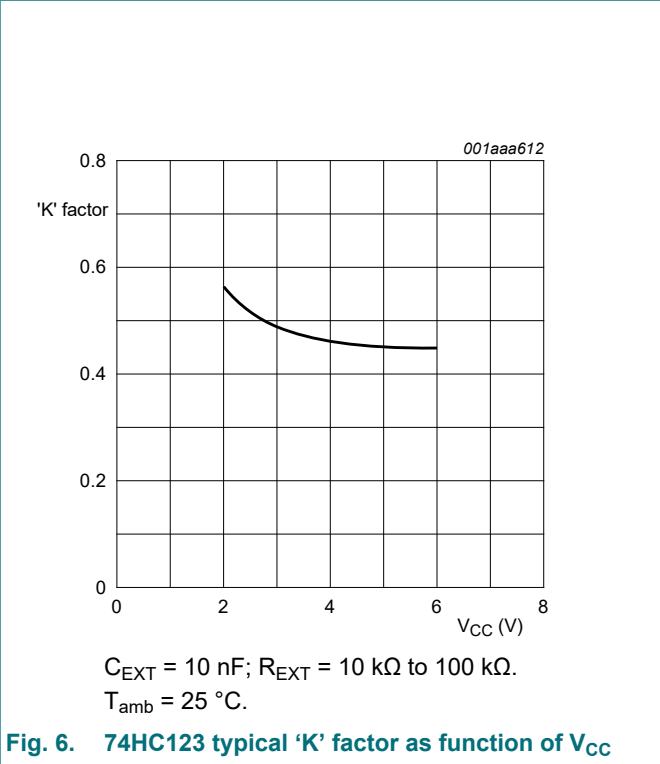
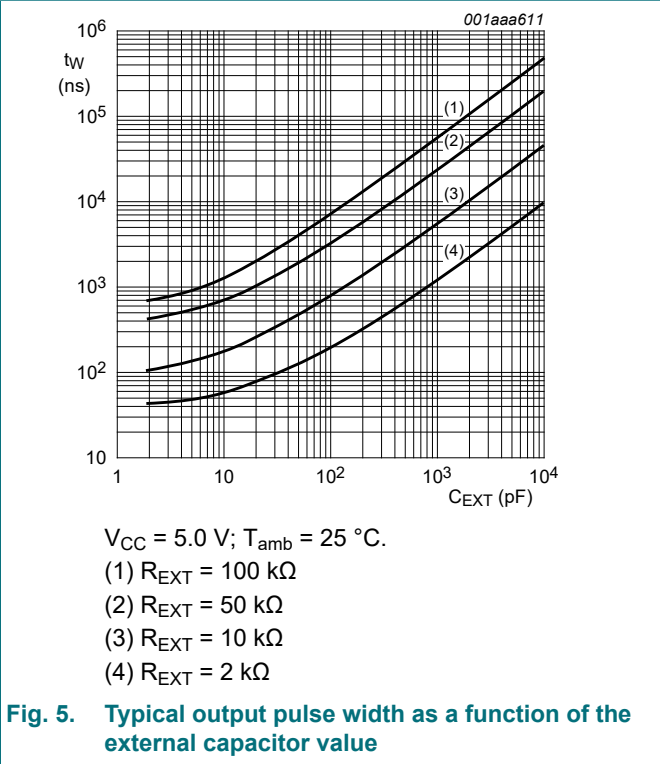
t_{pd} is the same as t_{PHL} and t_{PLH}; t_i is the same as t_{THL} and t_{TLH}
- [2]

For other R_{EXT} and C_{EXT} combinations see Fig. 5. If C_{EXT} > 10 nF, the next formula is valid:
t_W = K × R_{EXT} × C_{EXT}, where:
t_W = typical output pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF;
K = constant = 0.45 for V_{CC} = 5.0 V and 0.55 for V_{CC} = 2.0 V, see Fig. 6.
The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.
- [3]

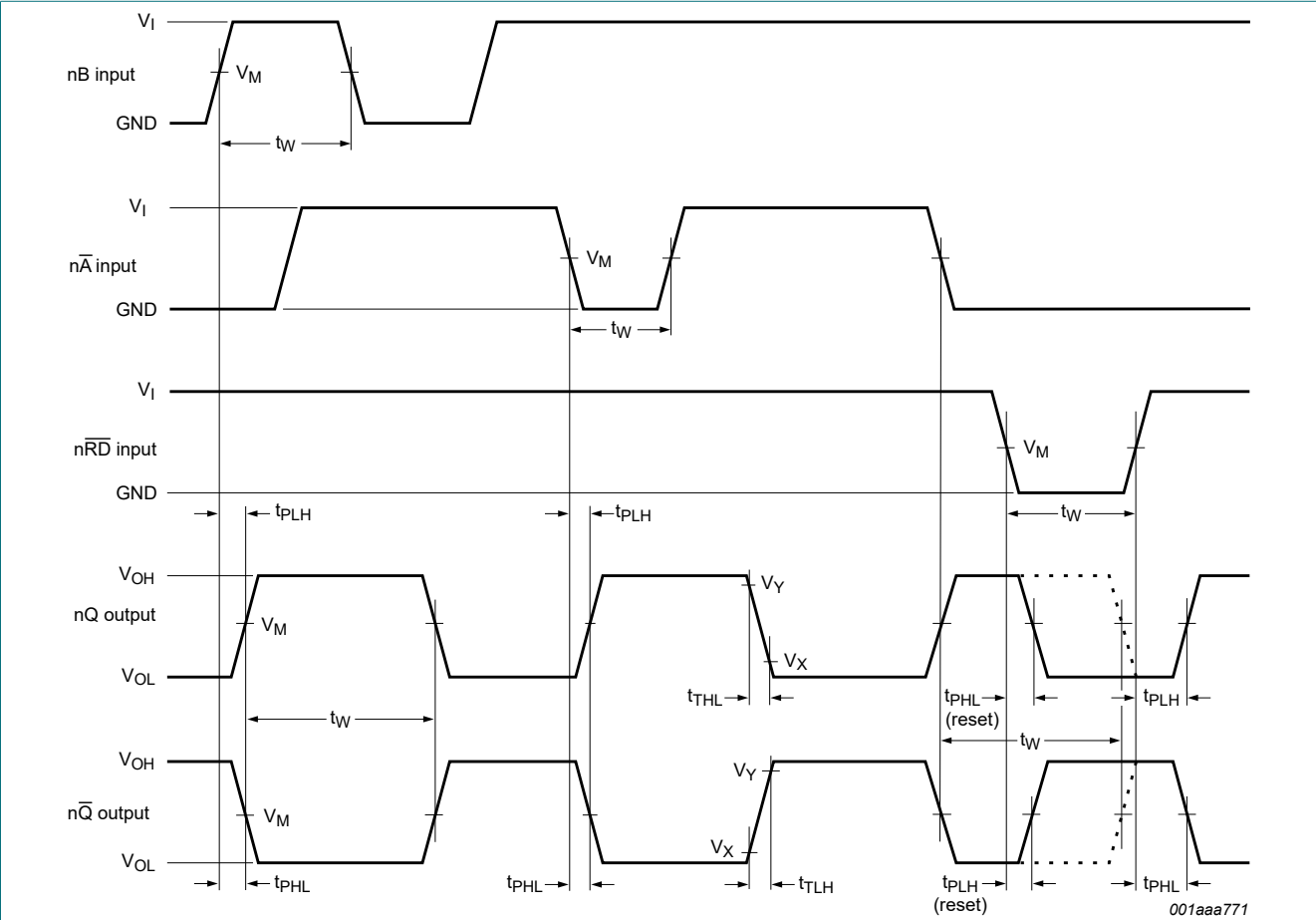
The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT} > 10 pF, the next formula (at V_{CC} = 5.0 V) for the setup time of a retrigger pulse is valid:
t_{trig} = 30 + 0.19 × R_{EXT} × C_{EXT}^{0.9} + 13 × R_{EXT}^{1.05}, where:
t_{trig} = retrigger time in ns;
C_{EXT} = external capacitor in pF; R_{EXT} = external resistor in kΩ.
The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is 7 pF.
- [4]

When the device is powered-up, initiate the device via a reset pulse, when C_{EXT} < 50 pF.
- [5]

C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i + Σ(C_L × V_{CC}² × f_o) + 0.75 × C_{EXT} × V_{CC}² × f_o + D × 16 × V_{CC} where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
D = duty factor in %;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
C_{EXT} = timing capacitance in pF;
Σ(C_L × V_{CC}² × f_o) sum of outputs.

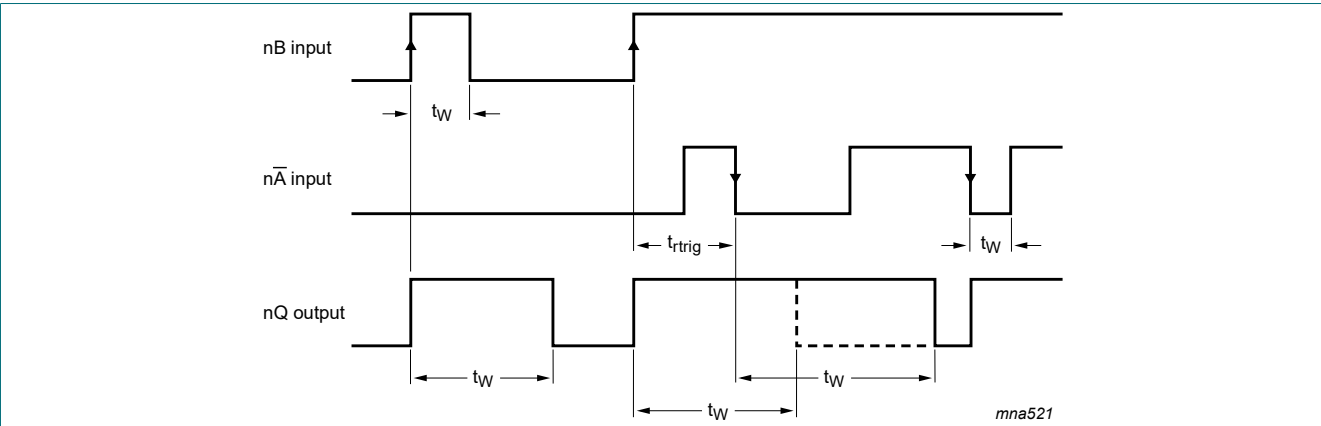


10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Propagation delays from inputs ($n\bar{A}$, nB , $n\bar{RD}$) to outputs (nQ , $n\bar{Q}$) and output transition times



$n\bar{RD} = \text{HIGH}$

Fig. 8. Output pulse control using retrigger pulse

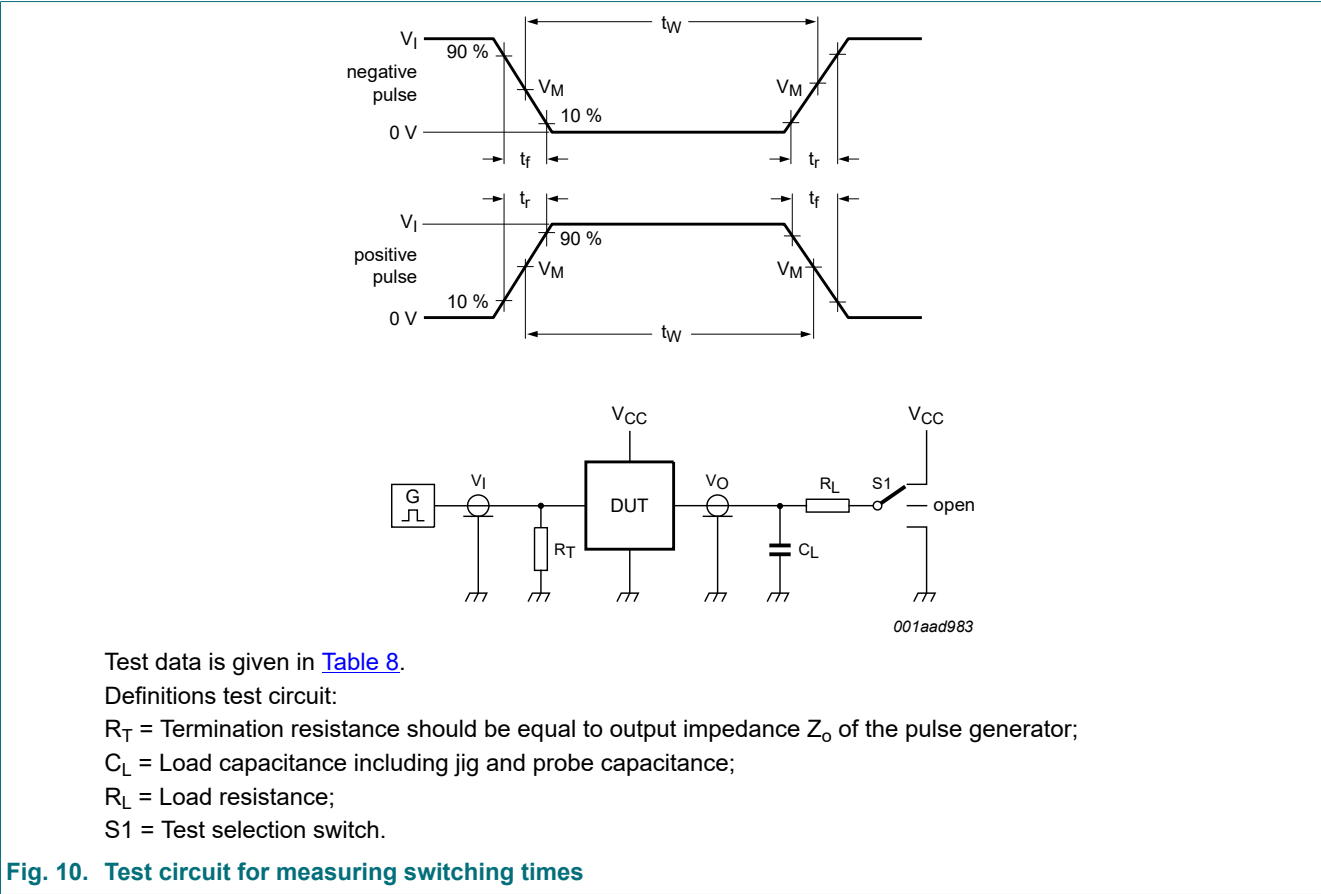
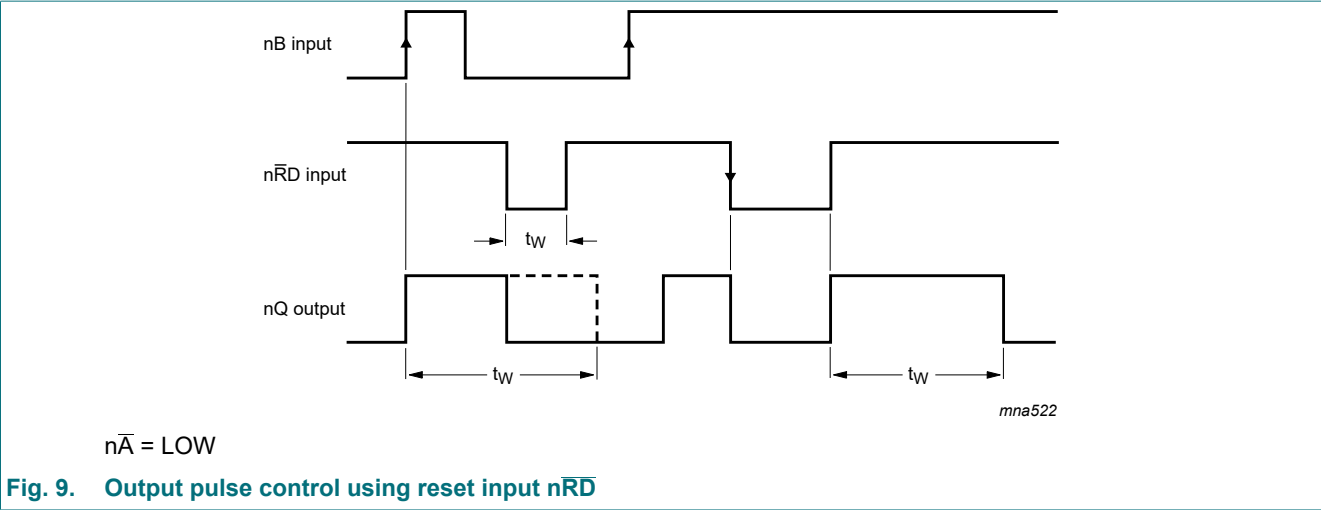


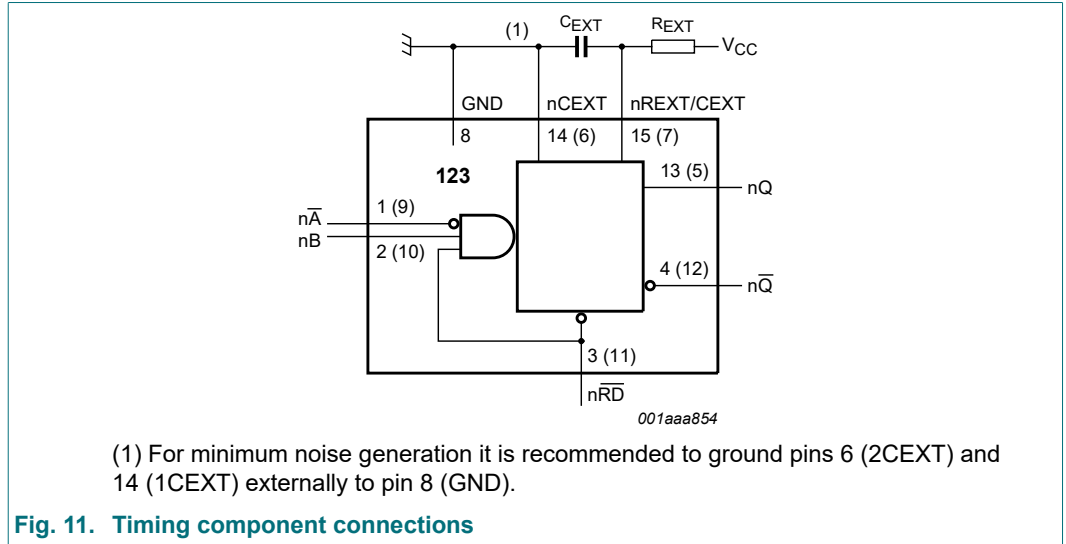
Table 8. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC123	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT123	3 V	6 ns	15 pF, 50 pF	1 k Ω	open

11. Application information

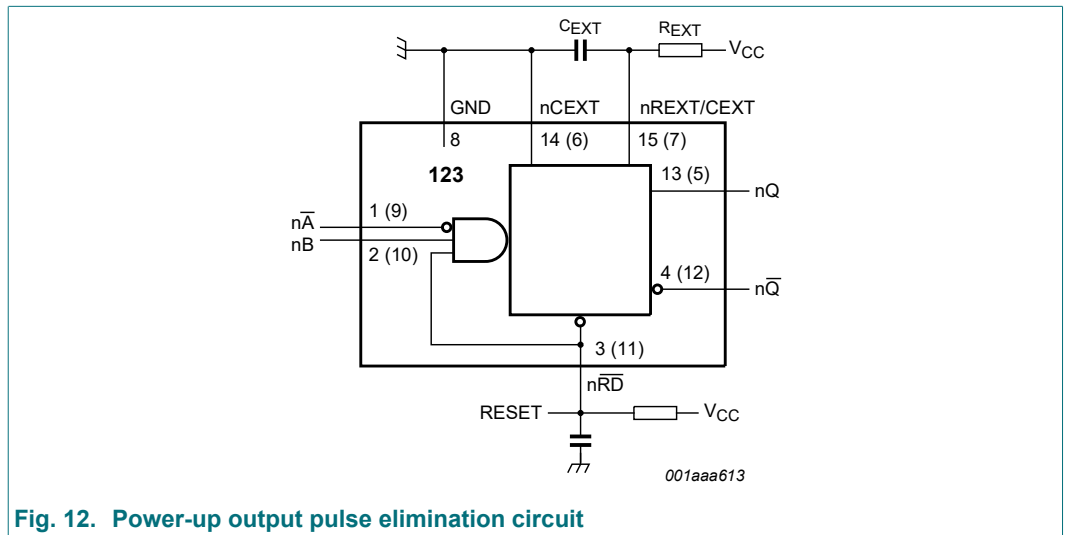
11.1. Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT} .



11.2. Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT} . This output pulse can be eliminated using the circuit shown in [Fig. 12](#).



11.3. Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Fig. 13](#).

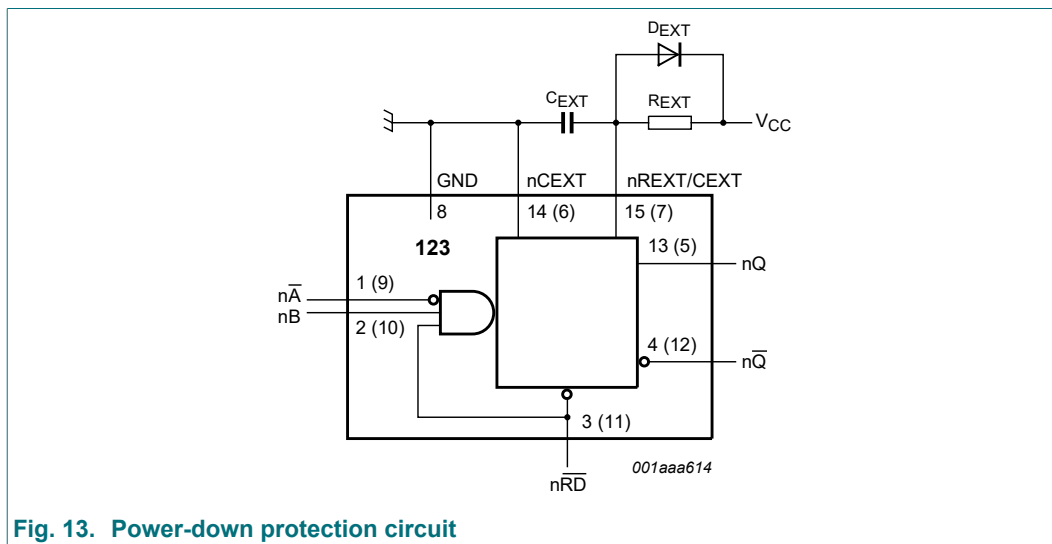


Fig. 13. Power-down protection circuit

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

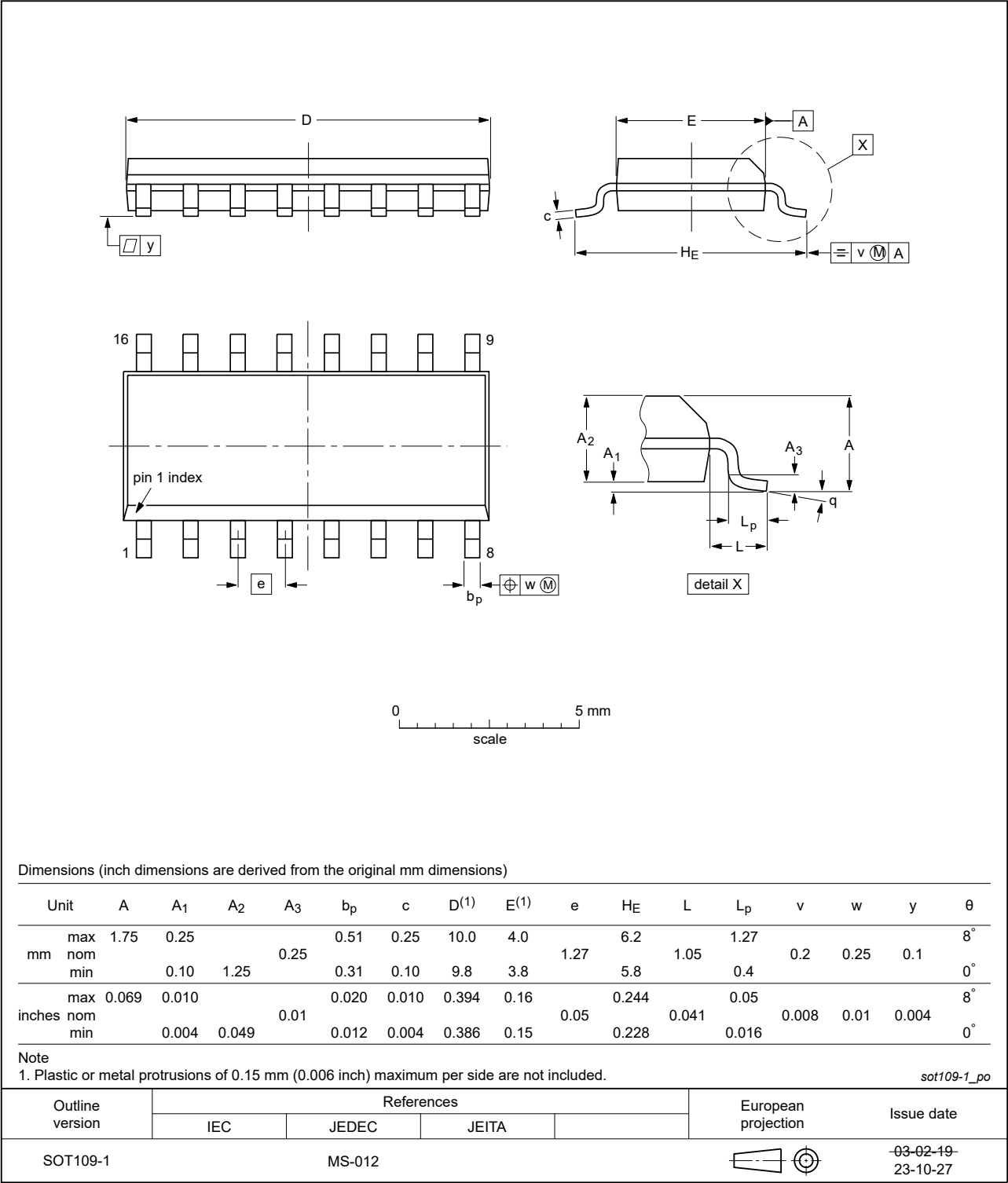


Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

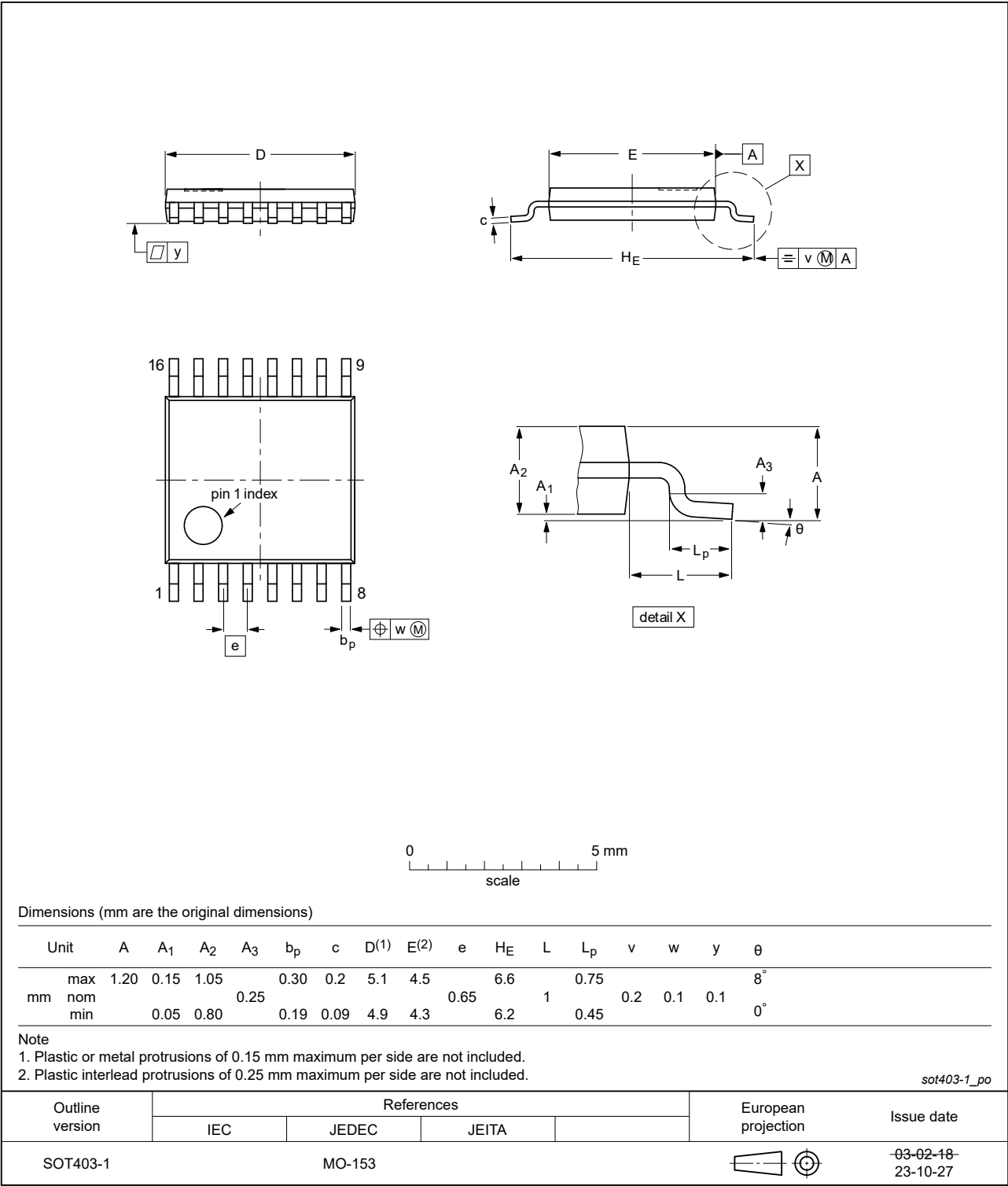


Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

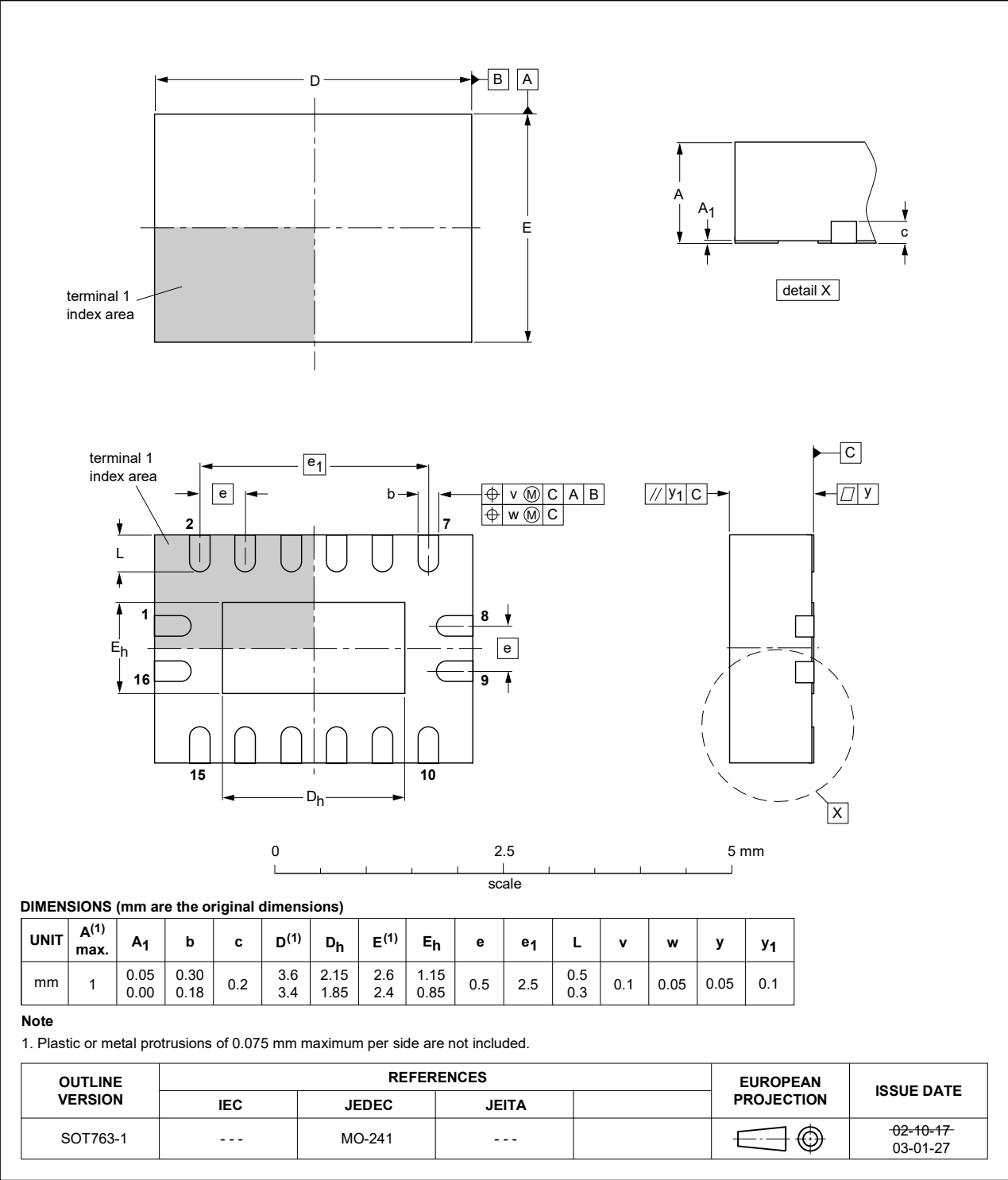


Fig. 16. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Abbreviation
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT123 v.13	20240221	Product data sheet	-	74HC_HCT123 v.12
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 14, Fig. 15: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC_HCT123 v.12	20210811	Product data sheet	-	74HC_HCT123 v.11
Modifications:	Type numbers 74HC123DB and 74HCT123DB (SOT338-1/SSOP16) removed.			
74HC_HCT123 v.11	20200903	Product data sheet	-	74HC_HCT123 v.10
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Section 1 and Section 2 updated. - Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT123 v.10	20151203	Product data sheet	-	74HC_HCT123 v.9
Modifications:	Type numbers 74HC123N and 74HCT123N (SOT38-4) removed.			
74HC_HCT123 v.9	20150119	Product data sheet	-	74HC_HCT123 v.8
Modifications:	Table 7: Power dissipation capacitance condition for 74HCT123 is corrected.			
74HC_HCT123 v.8	20111216	Product data sheet	-	74HC_HCT123 v.7
Modifications:	Legal pages updated.			
74HC_HCT123 v.7	20110825	Product data sheet	-	74HC_HCT123 v.6
74HC_HCT123 v.6	20110314	Product data sheet	-	74HC_HCT123 v.5
74HC_HCT123 v.5	20090713	Product data sheet	-	74HC_HCT123 v.4
74HC_HCT123 v.4	20060616	Product data sheet	-	74HC_HCT123 v.3
74HC_HCT123 v.3	20040511	Product specification	-	74HC_HCT123_CNV v.2
74HC_HCT123_CNV v.2	19980708	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information.....2

4. Functional diagram.....2

5. Pinning information.....4

5.1. Pinning..... 4

5.2. Pin description..... 5

6. Functional description..... 5

7. Limiting values..... 6

8. Recommended operating conditions.....6

9. Static characteristics.....6

10. Dynamic characteristics..... 8

10.1. Waveforms and test circuit..... 11

11. Application information..... 13

11.1. Timing component connections..... 13

11.2. Power-up considerations..... 13

11.3. Power-down considerations..... 14

12. Package outline..... 15

13. Abbreviations..... 18

14. Revision history..... 18

15. Legal information..... 19

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