



MOTOROLA

**MC12009 MC12509
MC12011 MC12511
MC12013 MC12513**

TWO-MODULUS PRESCALER

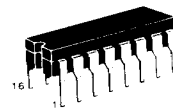
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 600 MHz (Typ) Toggle Frequency
- MC12009 ($\div 5/6$), MC12011 ($\div 8/9$), MC12013 ($\div 10/11$)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- +5.0 or -5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ohms and 4 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

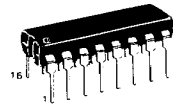
*When using a +5.0 V supply, apply +5.0 V to Pin 1 (V_{CC}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using -5.2 V supply, ground Pin 1 (V_{CC}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply -5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

MECL PLL COMPONENTS

TWO-MODULUS PRESCALER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage ($V_{CC} = 0$)	V_{EE}	-8.0	Vdc
Input Voltage ($V_{CC} = 0$)	V_{in}	0 to V_{EE}	Vdc
Output Source Current Continuous Surge	I_O	< 50 < 100	mA dc
Storage Temperature Range	T_{stg}	-65 to +175	°C

(Recommended Maximum Ratings above which performance may be degraded)

Operating Temperature Range	T_A	°C
MC12009, MC12011, MC12013 MC12509, MC12511, MC12513	-30 to +85 -55 to +125	

*DC Fan-Out (Gates and Flip-Flops)

n

70

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*AC fan-out is limited by desired system performance.

PIN ASSIGNMENT

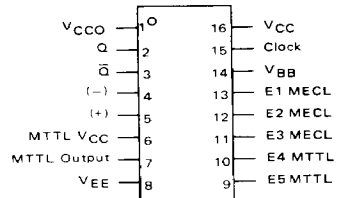
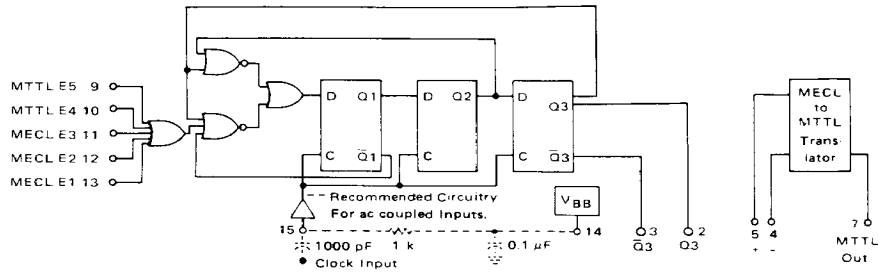
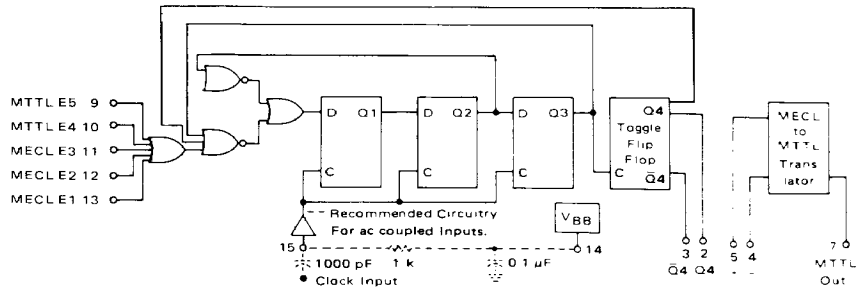


FIGURE 1 – LOGIC DIAGRAMS

MC12009



MC12011



MC12013

± 10 for one or all
E1 thru E5 high
± 11 for all
E1 thru E5 low
Tie unused gate inputs low.

Pull down resistors required on
Pins 2, 3 when not connected to
translator.
Basic IC Capability: ± 10/11

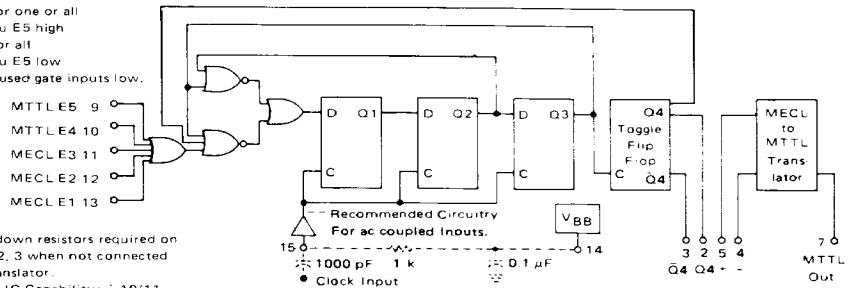
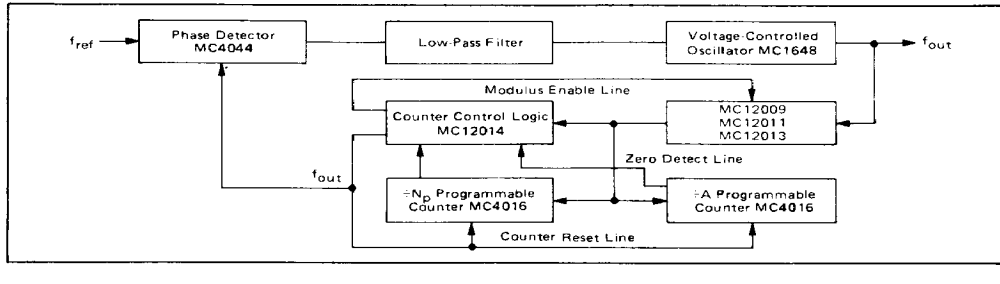


FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



ELECTRICAL CHARACTERISTICS Supply Voltage -5.2 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to -20 Vdc.

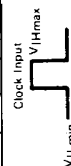
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① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

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② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

Characteristic		TEST VOLTAGE/CURRENT VALUES										mA				
		Volts														
		V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	I _L	I _{OH}	
@ Test Temperature																
-30°C																
-25°C																
+25°C																
+55°C																
TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:																
Characteristic		Pin Under Test	MC12009, MC12011, MC12013				+85°C				V _{EE} /Gnd					
			Min	Max	Typ	Min	Max	Unit	V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	V _{IHmax}	V _{IHmin}	I _L	I _{OH}
Power Supply Drain Current	I _{CC1}	8	-88			-80	5.2	mAdc	4	5				1.16		8
Input Current	I _{CC2}	6		5.2				mAdc						6		8
	I _{INH1}	15		375		250		µAdc	15					1.16		8
	I _{INH2}	13							11		9.10					
	I _{INH3}	13							12		9.10					
Input Current	I _{INH4}	4	1.7	6.0	2.0	6.0	2.0	6.4	mAdc	5	4					8
	I _{INH5}	5	1.7	6.0	2.0	6.0	2.0	6.4	mAdc	5	4					8
	I _{INH6}	5	0.7	3.0	1.0	3.6			mAdc	4	5			6		8
	I _{INH7}	9		100		100		100	µAdc			9	10			8
Leakage Current	I _{INL1}	10		100		100		100	µAdc							8
	I _{INL2}	15	-10		10		10		µAdc					1.16		8
	I _{INL3}	12												1.16		8
	I _{INL4}	13												1.16		8
Reference Voltage	V _{BB}	14			3.67		3.87		Vdc					1.16		8
	V _{OH1}	2	3.900	4.110	4.000	4.190	4.070	4.300	Vdc					1.16	14	8
	V _{OH2}	3	3.900	4.110	4.000	4.190	4.070	4.300	Vdc					1.16		8
	V _{OL1}	7	2.4		2.6		2.8		Vdc	5	4			6		8
Logic '0' Output Voltage	V _{OL1}	2	3.070	3.385	3.110	3.410	3.135	3.445	Vdc					1.16		8
	V _{OL2}	3	3.070	3.385	3.110	3.410	3.135	3.445	Vdc					1.16		8
	V _{OL3}	7	0.94		0.80		0.72		Vdc	4	5			1.16		8
	V _{OL4}	2	3.880		3.980		4.050		Vdc					6		8
Logic '1' Threshold Voltage	V _{TH1}	7							Vdc					1.16		8
	V _{TH2}	3							Vdc					1.16		8
	V _{TH3}	2							Vdc					1.16		8
	V _{TH4}	3							Vdc					1.16		8
Logic '0' Threshold Voltage	V _{TL1}	7	65	20	65	20	65	20	mAdc	5	4			1.16		8
	V _{TL2}	3							mAdc					1.16		8
	V _{TL3}	2							mAdc					1.16		8
	V _{TL4}	3							mAdc					1.16		8
Short Circuit Current	I _{OS}	7							mAdc					1.16		8
	I _{OS1}	7							mAdc					1.16		8
	I _{OS2}	3							mAdc					1.16		8
	I _{OS3}	2							mAdc					1.16		8

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② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to +3.0 Vdc.

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE/CURRENT VALUES										mA																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
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SWITCHING CHARACTERISTICS

SWITCHING CHARACTERISTICS											TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW										
Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013									Unit	Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V _{IHmin} †	V _{ILmin} †	V _P -3.0 V	V _{EE} -3.0 V	V _{CC} +2.0	
			-30°C			+25°C			+85°C												
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max										
Propagation Delay (See Figures 3 and 5)	t ₁₅₊₂₊ t ₁₅₊₂₋ t ₁₅₊₇₊ t ₁₅₊₇₋	2 2 7 7	- - - -	8.1 7.5 8.4 6.5	- - - -	8.1 7.5 8.1 6.5	- - - -	8.9 8.7 8.9 7.1	ns ns A A	15 15 A A	- - - -	- - - -	- - - -	11 12 13 11 12 13 - -	9 10 8 8 8	8 8 8 8	1.6 1.6 1.6 1.6 1.6 1.6 1.6 1.6				
Setup Time (See Figures 4 and 5)	t _{setup1} t _{setup2}	11 9	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	ns ns	15 15	- -	- -	11 12 13 11 12 13	9 10 8	8 8	1.6 1.6 1.6 1.6			
Release Time (See Figures 4 and 5)	t _{rel1} t _{rel2}	11 9	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	ns ns	15 15	- -	- -	11 12 13 11 12 13	9 10 8	8 8	1.6 1.6 1.6 1.6			
Toggle Frequency (See Figure 6)	f _{max}	2	-	-	-	-	-	-	-	-	MHz	-	-	-	-	-	-	-			
			MC12009 5.6			MC12011 8.9			MC12013 10.11												
			440			480			440												
			500			550			500												
			500			550			500												

† Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other inputs of the same type (i.e., MECL or MTTL).

	-30°C	+25°C	+85°C	
t _{VIHmin}	+1.03	+1.115	+1.20	Vdc
t _{VILmin}	+0.175	+0.200	+0.235	Vdc

SWITCHING CHARACTERISTICS

SWITCHING CHARACTERISTICS											TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW										
Characteristic	Symbol	Pin Under Test	MC12509, MC12511, MC12513									Unit	Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V _{IHmin} †	V _{ILmin} †	V _P -3.0 V	V _{EE} -3.0 V	V _{CC} +2.0	
			-55°C			+25°C			+125°C												
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max										
Propagation Delay (See Figures 3 and 5)	t ₁₅₊₂₊ t ₁₅₊₂₋ t ₁₅₊₇₊ t ₁₅₊₇₋	2 2 7 7	- - - -	- 8.1 7.5 8.4 6.5	- - - -	- 8.1 7.5 8.1 6.5	- - - -	- 9.4 8.7 9.4 7.6	- - - -	ns	15 15 A A	- - - -	- - - -	- 11 12 13 11 12 13 - -	- 9 10 8 8	- 8 8 8	- 1.6 1.6 1.6 1.6 1.6 1.6				
Setup Time (See Figures 4 and 5)	t _{setup1} t _{setup2}	11 9	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	ns ns	15 15	- -	- 11 12 13	- 8	- 8	- 1.6 1.6				
Release Time (See Figures 4 and 5)	t _{rel1} t _{rel2}	11 9	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	ns ns	15 15	- -	- 11 12 13	- 8	- 8	- 1.6 1.6				
Toggle Frequency (See Figure 6)	f _{max}	2	-	-	-	-	-	-	-	-	MHz	-	-	-	-	-	-	-			
			MC12509 5.6			MC12511 8.9			MC12513 10.11												
			420			480			420												
			500			550			500												
			500			550			500												

† Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other inputs of the same type (i.e., MECL or MTTL).

	-55°C	+25°C	+125°C	
t _{VIHmin}	+1.02	+1.15	+1.27	Vdc
t _{VILmin}	+0.165	+0.215	+0.260	Vdc

FIGURE 3 — AC VOLTAGE WAVEFORMS

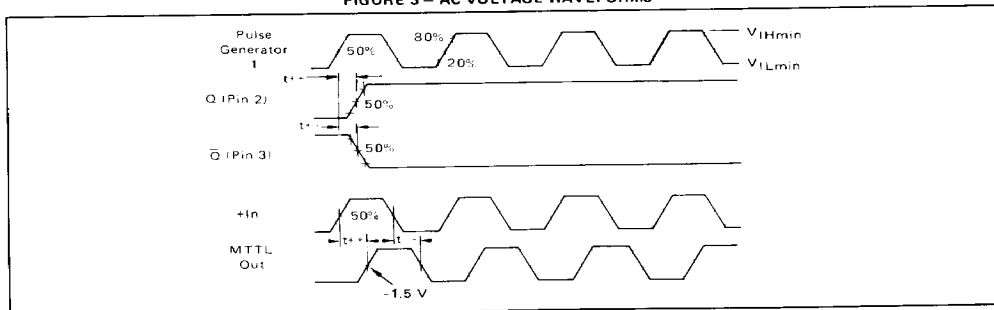


FIGURE 4 – SETUP AND RELEASE TIME WAVEFORMS

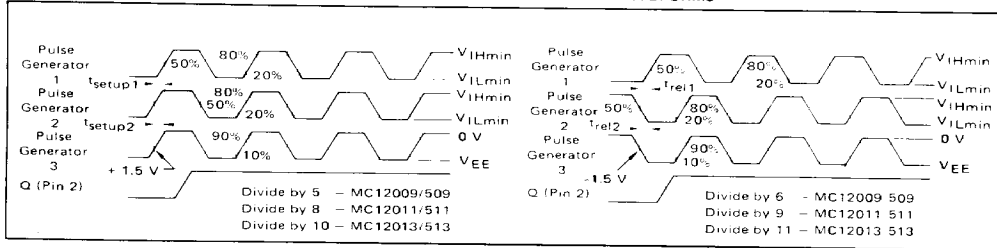


FIGURE 5 – AC TEST CIRCUIT

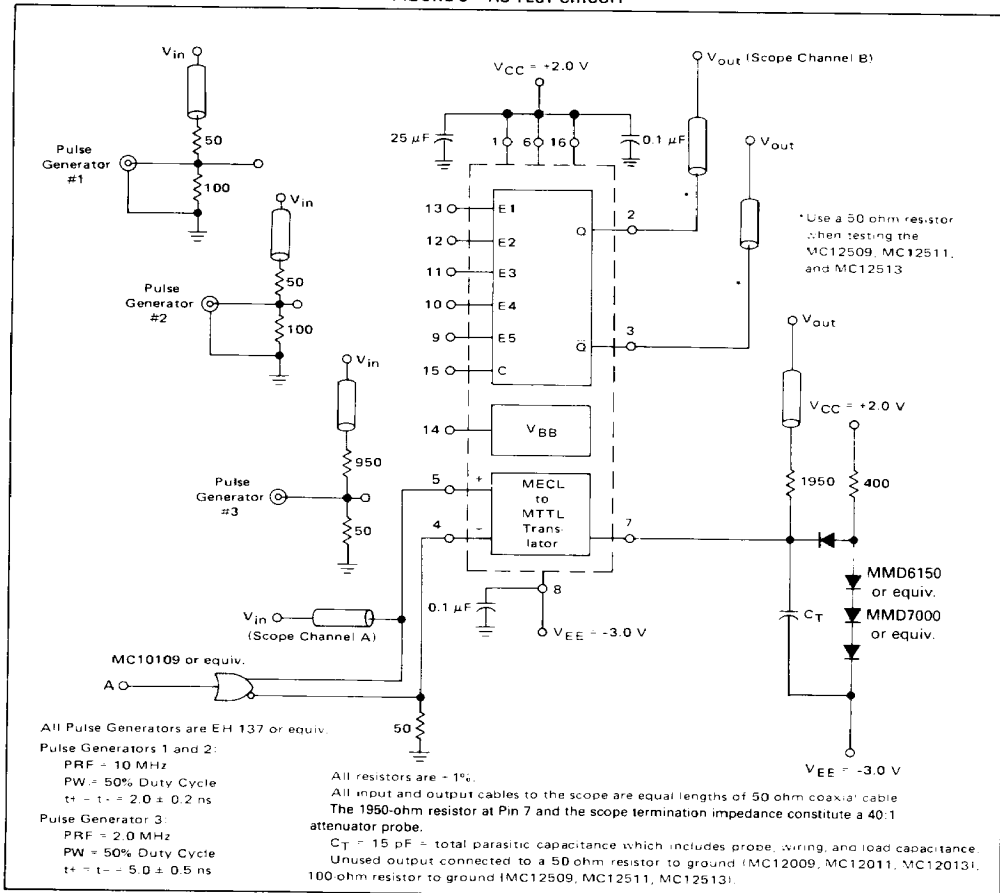
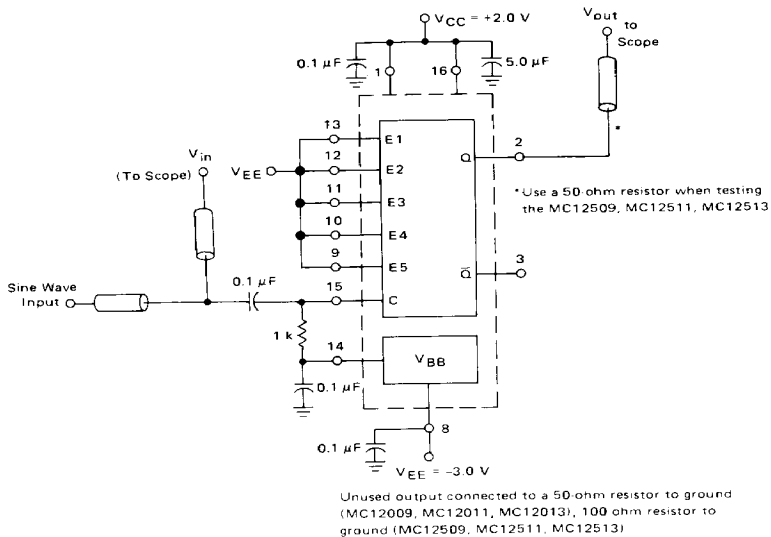
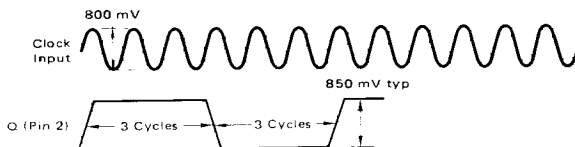


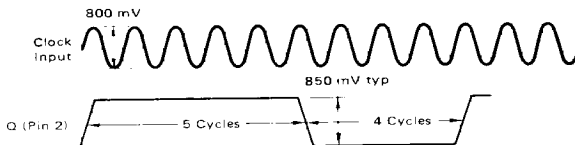
FIGURE 6 — MAXIMUM FREQUENCY TEST CIRCUIT



DIVIDE BY 6



DIVIDE BY 9



DIVIDE BY 11

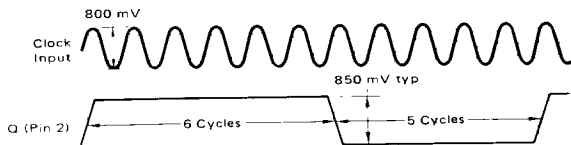
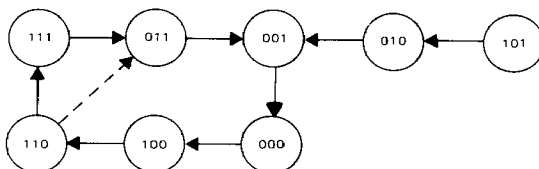
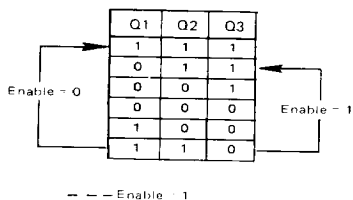
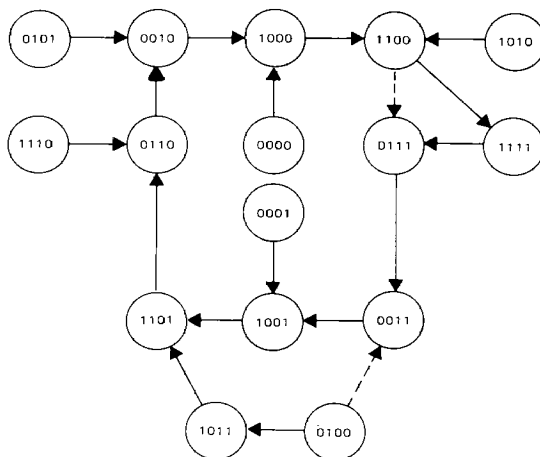
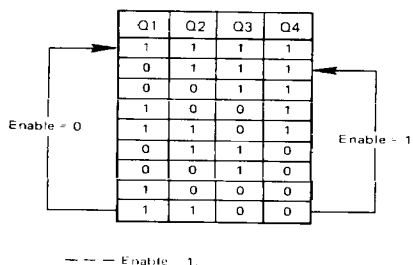


FIGURE 7 – STATE DIAGRAM

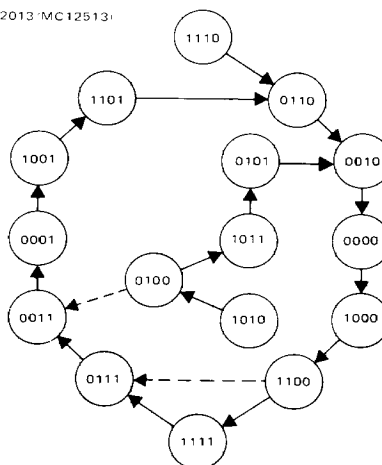
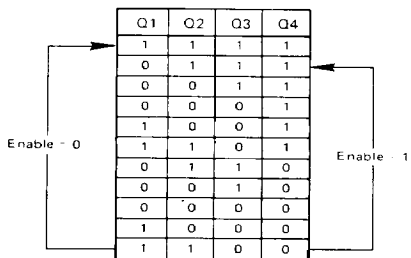
DIVIDE BY 5/6 (MC12009/MC12509)



DIVIDE BY 8/9 (MC12011/MC12511)



DIVIDE BY 10/11 (MC12013/MC12513)



NOTES

--- Enable = 1

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

APPLICATIONS INFORMATION

The primary application of these devices is as a high-speed variable modulus prescaler in the divide by N section of a phase-locked loop synthesizer used as the local oscillator of two-way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in Motorola's "Electronic Tuning Address Systems" (SG72).

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In their basic form, these devices will divide by 5/6, 8/9, or 10/11. Division by 5, 8, or 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, 9, or 11 occurs when all inputs E1 through E5 are low. (Unconnected MECL inputs are normally high, unconnected MTTL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.) A few of the many configurations are shown below, only for the MC12013/MC12513.

FIGURE 8 — DIVIDE BY 10/11 (MC12013/MC12513)

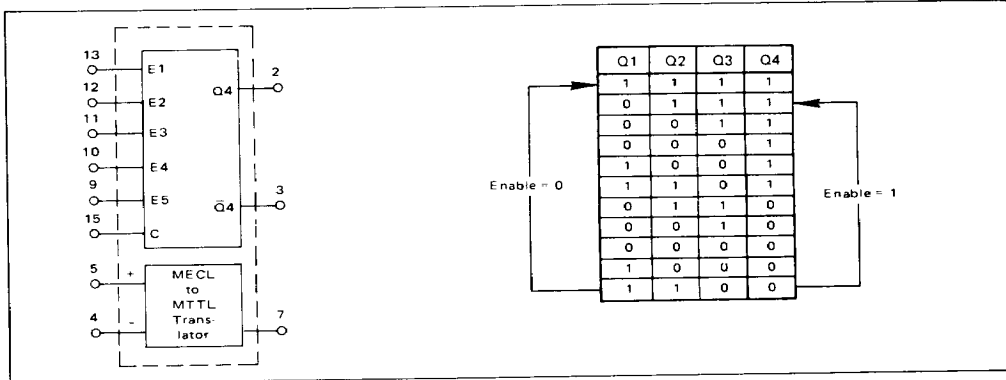


FIGURE 9 — DIVIDE BY 20/21 (MC12013/MC12513)

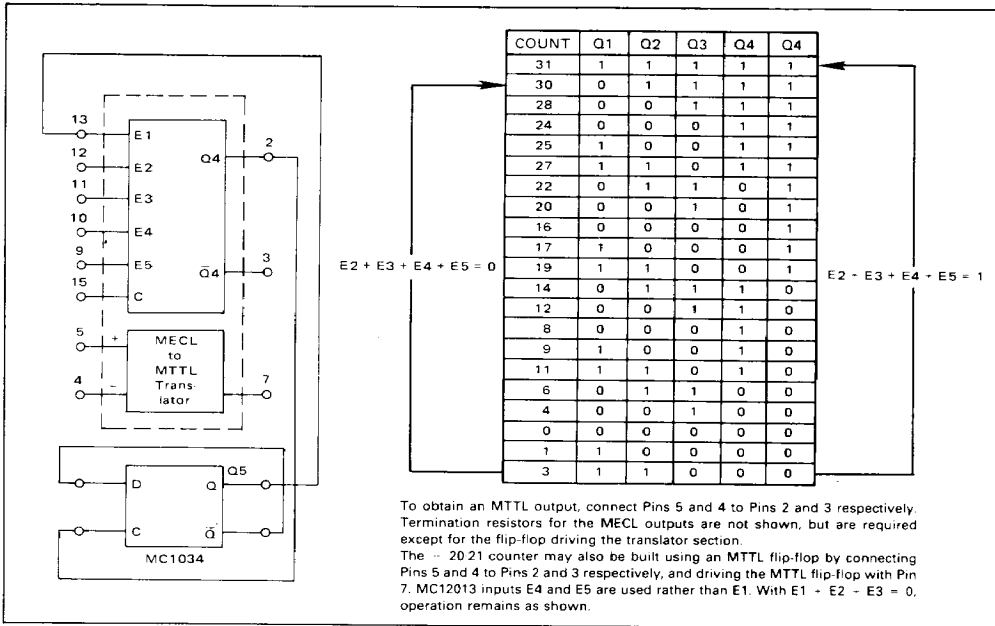


FIGURE 10 — DIVIDE BY 40/41 (MC12013/MC12513)

