

CD4018B Types

CMOS Presettable Divide-By-'N' Counter

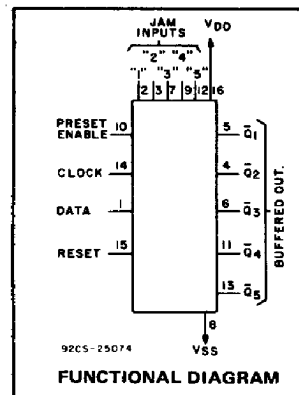
High-Voltage Types (20-Volt Rating)

■ CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\bar{Q}_5$, $\bar{Q}_4$, $\bar{Q}_3$, $\bar{Q}_2$, $\bar{Q}_1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5; or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

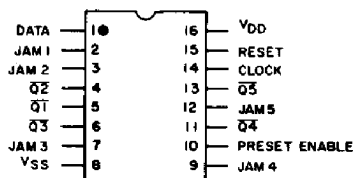
The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Medium speed operation 10 MHz (typ.) at $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of $1\text{ }\mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at $V_{DD} = 5\text{ V}$
 2 V at $V_{DD} = 10\text{ V}$
 2.5 V at $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL DIAGRAM
Top View



92CS-24460

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-'N' counters/frequency synthesizers
- Frequency division
- Counter control/timers

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5\text{ V}$

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{ mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{ mm}$) from case for 10s max $+265^\circ\text{C}$

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RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Clock Input Frequency, f_{CL}	5 10 15	— — —	3 7 8.5	MHz
Clock Pulse Width, t_W	5 10 15	160 70 50	— — —	ns
Clock Rise & Fall Time, t_{rCL}, t_{fCL}	5 10 15	Unlimited		μs
Data Input Set-Up Time, t_S	5 10 15	40 12 16	— — —	ns
Data Input Hold Time, t_H	5 10 15	140 80 60	— — —	ns
Preset or Reset Pulse Width, t_W	5 10 15	160 70 50	— — —	ns
Preset or Reset Removal Time	5 10 15	160 60 40	— — —	ns

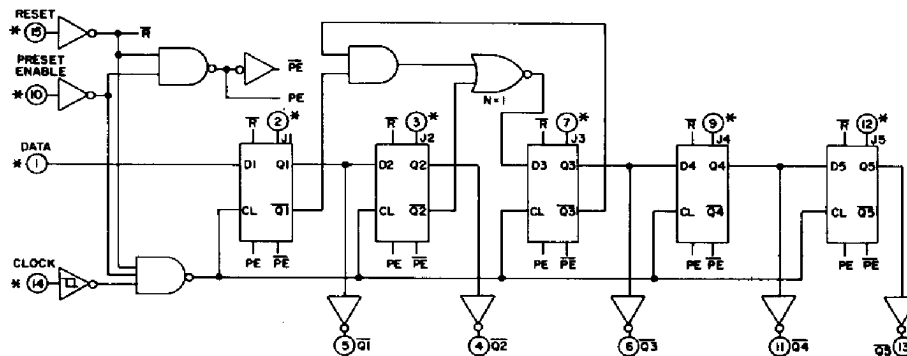


Fig. 1 — Logic diagram.

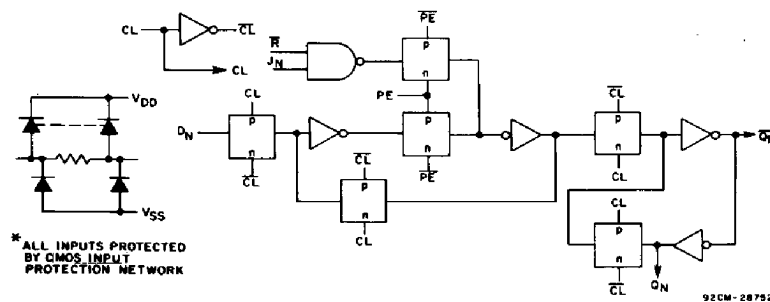


Fig. 2 — Detail of a typical stage.

CD4018B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

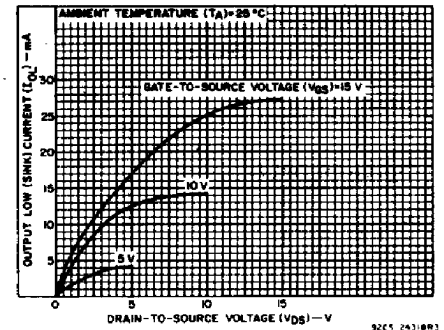


Fig. 3 - Typical output low (sink) current characteristics.

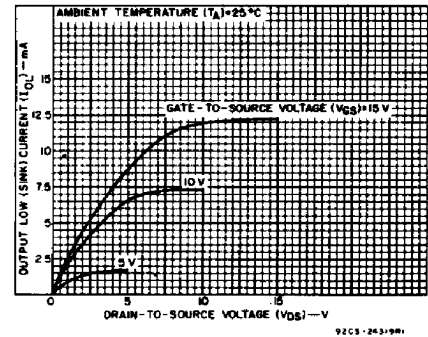


Fig. 4 - Minimum output low (sink) current characteristics.

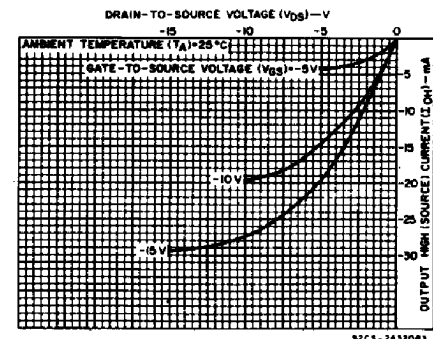


Fig. 5 - Typical output high (source) current characteristics.

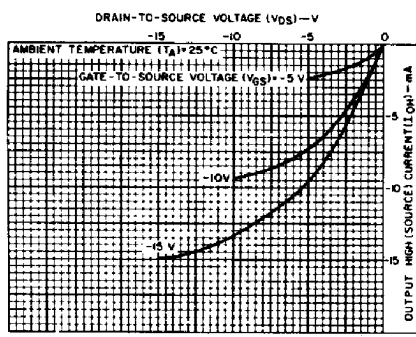


Fig. 6 - Minimum output high (source) current characteristics.

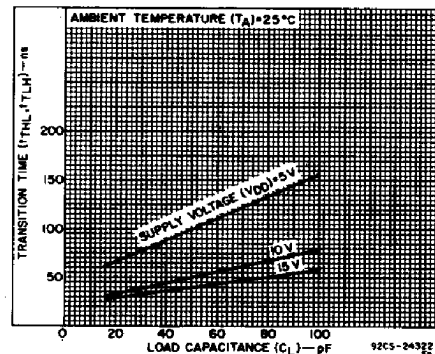


Fig. 7 - Typical transition time as a function of load capacitance.

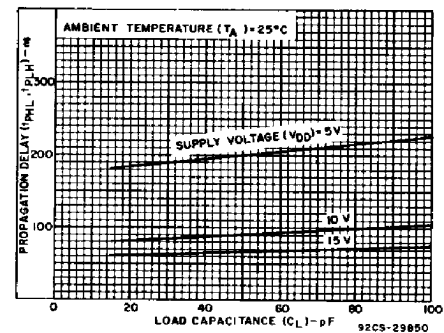


Fig. 8 - Typical propagation delay time as a function of load capacitance (CLOCK to Q).

CD4018B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V _{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
Propagation Delay Time; t _{PLH} , t _{PHL}		5	—	200	400	ns
		10	—	90	180	
		15	—	65	130	
Transition Time; t _{THL} , t _{TLH}		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Maximum Clock Input Frequency, f _{CL}		5	3	6	—	MHz
		10	7	14	—	
		15	8.5	17	—	
Minimum Clock Pulse Width, t _W		5	—	80	160	ns
		10	—	35	70	
		15	—	25	50	
Clock Rise & Fall Time; t _{rCL} , t _{fCL}		5	Unlimited			μs
		10				
		15				
Minimum Data Input Set-Up Time, t _S		5	—	20	40	ns
		10	—	6	12	
		15	—	3	6	
Minimum Data Input Hold Time, t _H		5	—	70	140	ns
		10	—	40	80	
		15	—	30	60	
Average Input Capacitance, C _I	Any Input		—	5	7.5	pF
PRESET* OR RESET OPERATION						
Propagation Delay Time; Preset or Reset to Q̄ t _{PLH} , t _{PHL}		5	—	275	550	ns
		10	—	125	250	
		15	—	90	180	
Minimum Preset or Reset Pulse Width, t _W		5	—	80	160	ns
		10	—	35	70	
		15	—	25	50	
Minimum Preset or Reset Removal Time		5	—	80	160	ns
		10	—	30	60	
		15	—	20	40	

* At PRESET ENABLE or JAM Inputs.

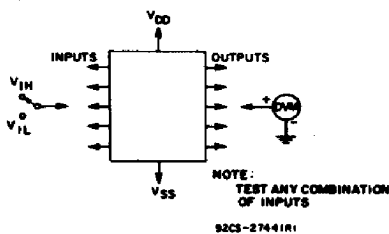


Fig. 12 - Input voltage test circuit.

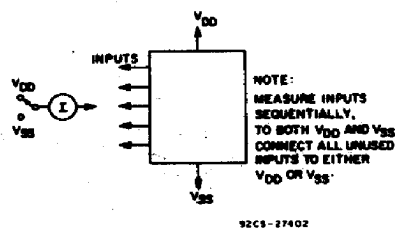


Fig. 13 - Input current test circuit.

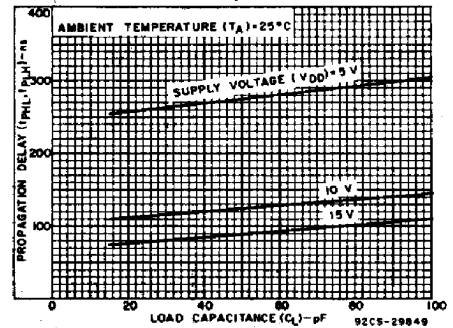


Fig. 9 - Typical propagation delay time as a function of load capacitance (RESET to Q).

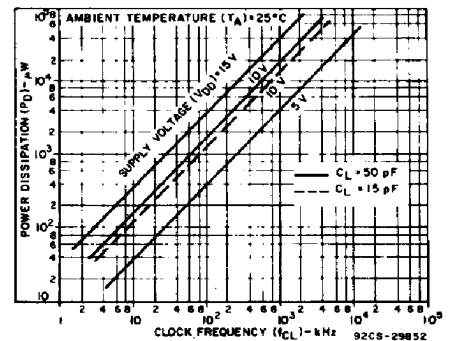


Fig. 10 - Typical dynamic power dissipation as a function of clock input frequency.

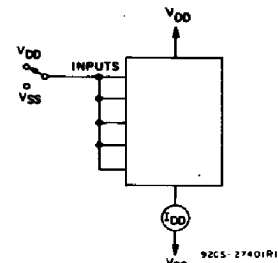


Fig. 11 - Quiescent device current test circuit.

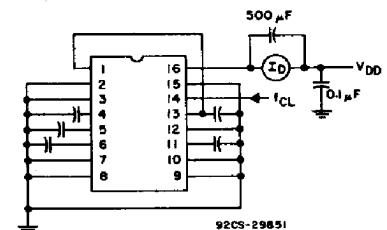


Fig. 14 - Dynamic power dissipation test circuit.

CD4018B Types

("DATA" INPUT TIED TO $\bar{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

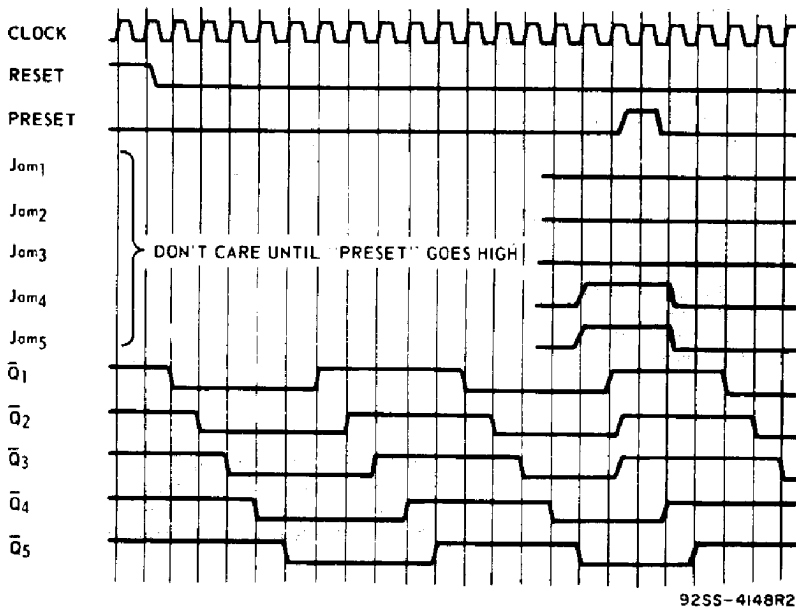
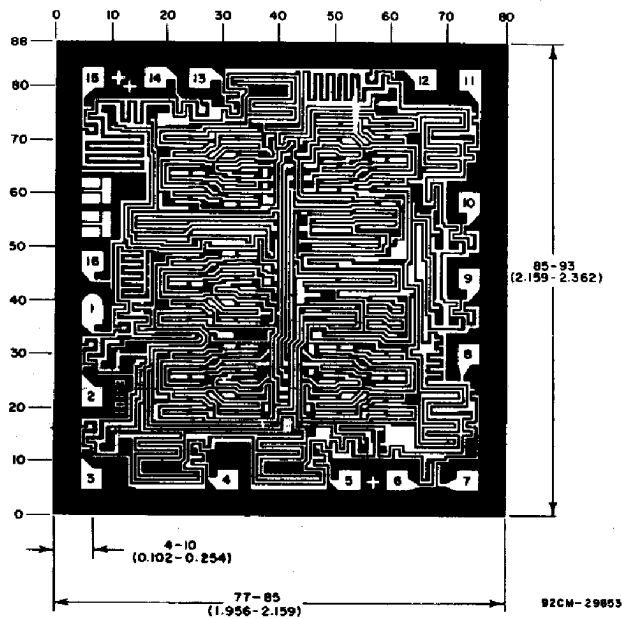


Fig. 15 - Timing diagram.



Chip dimensions and pad layout for CD4018B

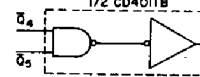
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10 $\bar{Q}_5$
 DIVIDE BY 8 $\bar{Q}_4$
 DIVIDE BY 6 $\bar{Q}_3$
 DIVIDE BY 4 $\bar{Q}_2$
 DIVIDE BY 2 $\bar{Q}_1$

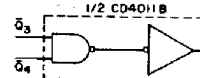
CONNECTED BACK TO "DATA"
 NO EXTERNAL COMPONENTS REQUIRED

DIVIDE BY 9



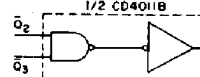
CONNECTED BACK TO "DATA"
 (SKIPS "ALL-1's" STATE)

DIVIDE BY 7



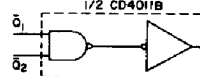
CONNECTED BACK TO "DATA"
 (SKIPS "ALL-1's" STATE)

DIVIDE BY 5



CONNECTED BACK TO "DATA"
 (SKIPS "ALL-1's" STATE)

DIVIDE BY 3



CONNECTED BACK TO "DATA"
 (SKIPS "ALL-1's" STATE)

92CS-1707/1R3

Fig. 16 - External connections for divide by 10, 9, 8, 7, 5, 4, 3, 2 operation.

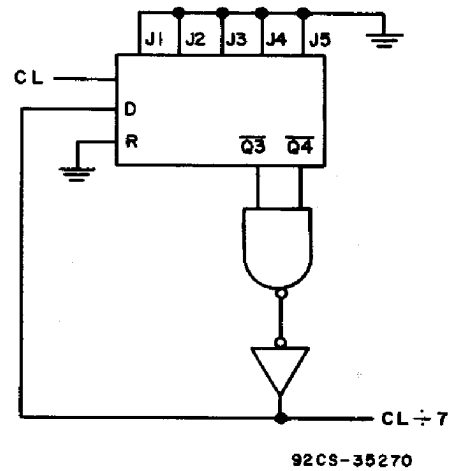


Fig. 17 - Example of divide by 7.