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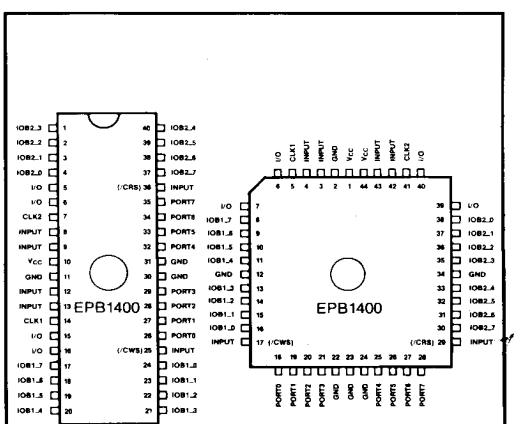
ALTERA

USER-CONFIGURABLE MICROPROCESSOR PERIPHERAL EPB1400

FEATURES

- Bus I/O — Register Intensive (BUSTER) EPLD.
- Erasable, User-Configurable Logic Device for Customized Microprocessor Peripheral Functions.
- Byte-Wide Microprocessor Bus Port with Programmable Control for use with 8, 16 and 32-bit MPUs at up to 25MHz Clock Rate.
- Dual Byte-Wide Input and Output Registers for Fully Buffered Microprocessor Interfacing.
- 20 General Purpose Macrocells Featuring:
  Programmable Flip-Flop Type (D/T/JK/SR)
  Programmable Clocking
  Dual Feedback for Implementing Buried Registers Without Wasting I/O pins.
- 7 Control Macrocells for User-Defined Microprocessor Interface Control.
- Enhanced Drive Capability of 24mA for Direct Connection from Bus Port to External Bus.
- Efficient Design Entry using TTL SSI and MSI Macrofunctions with the Altera Programmable Logic User Software (A+PLUS).
- Packaged in 40 Pin Dual-In-Line (Plastic/ Cerdip) as well as 44 Lead JLCC or PLCC Chip Carriers.

CONNECTION DIAGRAM



(a) 40 Pin DIP **(b) 44 Lead JLCC**

GENERAL DESCRIPTION

The Altera EPB1400 is a user-configurable microprocessor peripheral device. Based on a Bus I/O-Register intensive (BUSTER) architecture, the device is a function-specific Erasable Programmable Logic Device (EPLD) tailored for the design of custom microprocessor peripheral applications.

A typical application environment for the EPB1400 is shown in Figure 1. The unique architecture and high integration density of the EPB1400 yields significant reduction in PC board real estate as well as critical speed enhancement. Integrating control and peripheral functions allows for the replacement of multiple MSI/SSI TTL packages and permits zero wait-state operation with 25 MHz processors. The EPB1400 contains a byte-wide I/O port which may interface to an 8-bit microprocessor directly, or to 16 and 32-bit devices operating in the 8-bit peripheral mode. Multiple EPB1400 devices may be operated in parallel when full 16 or 32-bit I/O is required.

The EPB1400 differs from general purpose programmable logic devices by the addition of specialized interface functions around a state-of-the-art user-configurable logic core. The result is a highly-integrated, user-programmable solution for custom peripheral functions (see Figure 2). Key elements include two byte-wide input functions which may be configured as transparent latches or edge-triggered registers (similar to 74373 or 74377, CMOS or TTL) and two byte-wide output latches (similar to 74373). (Hereafter, the input functions will simply be referred to as input registers.) These byte-wide functions may be used for buffering data from and to the EPB1400 internal bus. Communication to an external bus is provided by an 8-bit bus transceiver (similar to 74245). Enhanced drive capability on the transceiver ports (24mA) allows direct connection to the external bus. Read/Write control for all microprocessor interface functions is provided by two strobe pins and by seven Control Macrocells. These Control Macrocells permit user-defined logic functions to act as control inputs for each of the I/O buffer registers as well as the bus port transceiver. As a result, the EPB1400 may be customized to meet the requirements of any microprocessor bus (e.g., 68020, 80386, 80286, MIL1750A, Z80, etc.)

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

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In addition to Control Macrocells, the EPB1400 also contains 20 General Purpose Logic Macrocells for implementation of sequential and combinatorial logic functions such as address decoding, interrupt logic and state machines. Each of the General Purpose Macrocells may be configured on an individual basis. Macrocell features such as Dual Feedback, Programmable Flip-flops and Programmable Clocks guarantee maximum pin utility and design flexibility. User-defined logic within a macrocell may be sent directly to an I/O pin or fed back for use by other macrocells. In addition, macrocell feedback may access the EPB1400 internal bus via the I/O buffer registers.

Designing with the EPB1400 is straightforward. Designs may be entered as a mixture of TTL schematics (LogiCaps Schematic Capture and the associated TTL Library, PLSLIB-TTL), state machine files (Altera State Machine Entry, PLSME) and traditional Boolean equations (created with any standard text editor). Once entered, designs are automatically compiled by the Altera Programmable Logic User Software (A+PLUS). The A+PLUS design processor performs complete logic minimization, device fitting and report generation. Within minutes, a standard JEDEC programming file is generated for use in simulation (Altera Functional Simulator, PLFSIM) as well as device programming operations. This integrated design cycle allows designs to be conceived, prototyped, and iterated easily and efficiently.

The EPB1400 utilizes a 1 micron CMOS EPROM technology. User-defined logic functions and architectural configurations are constructed by selectively programming EPROM cells within the device. The EPROM technology guarantees 100% programming yield to the end user due to Generic Testability: all devices are tested 100% at the factory before shipment. Ultraviolet erasable devices enable design iterations to be performed rapidly without additional expense. For volume production needs, plastic One-Time-Programmable (OTP) versions are available.

FUNCTIONAL DESCRIPTION

The EPB1400 has 8 dedicated input pins, 20 I/O pins and 8 bus port pins. The EPB1400 is housed in 40 pin DIP or 44 pin J-lead, surface mount packages.

The EPB1400 detailed block diagram is shown in Figure 3. It contains two key functional blocks, the Microprocessor Interface Block and the Programmable Logic Core Block. Control Macrocells within the Microprocessor Interface Block provide custom control interface to any microprocessor. Of the 8 dedicated input pins, 4 may also be used as strobe inputs to the byte-wide elements in the Microprocessor Interface Block. These byte-wide elements include 2 input buffer registers, 2 output latches and a bus port transceiver. All byte-wide elements communicate via the internal bus.

Figure 1. Typical Microprocessor-Based System

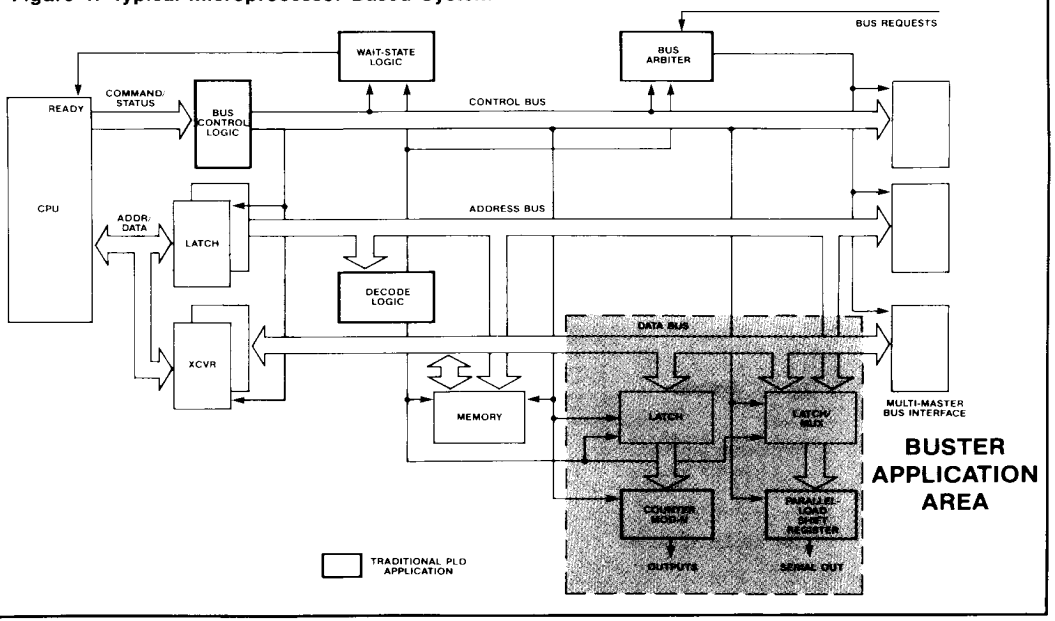
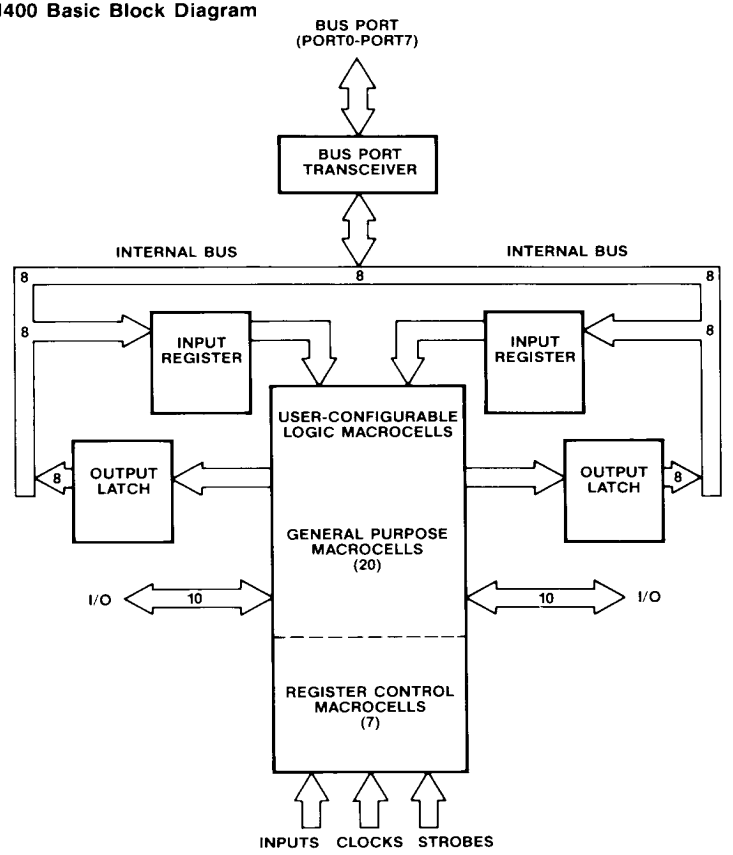


Figure 2. EPB1400 Basic Block Diagram

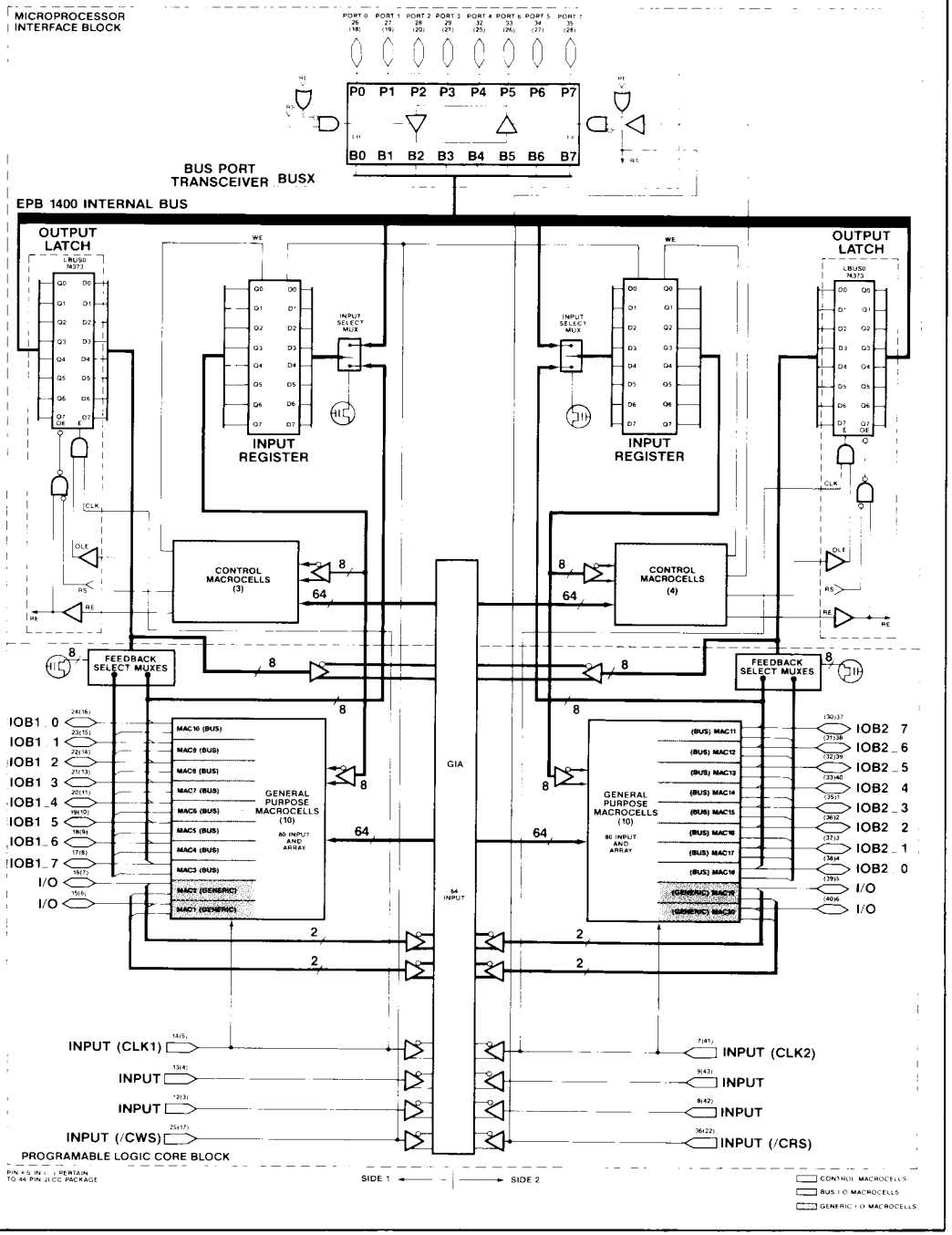


The Programmable Logic Core Block accepts general purpose logic functions related to microprocessor peripheral applications. These may include address decoding, frequency division, parallel/serial data conversions and state machine functions. The Programmable Logic Core contains 20 General Purpose Macrocells. The inputs to these macrocells come from an 80-input logic array consisting of 64 inputs from a Global Interconnect Access (GIA) and 16 feedback signals from input registers within the Microprocessor Interface Block. All macrocells contain programmable options that may be accessed on an individual macrocell basis. These include Dual Feedback, Programmable Flip-flops and Programmable Clocks. All macrocells may be buried internally while associated I/O pins are used as input pins. In addition to feeding the GIA, Macrocell feedback signals may also act as inputs to the input registers and output latches within the Microprocesor Interface Block.

MICROPROCESSOR INTERFACE BLOCK

The architecture of the EPB1400 Microprocessor Interface Block provides fast and efficient access to any microprocessor bus. An 8-bit internal bus is used to connect five byte-wide elements within the Microprocessor Interface Block. These five elements consist of two input buffer registers, two output latches, and a bus port transceiver. Control signals for each byte-wide element are derived within the Control Macrocells on each side. As a result, user-defined logic functions may be used for control of the I/O buffer registers and bus port transceiver.

Figure 3. EPB1400 Detailed Block Diagram



CONTROL MACROCELLS

Figure 4 shows the AND-OR-INVERT structure within each of the seven Control Macrocells. The three Control Macrocells on Side 1 provide control inputs for the buffer registers located on Side 1. The control inputs generated are Write Enable (WE) of the input register, and Output Latch Enable (OLE) and Read Enable (RE) of the output latch. User-defined logic within these Control Macrocells may be a function of any signals within the 80-input Control Array; 16 of these array signals come from the true and complement of the 8 buffered outputs from the input register (Q and /Q), the remaining 64 array signals are contained within the GIA of the EPB1400. Signals within the GIA originate from feedback signals generated by macrocells within the Programmable Logic Core Block as well as signals from input pins to the device.

The four Control Macrocells on Side 2 generate control inputs for the microprocessor interface elements on Side 2. These control inputs are the Write Enable (WE) of the input register, Output Latch Enable (OLE) and Read Enable (RE) of the output latch, and port Output Enable (OE) of the bus port transceiver. User-defined logic within these Control Macrocells may be a function of any signals within the 80-input Control Array, which consists of true and complement feedback signals from the buffered outputs of the input register on the same side (16) as well as signals in the GIA (64).

In situations where minimum skew is desired, the Control Macrocells may be augmented. In this case, fast strobing comes from dedicated input pins of the EPB1400. Pin 25 (/CWS) and Pin 36 (/CRS) provide a fast write strobe and a fast read strobe for the input registers, output latches and bus transceiver port. In addition, Pins 14 and 7 (CLK1 and CLK2) may act as fast clocks for the output latches.

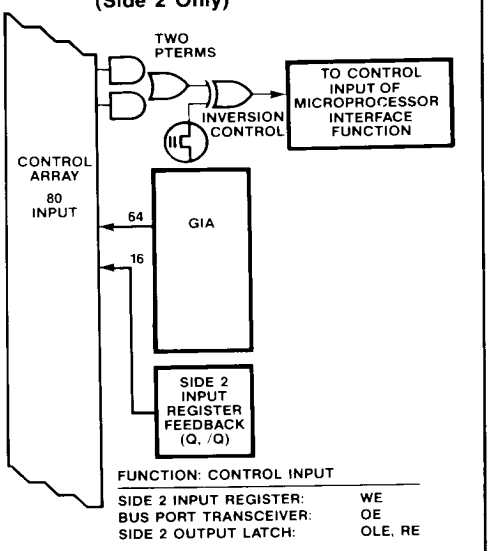
INTERNAL BUS

The 8-bit internal bus forms a highway for communication between the input registers, output latches, and the transceiver port. During normal operation, data passes from the transceiver port to the input register, or from the output latch through the transceiver to the external bus. Data from an output latch may also feed the input register. On-chip bus arbitration circuitry resolves bus contention.

MICROPROCESSOR INTERFACE FUNCTIONS

The Microprocessor Interface Block is equipped with 2 input registers, 2 output registers and the bus port transceiver. Customized peripheral functions are made possible by user-configurable options within these elements. For example, an input register may be configured as an edge-triggered register or as a flow-through latch. Data inputs for the input register may come from a set of input pins or from data off the internal bus. Read, write and output control inputs for each byte-wide element may come from user-defined logic functions in a Control Macrocell as well as pin strobes.

Figure 4. Control Macrocell Architecture (Side 2 Only)

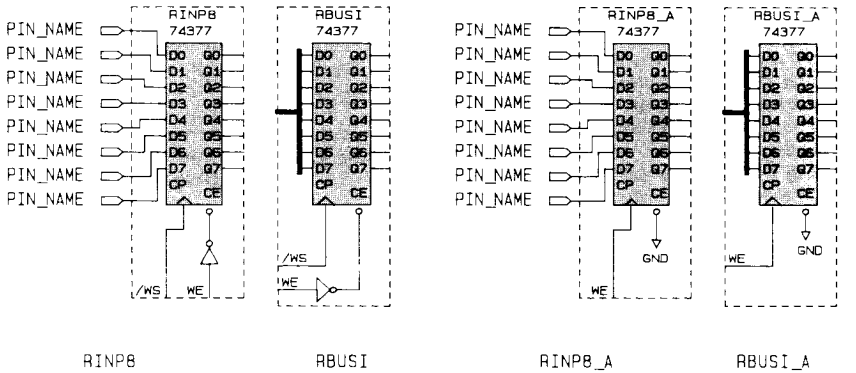


The Microprocessor Interface Functions shown in Figure 5 provide access to the different configurations for the input registers, output latches and bus port transceiver. Definitions for each function are given in Table 1.

During the design entry phase, the Microprocessor Interface Functions are accessed via functions represented by the graphic symbols shown in Figure 5. These 8 functions, along with over 100 standard SSI/MSI functions, are contained in the Altera TTL MacroFunction Library. All functions within this library may be used with the EPB1400.

Complete function tables as well as timing waveforms for each Microprocessor Interface Function are given in Figure 15A through Figure 15F. A brief description with design guidelines follows.

Figure 5. EPB1400 Microprocessor Interface Functions



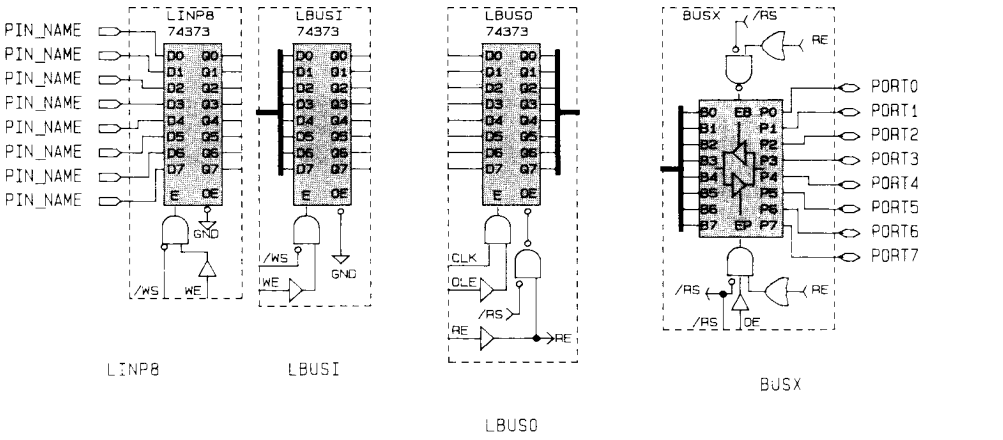


Table 1.

R = REGISTERED (edge-triggered)
L = LATCH (flow-through)

RINP8	8-Bit Input Register(74377) Input from External Pins
RBUSI	8-Bit Input Register(74377) Input from Internal Bus
RINP8_A	8-Bit Input Register(74377) Input from External Pins No Write Strobe (WS)
RBUSI_A	8-Bit Input Register(74377) Input from Internal Bus No Write Strobe (WS)
LINP8	8-Bit Input Latch(74373) Input from External Pins
LBUSI	8-Bit Input Latch(74373) Input from Internal Bus
LBUSO	8-Bit Output Latch(74373) Output to Internal Bus
BUSX	Bus Transceiver(74245) Output to Bus Port Input to Internal Bus

INPUT REGISTERS/LATCHES

RINP8 and RBUSI are edge-triggered input registers similar to the 74377. Fast pin strobing is implemented by connecting the /WS input of the function to the /CWS input pin. The WE control input to the function comes from a user-defined logic function (i.e. a Control Macrocell) and acts as a clock enable input to the registers. I/O pins are the data source for the RINP8 function, while the internal bus is the data source for RBUSI.

Truth tables for the RINP8 and RBUSI functions are shown in Figures 15A and 15B.

RINP8_A and RBUSI_A are also edge-triggered input registers based on the 74377 (similar to RINP8 and RBUSI). No pin strobes are used. Clocking is based solely on the WE control input, which is derived from a user-defined logic function. Triggering occurs on the rising edge of the WE signal. I/O pins are the source for the RINP8_A function, while the internal bus is the source for RBUSI_A.

Truth tables for the RINP8_A and RBUSI_A functions may be derived from Figures 15A and 15B for cases where /WS is not connected. (/WS=NC)

LINP8 and LBUSI are flow-through input latches similar to the 74373. Fast pin strobing is achieved by connecting the /WS control input of the function to the /CWS input pin. If pin strobing is not desired, the /WS control input is connected to an internal ground source. The WE control input of the function comes from a Control Macrocell. These latches pass data when /WS is low and WE is high. I/O pins are the source for the LINP8 function, while the internal bus is the source for LBUSI.

Truth tables for the LINP8 and LBUSI functions are shown in Figures 15C and 15D.

DESIGN GUIDELINES FOR INPUT REGISTERS

The /CWS input pin may always be used as a general purpose input to the GIA. When the /CWS pin is used as a strobe to one input register, then it must also be used as a strobe by the other input register.

When an input register configuration is chosen that uses I/O pins as the data source (RINP8, RINP8_A, or LINP8), the designer may select one of two sets of I/O pins to be used as the D0-D7 inputs for that input register. The two sets of I/O pins are IOB1_0 through IOB1_7 and IOB2_0 through IOB2_7 (see pin connection diagram for pin numbers). If both input registers are configured to have I/O pins as sources, then both sets of I/O pins will be used in that manner. When the designer does not specify which set of I/O pins should be used for a given input register, the A+PLUS software will automatically fit the design, providing complete placement of resources based on circuit interconnectivity. If the input register is placed on Side 1 of the Microprocessor Interface Block, then IOB1_0 through IOB1_7 will directly feed D0-D7 of the input register. For Side 2, IOB2_0 through IOB2_7 will be used.

OUTPUT LATCHES

LBUSO is a flow-through output latch similar to the 74373. The latch enable is based on an AND function of two control inputs, the latch Clock (CLK) and the Output Latch Enable (OLE). Fast pin strobing is implemented by connecting the CLK input of the function to the CLK1 or CLK2 pin. When the CLK input is left unconnected, it is defaulted to an internal VCC source. The OLE input to the function is used to enable the CLK input. OLE is derived from a Control Macrocell. If pin strobing is not used for the CLK input, then the OLE input provides complete latch control.

Output control of LBUSO is an AND function of two signals, the complement of an active-low Read Strobe (complement of /RS), and Read Enable (RE). The /RS is active when pin strobing is used on the bus port transceiver (BUSX). In this case, the /RS control input of the BUSX function is connected to the /CRS pin. Under these conditions, the RE input to the AND gate of LBUSO acts as an enable signal for the /RS signal. The RE input is derived from a Control Macrocell. When the bus port transceiver does not use pin strobing, the /RS signal defaults to an internal ground connection. Under these conditions, the RE control input to LBUSO has complete control over the output enable function for the output latch.

A truth table of the LBUSO function is shown in Figure 15E.

DESIGN GUIDELINES FOR OUTPUT LATCHES

When the CLK control input of one output latch is used for pin strobing from the CLK1 pin and the remaining output latch uses pin strobing, then the CLK control input of the remaining output latch must be connected to the CLK2 pin. Whenever pin strobes are not used, the CLK control input of the output latch defaults to an internal VCC connection. The CLK1 and CLK2 input pins may always be used as general purpose inputs to the GIA. In addition, the CLK1 and CLK2 pins may be used as clock signals for the General Purpose Macrocells on Side 1 and Side 2, respectively.

The /RS control input is common among both output latches and the bus port transceiver. When pin strobing is used, the /RS control input must be connected to the /CRS pin. Like other pin strobes, the /CRS input pin may always be used as a general purpose input to the GIA. OLE and RE come from Control Macrocells and are independent of other control functions.

The RE input to LBUSO may affect the RE input to BUSX (bus transceiver). For possible implications, please see Design Guidelines for Bus Port Transceiver.

The data source of an output latch is determined by the connections to the D0-D7 inputs of the output latch. As shown in Figure 3, the D0-D7 connections come from one of two possible sources: 1) internal (buried) feedback from a group of General Purpose Macrocells (Bus I/O type) within the Programmable Logic Core Block, or 2) external (from the I/O pin) feedback from the same set of macrocells. In addition to choosing internal or external macrocell feedback, the designer may specify which group of Bus I/O Macrocells should be fed to an output latch. If the group of Bus I/O Macrocells is on Side 1 of the EPB1400, then the D0 to D7 inputs to the output latch will come from feedback signals derived in Macrocell 10 to Macrocell 3, respectively. Similarly, Macrocell 18 through Macrocell 11 are used when Side 2 is specified. These macrocells are called Bus I/O Macrocells because their feedback signals are routed on buses to byte-wide elements within the Microprocessor Interface Block. If no specifications are made, A+PLUS software invokes its automatic fitting algorithm to fit the design.

BUS PORT TRANSCEIVER

BUSX is similar to the 74245 bi-directional bus transceiver. Directional control over the transceiver is achieved by logic functions that are based on control inputs to the BUSX function. A three-input AND gate enables data from the internal bus to pass to the external port. Inputs to this AND gate consist of the following control signals: 1) an active-low Read Strobe (/RS); 2) an Output Enable signal (OE); and 3) a Read Enable input (RE). The /RS control input to the BUSX function is connected to the /CRS pin for pin strobing. Otherwise, the unconnected /RS control input defaults to an internal ground connection. The OE control input is derived within a Control Macrocell. The RE signal is the logical OR of the RE inputs related to the LBUSO output latch functions used in the design. When /RS,OE and RE take on the logic levels Low, High and High respectively (a read operation), data will be passed from the internal bus to the external microprocessor bus.

A two-input NAND gate controls data transmission from the external microprocessor bus to the internal bus of the EPB1400. The control inputs to this NAND gate are /RS and RE. When /RS is at a high logic level or RE is at a low logic level (no read operation), then data from the external bus port will be transferred to the internal bus.

A truth table for the BUSX function is shown in Figure 15F.

DESIGN GUIDELINES FOR BUS PORT TRANSCEIVER

In order to guarantee proper Read operation and avoid bus contention, the RE input to the bus port transceiver cannot be connected directly to the BUSX function. Instead, the RE input to BUSX is the logical OR function of the RE inputs on LBUSO functions. This avoids simultaneous transfer of data to the internal bus by both the bus transceiver and either output latch.

Figure 3 details the Programmable Logic Core Block. General Purpose Macrocells allow the implementation of user-defined mixes of combinatorial and sequential logic functions such as address decoding, interrupt logic and state machines.

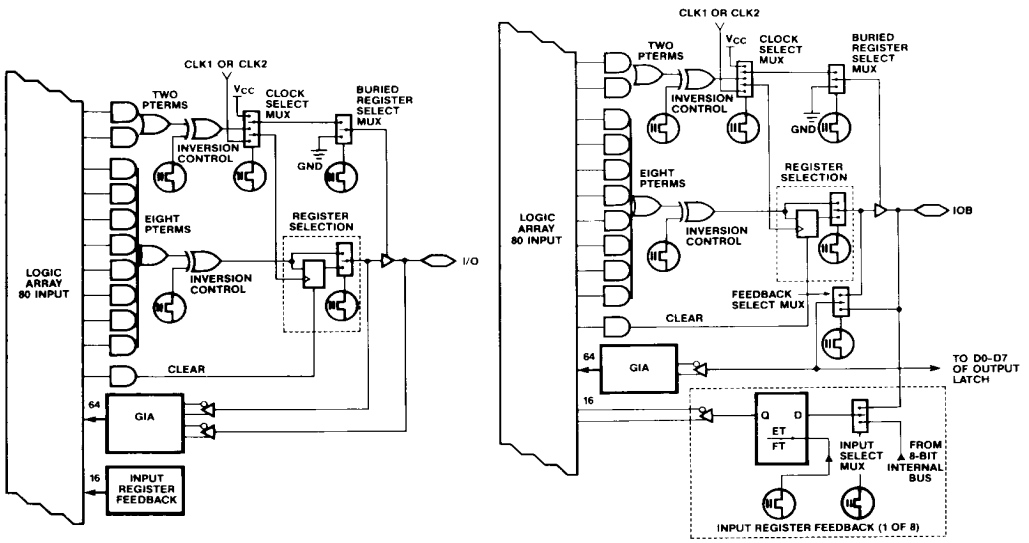
GENERAL PURPOSE MACROCELLS

A total of 20 General Purpose Macrocells, 10 located on each side, are contained within the Programmable Logic Core Block. All General Purpose Macrocells are fed by an 80-input logic array; 64 of the array signals come from the GIA while the remaining 16 come from an input register within the Microprocessor Interface Block. The 64 array signals from the GIA are comprised of the true and complement form of all dedicated input pins (16), all General Purpose Macrocell internal feedback signals (40) and all external Generic I/O Macrocell feedback signals (8). As a result, each product term is equivalent to an 80-input AND gate.

Within each group of General Purpose Macrocells, there are two types of macrocells, Generic I/O and Bus I/O. Each side has 2 Generic I/O Macrocells and 8 Bus I/O Macrocells. Figure 6A shows the composition of the Generic I/O Macrocell. Figure 6B shows the Bus I/O Macrocell.

Common features among the Generic I/O and Bus I/O Macrocells include programmable flip-flop

Figure 6A, 6B. General Purpose Macrocell Architecture



(A) Generic I/O Type **(B) Bus I/O Type**

options, programmable clock/OE options and programmable register clear functions. Both macrocell types may be configured as D,T,JK or SR flipflops. Flip-flop selection may be bypassed for purely combinatorial outputs. The programmable clock feature allows selection of either a dedicated clock pin (CLK1 or CLK2) or a user-defined logic function to clock the macrocell flip-flop. The logic resources allocated for this user-definable clock signal accommodate up to 2 product terms with optional inversion control. This function is shared by the output enable (OE) function of the macrocell. As a result, if either CLK1 or CLK2 is used to clock the flip-flop, then the 2 product term logic network is used for the programmable OE function. Conversely, when the 2 product term network is used for clocking of the flip-flop, then OE must be attached to either VCC or GND, corresponding to a permanently enabled output or a buried register. One independent product term is used to perform an asynchronous clear function on the flip-flop. When the Clear product term goes to a high level, the Q output of the macrocell goes to a low level, independent of the flip-flop clock.

Both types of macrocells also contain a dual feedback feature. Dual Feedback allows a macrocell to be used internally for buried functions while the associated macrocell pin is used as an input pin. The distinction between Generic I/O and Bus I/O Macrocells is related to the destination of these dual feedback signals.

The 4 Generic I/O Macrocells (2 on each side) contain internal and external feedback to the GIA. They are not used as direct data inputs to byte-wide resources in the Microprocessor Interface Block. However, the 16 Bus I/O Macrocells (8 on each side) contain feedback that can act as inputs to the GIA and byte-wide inputs to the Microprocessor Interface Block. The diagram in Figure 6B shows that the designer has the option to choose between internal feedback or external feedback from Bus I/O Macrocells via a Feedback Select Mux. Once chosen, the feedback signals may act as inputs to the GIA as well as the D0 to D7 inputs for the output latch on the same side as the Bus I/O Macrocells. In addition, the external feedbacks (pins IOB1_0 through IOB1_7 or pins IOB2_0 through IOB2_7) may act as the D0 through D7 inputs to the input register on the same side.

ADDITIONAL BURIED REGISTERS

Applications which do not employ both input registers or both output latches in the Microprocessor Interface Block may use the unused elements as buried registers. The 8-bit internal data bus transports data from the output latches to input registers. The input registers pass bytes of data which are accessed in true and complement form by Control Macrocells and General Purpose

Macrocells. Applications which do not use any of the input or output latches can tap up to 32 additional buried register bits. Control over these additional buried registers is maintained through the use of independently programmable Control Macrocells.

Pipelining operations are also made possible. Single stage pipelining uses either a vacant input register or vacant output latch as an 8-bit buried register. For double stage pipelining, data may be clocked in both the output latch and input register, each of which may be converted to an 8-bit buried latch or register.

The bus port transceiver can be transformed into 8 additional input pins. In normal use, the port transceiver passes data from an external port to the internal bus where it may feed the input registers in the Microprocessor Interface Block. Therefore, data can be taken from the 8 port pins (PORT0-PORT7), pass through a flow-through latch, and ultimately access logic arrays used by Control Macrocells and General Purpose Macrocells.

EPB1400 DESIGN SUPPORT — A+PLUS

Complete CAE/CAD support for EPB1400 designs is provided through Altera Programmable Logic User Software (A+PLUS). This provides a PC-based development environment which permits a variety of design entry options, performs automatic logic minimization and design fitting, and produces an object code device programming file. In addition, functional verification of designs is possible through the use of simulation tools.

EPB1400 designs may be entered using schematic capture, state machine entry or traditional Boolean equation entry formats. A mixture of these input mechanisms is accepted by the A+PLUS design processor.

The Altera LogiCaps Schematic Capture package provides an efficient and simple to use entry method for design of the EPB1400. Macrofunction libraries access over 100 popular TTL SSI/MSI functions as well as the 8 microprocessor interface functions shown in Figure 5. LogiCaps features 10 levels of zoom, split-screen capability, real-time orthogonal rubberbanding, user-definable macro definition with optional tail-end recursion, bus and multi-page support.

Designs may also be entered using a high level state machine input language. This format uses IF_THEN_ELSE constructs as well as a mixture of truth tables and Boolean expressions.

Design processing is automatic. The A+PLUS design processor performs macrofunction reduction and decomposition (MacroMunching), complete logic minimization, and design fitting. The design processor consists of translator, minimizer, and fitter modules. The Translator performs design rule checking for logical consistency and completeness. The Minimizer uses artificial intelligence techniques that allow for complete logic reduction, resulting in full optimization of EPLD resources. The Fitter matches the design requirements with the EPLD resources, then intelligently assigns pin numbers which satisfy all internal connections. The end result is an industry standard JEDEC file which can act as an input to simulation software for complete functional verification of the design. Once simulation is complete, the JEDEC file is used to program the EPB1400 with programming software and hardware available to support all Altera development system options.

CALCULATING DELAY PATHS

A timing model for the Programmable Logic Core Block is shown in Figure 7 and associated waveforms are shown in Figure 8. Timing of external paths is given in Figure 9. Additional parametric relationships are shown in Figures 10A and 10B as well as in Figures 11A and 11B. Delay paths related to the Microprocessor Interface Functions are shown in Figure 15A through Figure 15F.

To calculate path delays within the Programmable Logic Core Block, begin at the start of the path in Figure 7 and follow the path to its completion, summing the delay of each block traversed by the path. For example, Figure 10A calculates the delay from input to combinatorial output (T_{PD}). T_{PD} is obtained by starting at the input pin, traversing the logic array, and exiting from the output pin. From this path, T_{PD} becomes the sum of the input delay (t_{IN}), the logic array delay (t_{LAD}) and the output delay (t_{OD}). Parameters related to registers are not taken into account for a combinatorial function. Figure 10B shows the calculation of T_{CNT}.

Delay paths that traverse the Microprocessor Interface Block must use the delay components noted in Figure 15A through Figure 15F. The sample calculation in Figure 11A shows the delay necessary to read data from an output latch into the bus port after the /CRS signal (T_{RSD}).

Delay paths that involve both the Microprocessor Interface Block and the Programmable Logic Core Block may also be calculated. The calculation in Figure 11B determines the delay necessary to write data to the input register (based on the /CWS strobe), then have that data appear on a combinatorial output.

FUNCTIONAL TESTING

Functional and parametric operation of the EPB1400 is guaranteed through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. The erasable nature of the EPB1400 allows test program patterns to be used and then erased.

Figure 7. Programmable Logic Core Block Delay Paths

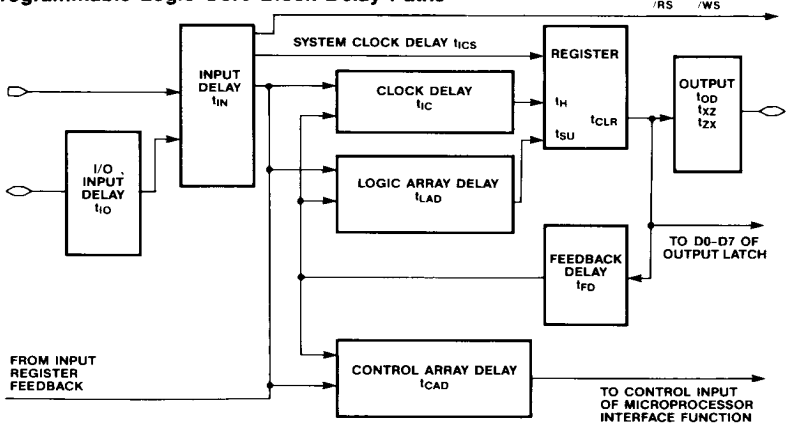
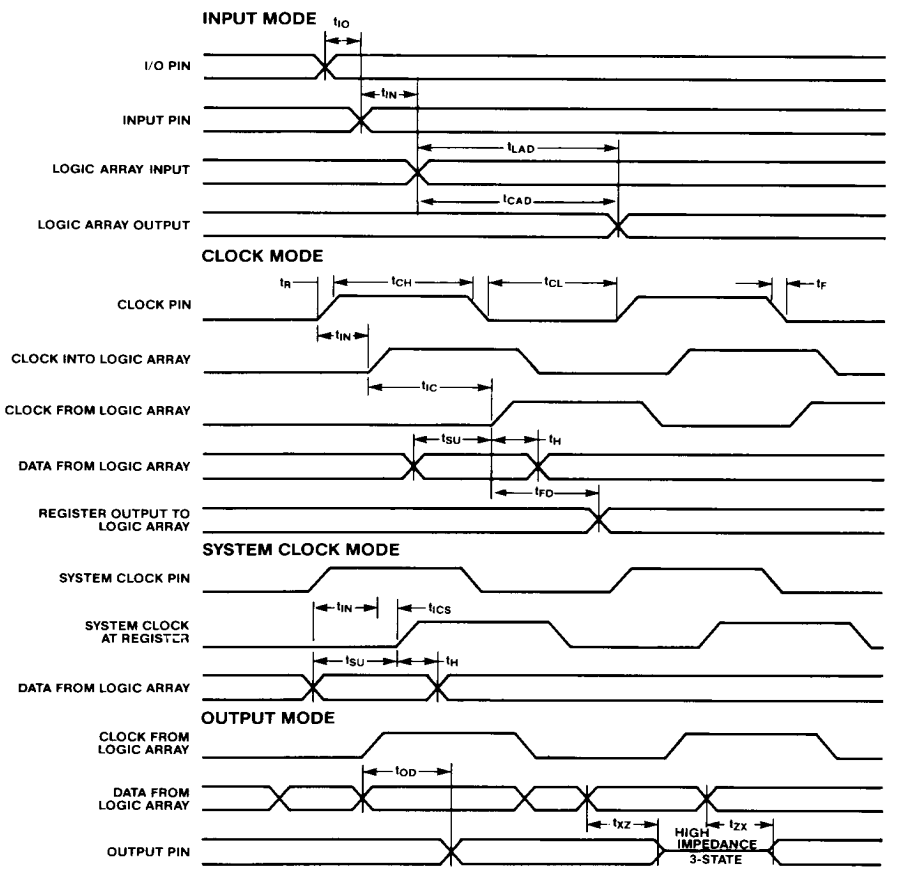


Figure 8. Switching Waveforms



ABSOLUTE MAXIMUM RATINGS

COMMERCIAL
OPERATING RANGE

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-550	+550	mA
I_{OUT}	DC OUTPUT current, per I/O pin		-25	+25	mA
I_{OUT}	DC OUTPUT current, per Bus Port pin		-50	+50	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
T_R	INPUT rise time	note (6)		250	ns
T_F	INPUT fall time	note (6)		250	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
Note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OH}	HIGH level TTL output voltage (Bus Port)	I_{OH} = -4mA DC	2.4			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.50	V
V_{OL}	LOW level output voltage (Bus Port)	I_{OL} = 24mA DC			0.50	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC3}	V_{CC} supply current	V_I = V_{CC} or GND No load, f = 1.0MHz note (5)		70	100	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{PORT}	Bus Port Pin Capacitance	V_{OUT} = 0V f = 1.0 MHz		15	pF
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		15	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		15	pF

AC CHARACTERISTICS

EPB1400-2, EPB1400

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)

			EPB1400-2			EPB1400			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency	note (7)	40.0			31.2			MHz
t_{IN}	Input pad and buffer delay				4			5	ns
t_{IO}	I/O input pad and buffer delay				5			7	ns
t_{LAD}	Logic Array delay				20			25	ns
t_{CAD}	Control Array delay				16			18	ns
t_{OD}	Output buffer and pad delay	C_1 = 35pF (Fig 12)			11			15	ns
t_{ZX}	Output buffer enable				15			20	ns
t_{XZ}	Output buffer disable	C_1 = 5pF note (2)			15			20	ns
t_{SU}	Register set-up time		10			12			ns
t_{HS}	Register hold time (system clock)		0			0			ns
t_H	Register hold time		10			12			ns
t_{CH}	Clock high time		12			16			ns
t_{CL}	Clock low time		12			16			ns
t_{IC}	Clock delay				20			25	ns
t_{ICS}	System clock delay				5			5	ns
t_{FD}	Feedback delay				3			4	ns
t_{CLR}	Register clear time				25			30	ns
t_{CNT}	Minimum clock period (register output feedback to register input-internal data)				33			40	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (5)	30.3			25.0			MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 12, (high voltage pin during programming), has capacitance of 100pF max.
5. Measured with device programmed as a 20 bit counter.
6. Clock t_R, t_F = 25ns.
7. The f_{MAX} values shown represent the highest frequency for pipelined data.

A Military Product Drawing will be prepared, in accordance with appropriate military specification formats, to provide guidance for the preparation of Source Control Drawings (SCD).

These preliminary specifications are provided for evaluation purposes. Conservative values are shown prior to full device characterization. Please request a copy of the current EPB1400 Electrical Specification for complete information.
A Military Product Drawing will be prepared, in accordance with appropriate military specification formats, to provide guidance for the preparation of source control drawings (SCD).

Figure 9. External Timing Paths

SYMBOL	PARAMETER	CONDITIONS	EPB1400-2			EPB1400			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{WSQ}	/CWS to input register output valid				10			14	ns
t_{WSD}	Bus port to /CWS setup		3			5			ns
t_{WSH}	Bus port or IOB to /CWS hold		0			0			ns
t_{RSD}	/CRS to bus port valid				20			30	ns
t_{SOV}	CLK1 or CLK2 to bus port valid	C_1 = 100pF			25			35	ns
t_{PD}	Input to non-registered output	C_1 = 35pF			35			45	ns
t_{CO1}	CLK1 or CLK2 to output				20			25	ns

Switching Waveforms

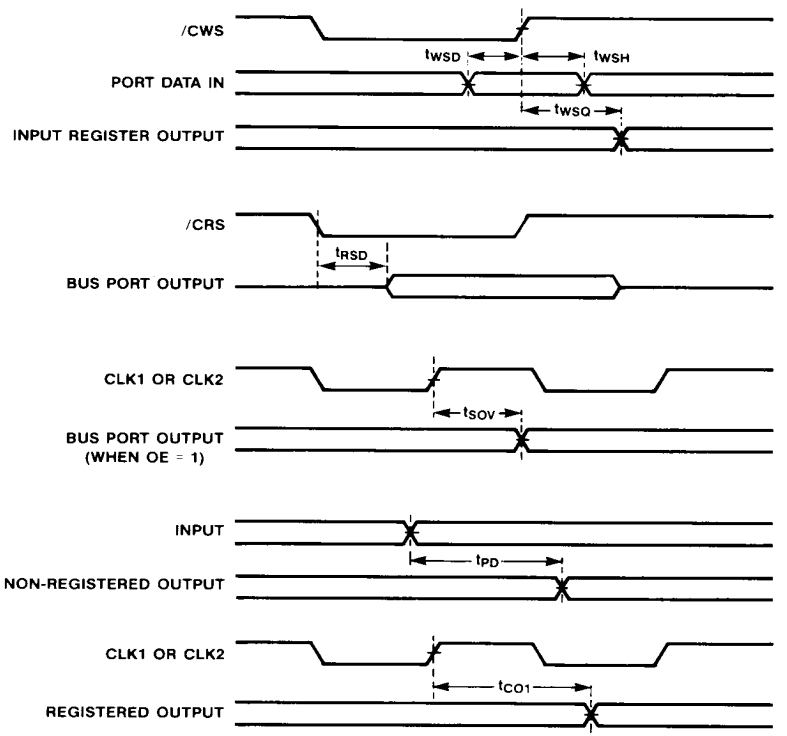
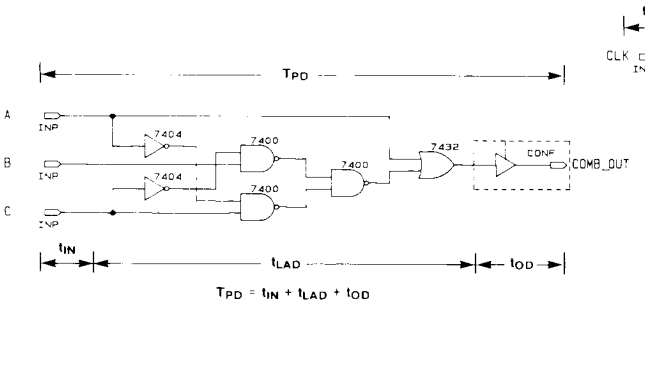
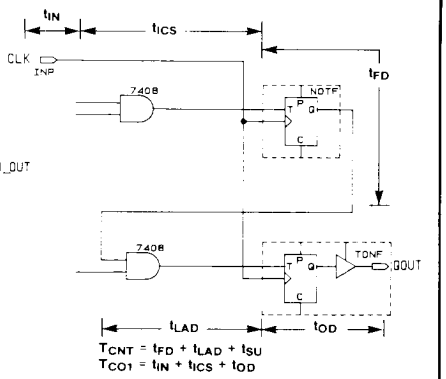


Figure 10A, 10B. Parametric Relationships within Programmable Logic Core Block

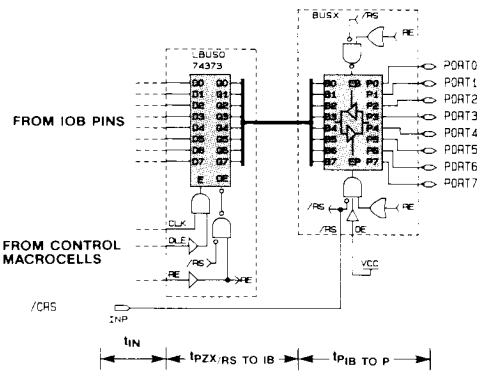


(A) T_{PD}, Delay from Input to Combinatorial Output

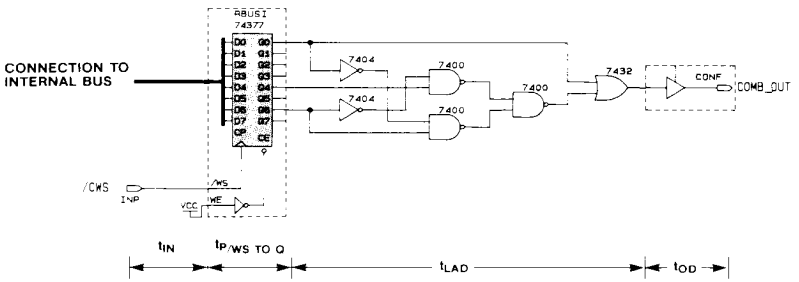


(B) T_{CNT}, Minimum Clock Period
(Delay from register output feedback to register input, on the internal path)
T_{CO1}, Delay from Clock to Output

Figure 11A, 11B. Parametric Relationships within the Microprocessor Interface Block



(A) T_{RSD}, Read Strobe Delay
(Delay to read the data from an Output Latch into the Bus Port, after the /CRS pin is asserted.)



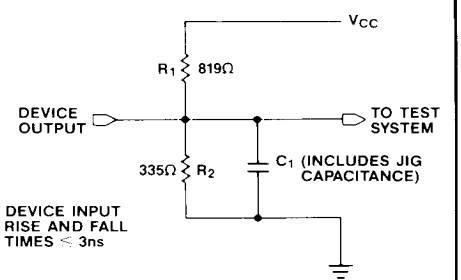
(B) Input Register Read to Combinatorial Output
(Delay from the time the /CWS pin is asserted to the time a combinatorial output is valid.)

This ability to perform application-independent, general purpose tests is called Generic Testing and is unique to erasable, user-configurable logic devices. Non-windowed, OTP versions of the EPB1400 combine erasable testing cycles at the wafer level with special on-chip test circuitry, used after packaging, to achieve 100% programming yield.

DESIGN SECURITY

The EPB1400 contains a programmable design security feature that controls access to data programmed into the device. If this programmable feature is used, the custom pattern in the device is free from interrogation or reverse engineering since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the device.

Figure 12. AC Test Conditions

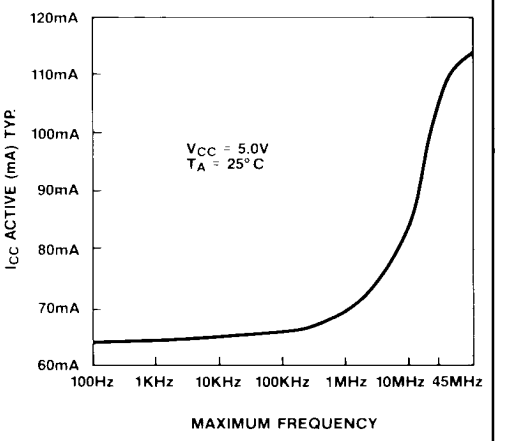


Power supply transients can affect AC measurements; simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity. Bus port measurements should use R_1 and R_2 values of 159Ω and 118Ω, respectively, with C_1 = 100pF.

PROGRAM ERASURE

Erasure of the programmed connections in the EPB1400 begins to occur on exposure to light wavelengths shorter than 4000 Angstroms. Note that sunlight and certain fluorescent lighting can erase a programmed EPB1400 since they have wavelengths in the range of 3000 to 4000 Angstroms. Constant exposure to room level fluorescent lighting could erase an EPB1400 in approximately 3 years. Direct sunlight could cause erasure in approximately 1 week. If the EPB1400 is to be exposed to these conditions for extended periods of time, an opaque label should be placed over the window.

Figure 13. I_{CC} vs F_{MAX}



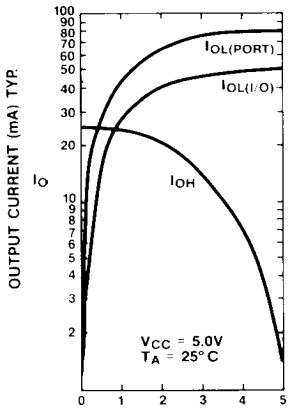
The recommended erase procedure for the EPB1400 is exposure to shortwave ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for erasure should be a minimum of 30Wsec/cm². The erasure time with this dosage is approximately 45 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The EPB1400 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated exposure dose for an EPB1400 without damage is 7000 Wsec/cm². This is approximately one week at 12000 μW/cm². Exposure of the EPB1400 to high intensity UV light for long periods of time may cause permanent damage.

The EPB1400 may be erased and re-programmed as many times as needed using the recommended erasure exposure levels.

LATCH-UP & ESD PROTECTION

EPB1400 input, I/O, and clock pins have been designed to resist electro-static discharge (ESD) and latch-up damage. Each of the EPB1400 pins will withstand voltage energy levels exceeding those specified by MIL STD 883C. EPB1400 pins will not latch-up for input voltages between -1V to VCC+1V with currents up to 100mA. During transitions the inputs may undershoot to -2.0V for periods less than 20ns. Additionally, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

Figure 14. Output Drive Currents



DESIGN RECOMMENDATIONS

Operation of devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The EPB1400 contains circuitry to protect inputs against high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

For proper operation, it is recommended that an opaque labels be placed over the device window. Input and output pins must be constrained to the range GND $<$ (V_{IN} or V_{OUT}) $<$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .2μF must be connected between V_{CC} and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

PACKAGE OUTLINES

Package outlines for the EPB1400 40 Pin DIP and 44 Pin JLCC/PLCC packages are shown in the Altera 1987 Databook, pages 4-17 and 4-18.

DEVELOPMENT SYSTEM REQUIREMENTS

The recommended development environment for design of the EPB1400 is the Altera PLCAD-SUPREME EPLD Development System. PLCAD-SUPREME includes all modules within the A+PLUS Software (version 5.0 or later release required for support of the EPB1400) as well as the LogiCaps Schematic Capture Package, macrofunction libraries, a functional simulator, a master programming module and selected adapters. In addition, a PLED1400 or PLEJ1400 device adapter must be purchased to support the EPB1400 device. For more information concerning development systems, please contact Altera Corporation.

The recommended system requirements for the Altera PLCAD-SUPREME Development System are as follows:

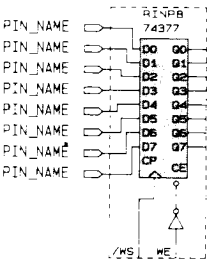
- IBM XT, AT or compatible computers
- CGA, EGA (with extended memory), or Hercules Graphics Adapter
- 640 KBytes RAM
- 10 Mbyte hard disk drive and 5¼ inch floppy drive
- DOS version 3.1 or later release
- 3-Button serial Mouse, Logitech LogiMouse (model C7) or Mouse Systems PC Mouse. Connects to serial port of computer.

Figure 15A. RINP8—Input Register, Data from IOB Pins

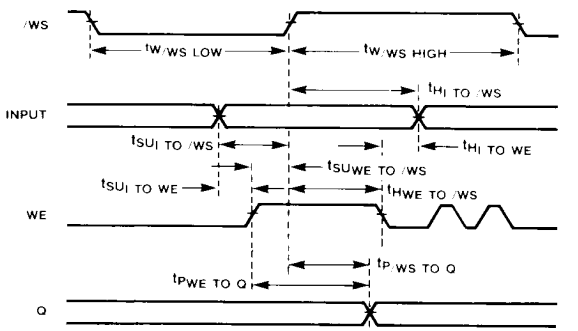
Truth Table

/WS	WE	I	Q	Q*
↑	H	L	X	L
↑	H	H	X	H
H	X	X	L	L
H	X	X	H	H
L	X	X	L	L
L	X	X	H	H
NC [1]	↑	L	X	L
NC [1]	↑	H	X	H

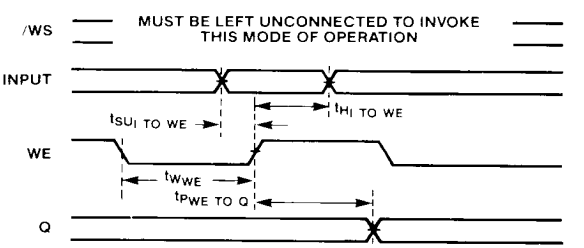
[1] When /WS is not connected (/WS = NC), operation reflects the RINP8_A function.



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_W	Pulse duration of /WS high	30			40			ns
	Pulse duration of /WS low	10			15			ns
	Pulse duration of WE	10			15			ns
t_{SU}	Input to /WS	12			17			ns
	WE to /WS	6			10			ns
	Input to WE	15			19			ns
t_H	Input to /WS	0			0			ns
	WE to /WS	6			8			ns
	Input to WE	0			0			ns
t_P	/WS to Q			6			9	ns
	WE to Q			10			12	ns



MODE 1: WRITE STROBE USED



MODE 2: WRITE STROBE NOT USED

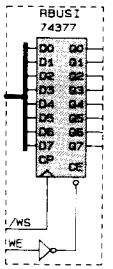
Figure 15B. RBUSI—Input Register, Data from Internal Bus

Truth Table

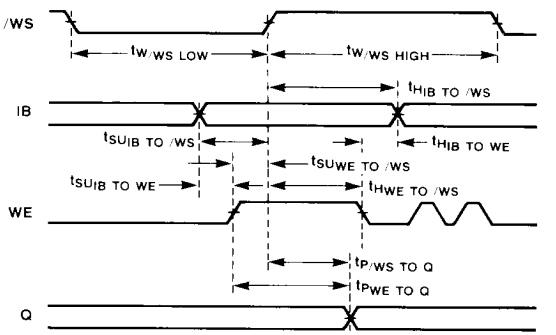
/WS	WE	IB	Q	Q+
↑	H	L	X	L
↑	H	H	X	H
H	X	X	L	L
H	X	X	H	H
L	X	X	L	L
L	X	X	H	H
NC [1]	↑	L	X	L
NC [1]	↑	H	X	H

IB—INTERNAL BUS

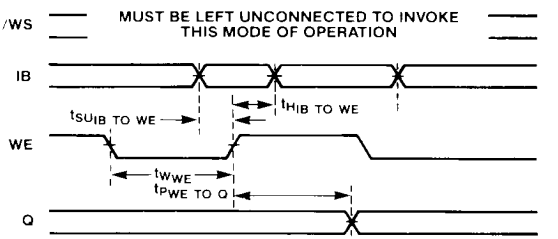
[1] When /WS is not connected (/WS = NC), operation reflects the RBUSI_A function.



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_W	Pulse duration of /WS high	30			40			ns
	Pulse duration of /WS low	10			15			ns
	Pulse duration of WE	10			15			ns
t_{SU}	Internal Bus to /WS	3			5			ns
	WE to /WS	6			10			ns
	Internal Bus to WE	6			7			ns
t_H	Internal Bus to /WS	0			0			ns
	WE to /WS	6			8			ns
	Internal Bus to WE	2			7			ns
t_P	/WS to Q			6			9	ns
	WE to Q			10			12	ns



MODE 1: WRITE STROBE USED

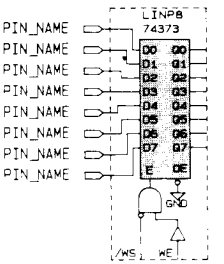


MODE 2: WRITE STROBE NOT USED

Figure 15C. LINP8—Input Latch, Data from IOB Pins

Truth Table

/WS	WE	I	Q	Q^+
L	H	L	X	L
L	H	H	X	H
H	X	X	L	L
H	X	X	H	H
X	L	X	L	L
X	L	X	H	H



		EPB1400-2			EPB1400			
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_W	Pulse duration of /WS high	30			40			ns
	Pulse duration of /WS low	15			20			ns
	Pulse duration of WE	15			20			ns
t_{SU}	Input to /WS	14			20			ns
	WE to /WS	9			12			ns
	Input to WE	15			19			ns
t_H	Input to /WS	0			0			ns
	WE to /WS	9			12			ns
	Input to WE	0			0			ns
t_P	/WS to Q			8			12	ns
	WE to Q			10			14	ns
	Input to Q			19			22	ns

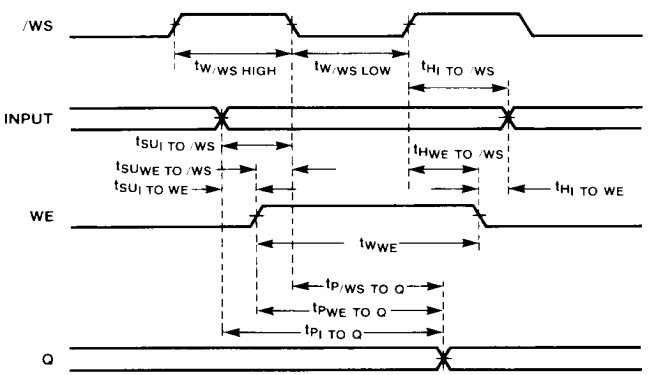
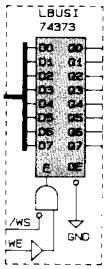


Figure 15D. LBUSI—Input Latch, Data from Internal Bus

Truth Table

/WS	WE	IB	Q	Q^+
L	H	L	X	L
L	H	H	X	H
H	X	X	L	L
H	X	X	H	H
X	L	X	L	L
X	L	X	H	H

IB—INTERNAL BUS



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_W	Pulse duration of /WS high	30			40			ns
	Pulse duration of /WS low	15			20			ns
	Pulse duration of WE	15			20			ns
t_{SU}	Internal Bus to /WS	5			8			ns
	WE to /WS	9			12			ns
	Internal Bus to WE	6			7			ns
t_H	Internal Bus to /WS	0			0			ns
	WE to /WS	9			12			ns
	Internal Bus to WE	2			7			ns
t_P	/WS to Q			8			12	ns
	WE to Q			10			14	ns
	Internal Bus to Q			10			10	ns

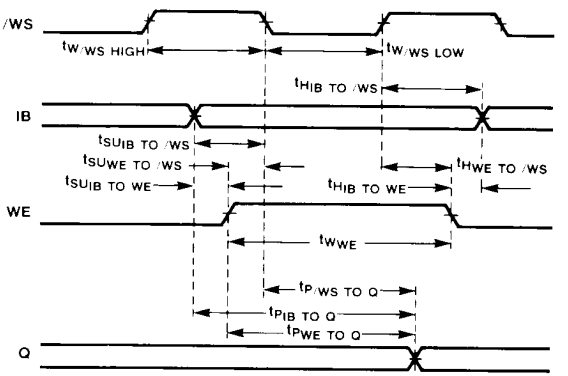
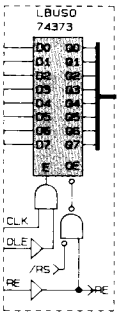


Figure 15E. LBUSO—Output Latch



Truth Tables

CLK	OLE	D	Q	Q^+
H	H	H	X	H
H	H	L	X	L
L	X	X	H	H
L	X	X	L	L
X	L	X	H	H
X	L	X	L	L

/RS	RE	Q	IB
L	H	H	H
L	H	L	L
X	L	X	Z
H	X	X	Z

IB—INTERNAL BUS

		EPB1400-2			EPB1400			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_W	Pulse duration of CLK	12			16			ns
	Pulse duration of OLE, RE	10			15			ns
	Pulse duration of /RS	10			15			ns
t_{SU}	Data to CLK	8			12			ns
	OLE to CLK	9			11			ns
	RE to /RS	7			8			ns
t_H	Data to CLK	2			2			ns
	OLE to CLK	8			9			ns
	RE to /RS	0			0			ns
t_P	Data to Internal Bus			4			10	ns
	CLK to Internal Bus			6			10	ns
	OLE to Internal Bus			8			11	ns
t_{PZX}	/RS to Internal Bus Valid			3			7	ns
	RE to Internal Bus Valid			8			16	ns
t_{PXZ}	/RS to Internal Bus Tri-state			3			5	ns
	RE to Internal Bus Tri-state			7			11	ns

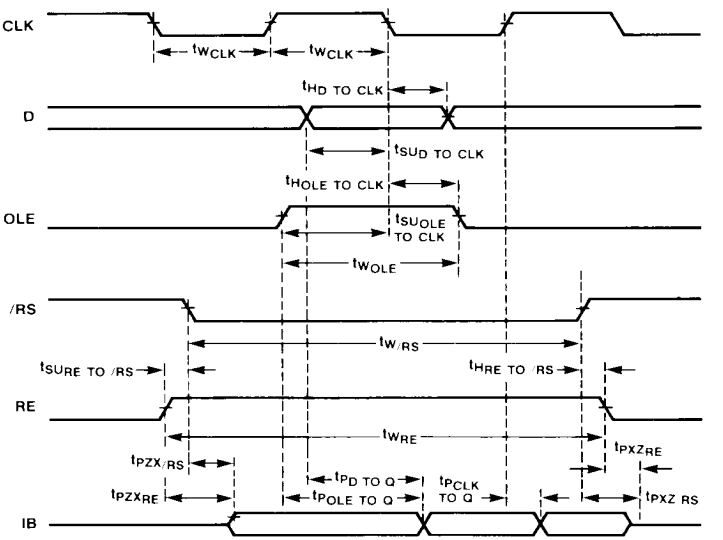
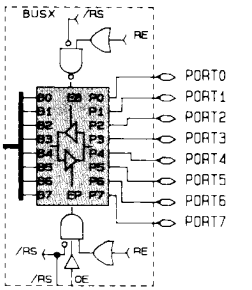


Figure 15F. BUSX—Bi-Directional Bus Port Transceiver

Truth Table

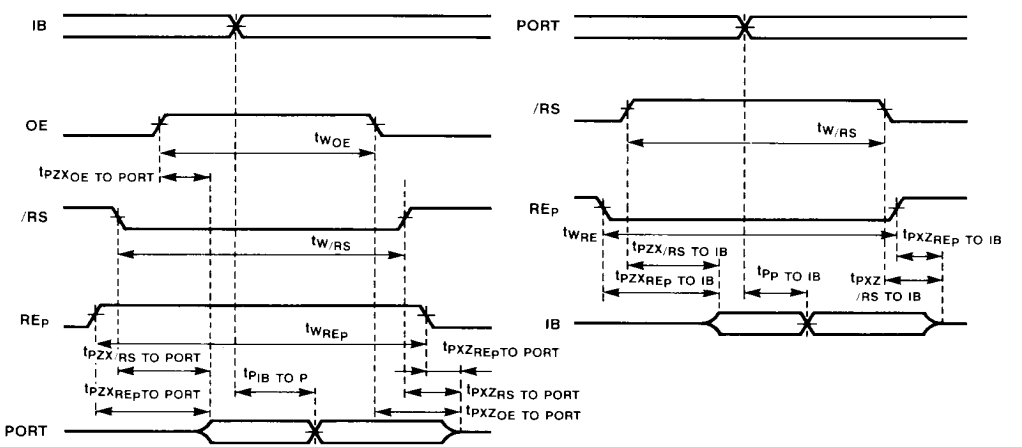
/RS	$RE_1 + RE_2$	OE	OPERATION
L	L	L	PORT DATA TO INTERNAL BUS
L	L	H	PORT DATA TO INTERNAL BUS
L	H	L	ISOLATION
L	H	H	INTERNAL BUS DATA TO PORT
H	L	L	PORT DATA TO INTERNAL BUS
H	L	H	PORT DATA TO INTERNAL BUS
H	H	L	PORT DATA TO INTERNAL BUS
H	H	H	PORT DATA TO INTERNAL BUS

RE_1 = RE FOR SIDE 1 OUTPUT LATCH
RE_2 = RE FOR SIDE 2 OUTPUT LATCH
RE_P = RE FOR THE BUS PORT, RE_P IS THE LOGICAL "OR" OF RE_1, RE_2
IB = INTERNAL BUS



SYMBOL	PARAMETER	EPB1400-2 MIN	EPB1400-2 TYP	EPB1400-2 MAX	EPB1400 MIN	EPB1400 TYP	EPB1400 MAX	UNIT
t_P	Port to Internal Bus			4			5	ns
	Internal Bus to Port			12			16	ns
t_{PZX}	/RS to Port Valid			14			22	ns
	OE to Port Valid			14			22	ns
	RE to Port Valid			14			22	ns
	/RS to Internal Bus Valid			3			7	ns
	RE to Internal Bus Valid			8			16	ns
t_{PXZ}	/RS to Port Tri-state			12			15	ns
	OE to Port Tri-state			12			15	ns
	RE to Port Tri-state			12			15	ns
	/RS to Internal Bus Tri-state			3			5	ns
	RE to Internal Bus Tri-state			7			11	ns

Note:
For parameters related to Bus Port outputs, load capacitance is 100pF. (C_1 = 100pF, Figure 12)



PRODUCT GRADES

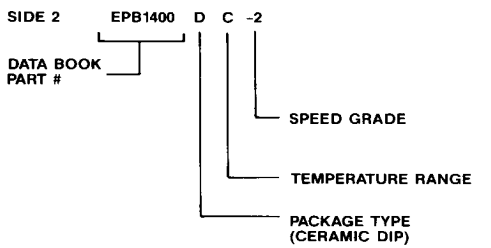
APPLICATION	TEMPERATURE RANGE	MARKING DESIG-NATOR
COMMERCIAL	0°C TO +70°C	C
AUTOMOTIVE/ INDUSTRIAL	-40°C TO +85°C	I
MILITARY	-55°C TO +125°C	M
MIL-STD-883C CLASS-B	-55°C TO +125°C	883B

Notes:
For specific package/grade/speed combinations that are available, please refer to product listings or call Altera marketing department.
(408) 984-2805 × 101

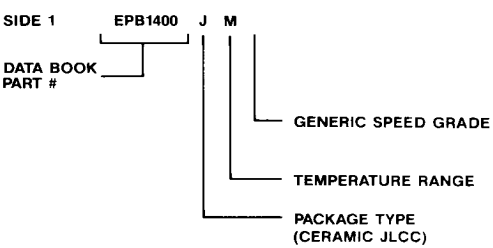
ORDERING INFORMATION

Some examples of ordering various package and electrical as well as temperature grades are given below.

a) Level-2 Product:



b) Generic Product:



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