PI49FCT3805/PI49FCT3806
PI49FCT3805A/PI49FCT3806A
PI49FCT3805B/PI49FCT3806B
PI49FCT3805C/PI49FCT3806C

3.3V Fast CMOS Buffer/Clock Driver

Features

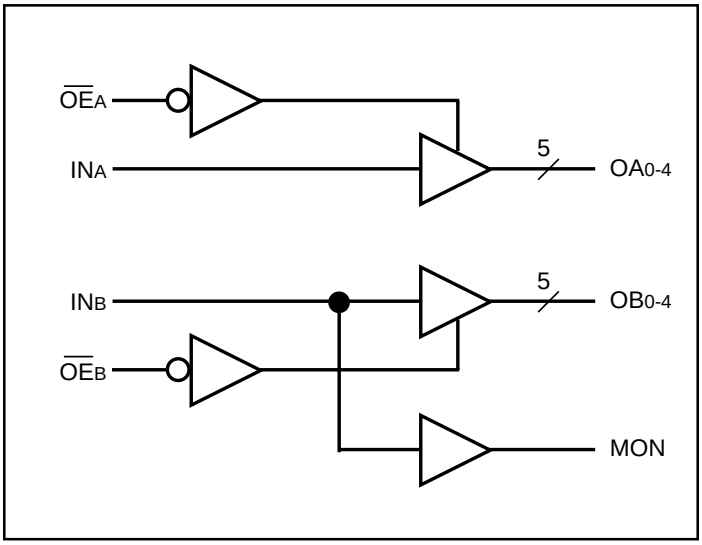
- 3.3V version of PI49FCT805/806
- Extremely low output skew: 0.5ns
- Monitor ouput pin
- Clock busing wih 3-state control
- TTL inpu and CMOS output compatible
- Industrial operation at–40°C to 85°C
- Extremely low static power (1mW, typ.)
- Hysteresis on all inputs
- Packages available:
  – 20-pin 300-mil wide SOIC (S)
  – 20-pin 150-mil wide QSOP (Q)
  – 20-pin 209-mil wide SSOP (H)
- Device models available on request

Product Description

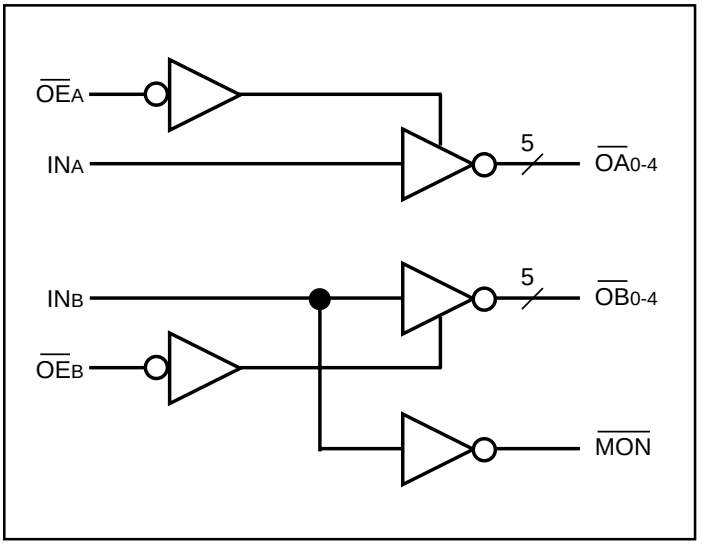
Pericom Semiconductor's PI49FCT series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed grades.

The PI49FCT3805 is a 3.3V non-inverting clock driver and the PI49FCT3806 is a 3.3V inverting clock driver designed with two independent groups of buffers. These buffers have 3-state Output Enable inputs (active LOW) with a 1-in, 5-out configuration per group. Each clock driver consist of two banks of drivers, driving five outputs each from a standard TTL compatible CMOS input.

PI49FCT3805 Logic Block Diagram



PI49FCT3806 Logic Block Diagram



Product Pin Description

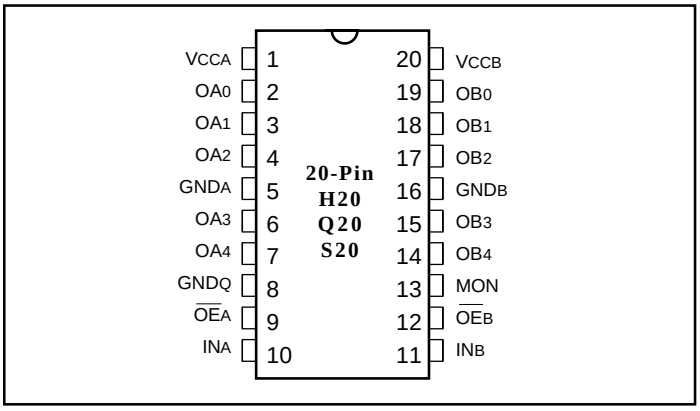
Pin Name	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_N, OB_N	Clock Outputs
MON	Monitor Output
GND	Ground
V_{CC}	Power

PI49FCT3805 Truth Table[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_N, OB_N	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

Note:
1. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance

PI49FCT3805 Product Pin Configuration

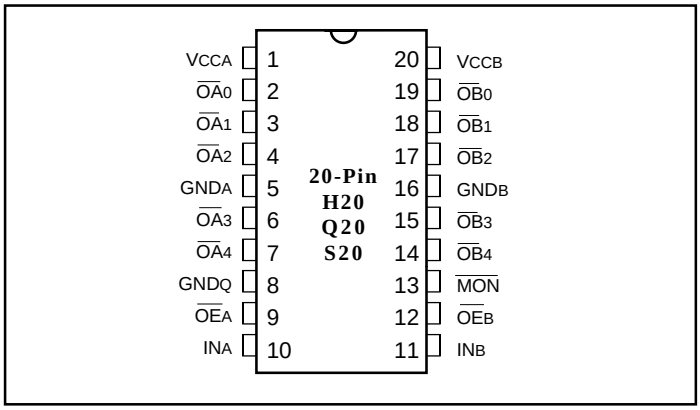


PI49FCT3806 Truth Table[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	$\overline{OA}_N$, $\overline{OB}_N$	$\overline{MON}$
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

Note:
1. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance

PI49FCT3806 Product Pin Configuration



Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[1]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Note:
1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & I/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Ambient Temperature = –40°C to +85°C, Vcc = 3.3V ±0.3V

DC Electrical Characteristics (Over the Operating Range)

Symbol	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
V_{OH}	Output HIGH voltage	V_{CC} = 1.5V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –0.1mA I_{OH} = –8mA	V_{CC}-0.2 2.4[3]	– 3.0	– –	V
V_{OL}	Output LOW voltage	V_{CC} = 1.5V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA I_{OL} = 16mA I_{OL} = 24mA	– – –	– 0.2 0.3	0.2 0.4 0.5	
V_{IH}	Input HIGH voltage	Guaranteed Logic HIGH level	Input Pins	2.0	–	5.5	
V_{IL}	Input LOW voltage	Guaranteed Logic LOW level	Input Pins	–0.5	–	0.8	
I_{IH}	Input HIGH current	V_{CC} = Max.	V_{IN} = V_{CC} (Input Pins)	–	–	1	µA
I_{IL}	Input LOW current	V_{CC} = Max.	V_{IN} = GND (Input & I/O Pins)	–	–	–1	
I_{OZH}	High impedance Output Current	V_{CC} = Max (3-State Output Pins)	V_{OUT} = V_{CC}	–	–	1	
I_{OZL}			V_{OUT} = GND	–	–	–1	
V_{IK}	Clamp diode voltage	V_{CC} = Min., I_{IN} = –18mA		–	–0.7	–1.2	V
I_{ODH}	Output HIGH current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		–35	–60	–110	mA
I_{ODL}	Output LOW current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		50	90	200	
I_{OS}	Short circuit current[5]	V_{CC} = Max., V_{OUT} = GND[5]		–60	–135	–240	
V_H	Input Hysteresis			–	150	–	mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. V_{OH} = V_{CC} – 0.6V at rated current.
4. This parameter is determined by device characterization but is not production tested.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}	—	3	30	µA
ΔI_{CC}	Supply Current per Inputs @ TTL HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	300	µA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE_A}$ or $\overline{OE_B}$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.08	0.16	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_O = 10 MHz 50% Duty Cycle $\overline{OE_A}$ or $\overline{OE_B}$ = GND Mon. Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.3	9.0[5]	mA
			V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	3.3	10.0[5]	
		V_{CC} = Max., Outputs Open f_O = 2.5 MHz 50% Duty Cycle $\overline{OE_A}$ or $\overline{OE_B}$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.8	6.0[5]	
			V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	1.8	7.0[5]	

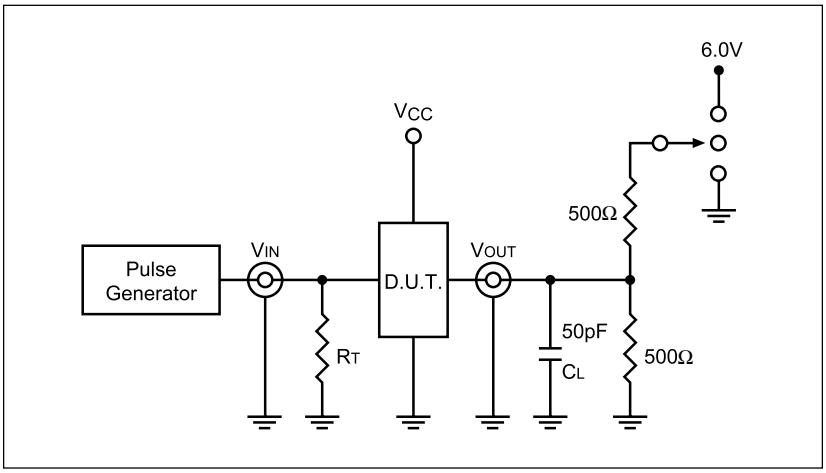
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (V_{IN} = V_{CC} – 0.6V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} – 0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Condition[1]	3805/3806		3805A/3806A		3805B/3806B		3805C/3806C		Units
			Com.		Com.		Com.		Com.		
			Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_N, IN_B to OB_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.8	1.5	5.0	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_A$ to OA_N, $\overline{OE}_B$ to OB_N		1.5	8.0	1.5	8.0	1.5	6.5	1.5	6.2	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_A$ to OA_N, $\overline{OE}_B$ to OB_N		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	
$t_{SK(o)}$[3]	Skew between two outputs of same package (Same transition)		—	0.7	—	0.7	—	0.5	—	0.5	
$t_{SK(p)}$[3]	Skew between opposite transition (t_{PHL}-t_{PLH}) of the same output		—	1.0	—	0.7	—	0.5	—	0.5	
$t_{SK(t)}$[3]	Skew between two outputs of different package at same temperature (Same transition)		—	1.5	—	1.2	—	1.0	—	0.8	

Note:
1. See test circuit and waveforms
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worst cast temperature (max. temp).

Tests Circuits for All Outputs[1], except for F_{IN} >100 MHz



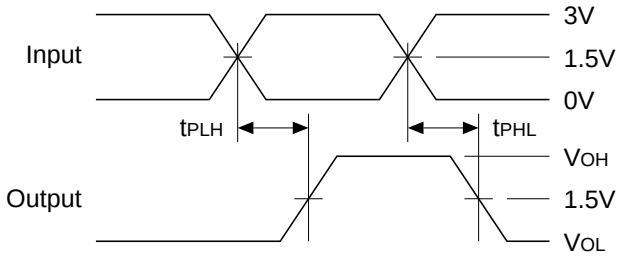
Switch Position

Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

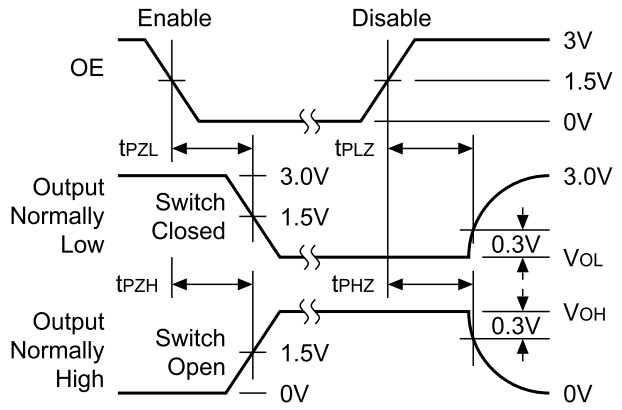
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SWITCHING WAVEFORMS

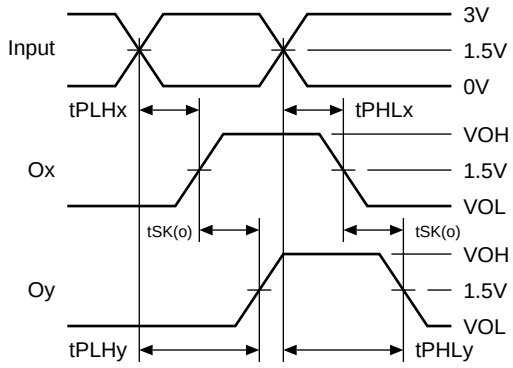
Propagation Delay



Enable and Disable Times

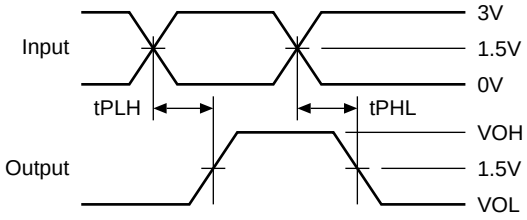


Output Skew – $t_{SK(o)}$



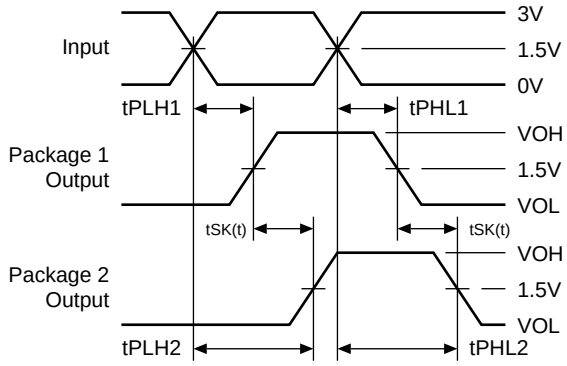
tSK(o) = | tPLHy – tPLHx | or | tPHLy – tPHLx |

Pulse Skew – $t_{SK(p)}$



tSK(p) = | tPHL – tPLH |

Package Skew – $t_{SK(t)}$

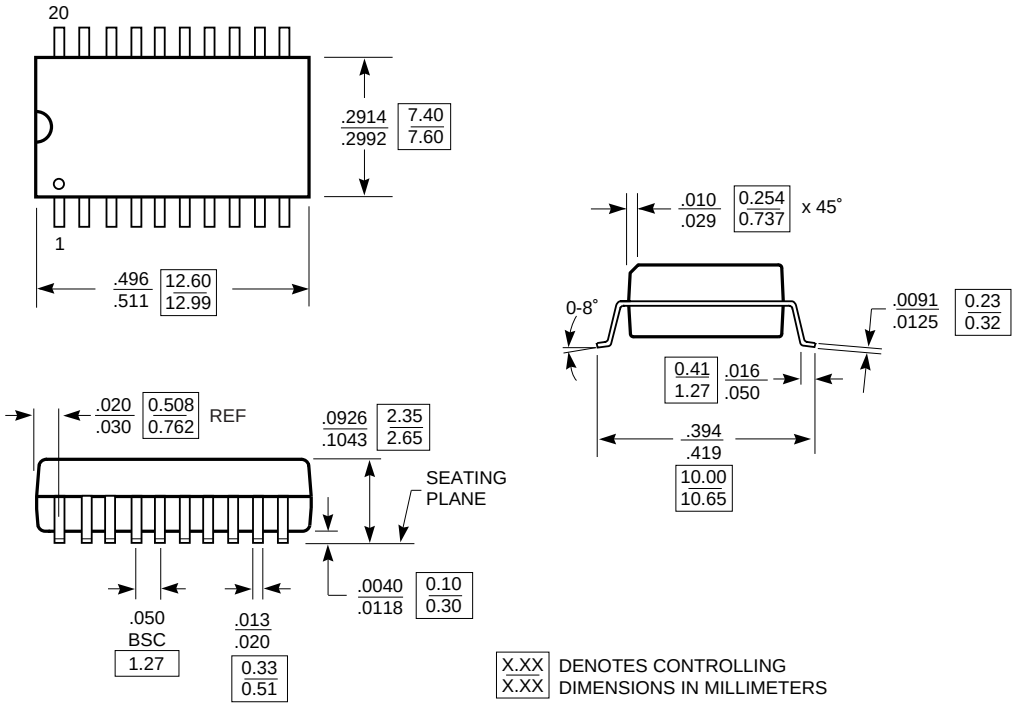


tSK(t) = | tPLH2 – tPLH1 | or | tPHL2 – tPHL1 |

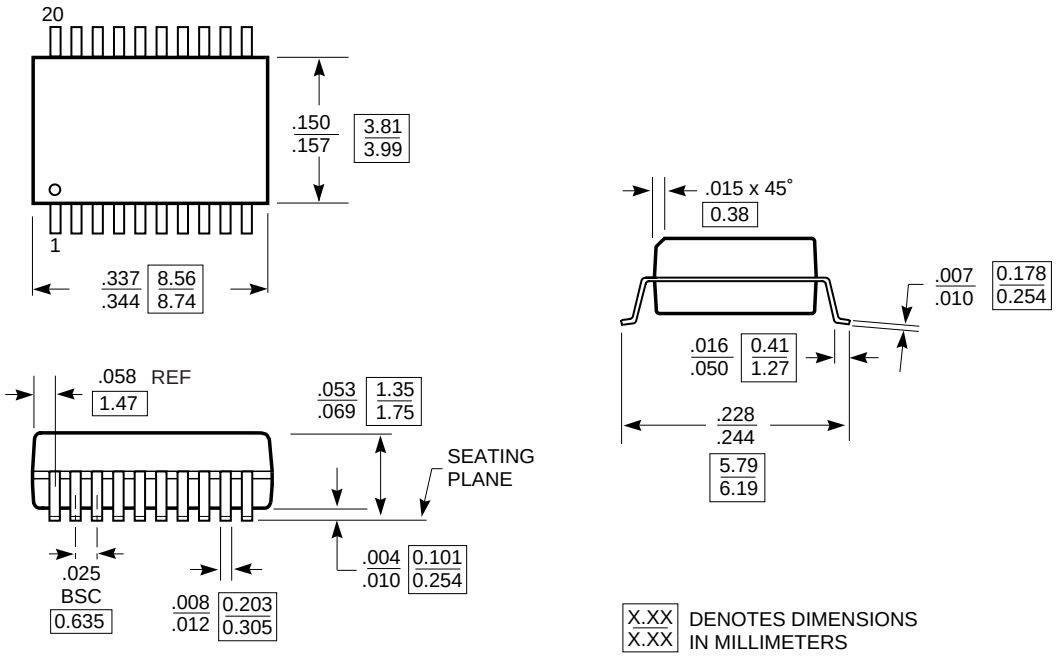
Ordering Information

Ordering Code	Package Type	Rating	Note
PI49FCT3805H PI49FCT3806H	20-pin 209 mil SSOP	Industrial	Refer to Switching Characteristic Table for Speed Grade Characteristics
PI49FCT3805Q PI49FCT3806Q	20-pin 150 mil QSOP		
PI49FCT3805S PI49FCT3806S	20-pin 300 mil SSIC		
PI49FCT3805AH PI49FCT3806AH	20-pin 209 mil SSOP		
PI49FCT3805AQ PI49FCT3806AQ	20-pin 150 mil QSOP		
PI49FCT3805AS PI49FCT3806AS	20-pin 300 mil SSIC		
PI49FCT3805BH PI49FCT3806BH	20-pin 209 mil SSOP		
PI49FCT3805BQ PI49FCT3806BQ	20-pin 150 mil QSOP		
PI49FCT3805BS PI49FCT3806BS	20-pin 300 mil SSIC		
PI49FCT3805CH PI49FCT3806CH	20-pin 209 mil SSOP		
PI49FCT3805CQ PI49FCT3806CQ	20-pin 150 mil QSOP		
PI49FCT3805CS PI49FCT3806CS	20-pin 300 mil SSIC		

20-Pin SOIC Package Drawing (S)



20-Pin QSOP Package Drawing (Q)



20-Pin SSOP Package Drawing (H)