

Digital transistors (built-in resistors)

DTD143EK / DTD143ES / DTD143EC

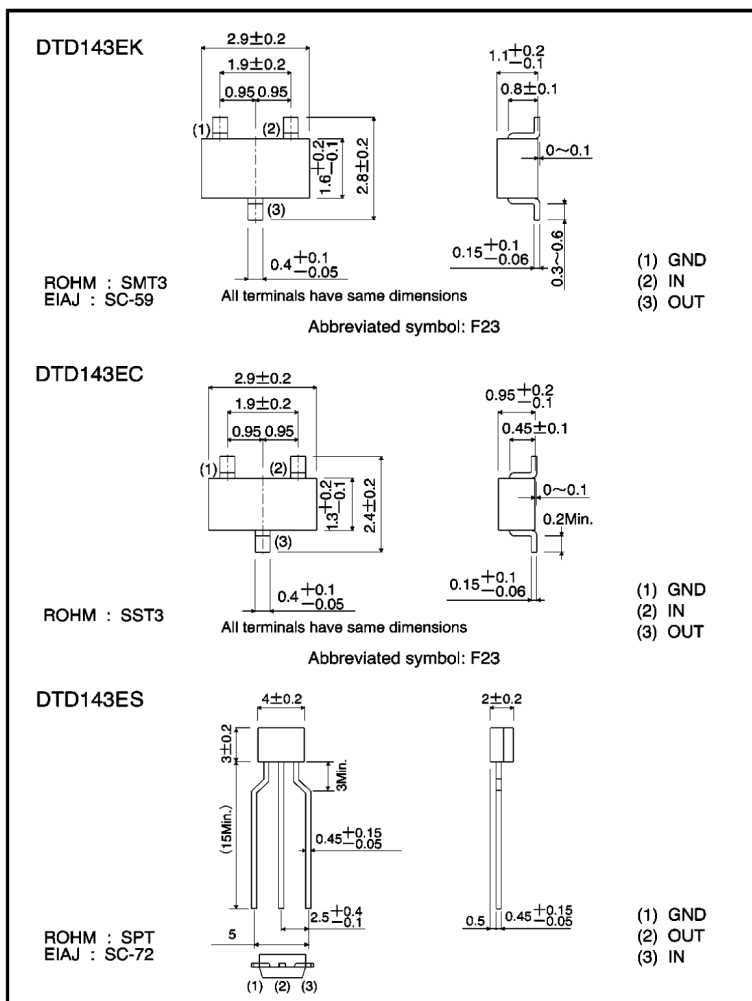
●Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.

●Structure

NPN digital transistor
(Built-in resistor type)

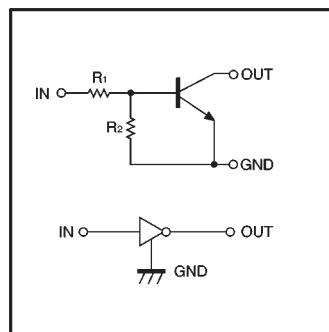
●External dimensions (Units: mm)



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits(DTD143E□)			Unit
		K	C	S	
Supply voltage	V _{CC}	50			V
Input voltage	V _{IN}	-10~+30			V
Output current	I _C	500			mA
Power dissipation	P _d	200	300		mW
Junction temperature	T _j	150			°C
Storage temperature	T _{stg}	-55~+150			°C

●Equivalent circuit



●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage	V _{I(off)}	—	—	0.5	V	V _{CC} =5V, I _O =100 μA
	V _{I(on)}	3	—	—		V _O =0.3V, I _O =20mA
Output voltage	V _{O(on)}	—	0.1	0.3	V	I _O /I _I =50mA/2.5mA
Input current	I _I	—	—	1.8	mA	V _I =5V
Output current	I _{O(off)}	—	—	0.5	μA	V _{CC} =50V, V _I =0V
DC current gain	G _I	47	—	—	—	V _O =5V, I _O =50mA
Input resistance	R _I	3.29	4.7	6.11	kΩ	—
Resistance ratio	R ₂ /R ₁	0.8	1	1.2	—	—
Transition frequency	f _T	—	200	—	MHz	V _{CE} =10V, I _E =-50mA, f=100MHz *

* Transition frequency of the device

●Packaging specifications

Part No.	Package	SMT3	SST3	SPT
	Packaging type	Taping	Taping	Taping
	Code	T146	T116	TP
	Basic ordering unit (pieces)	3000	3000	5000
DTD143EK		○	—	—
DTD143EC		—	—	○
DTD143ES		—	○	—

●Electrical characteristic curves

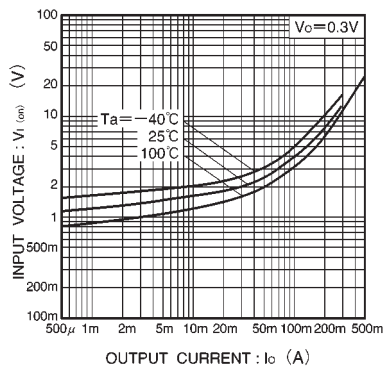


Fig.1 Input voltage vs. output current (ON characteristics)

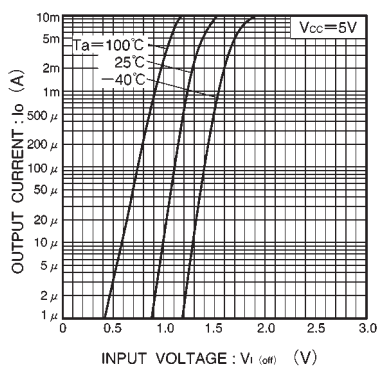


Fig.2 Output current vs. input voltage (OFF characteristics)

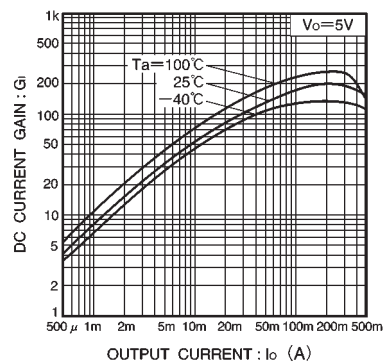


Fig.3 DC current gain vs. output current

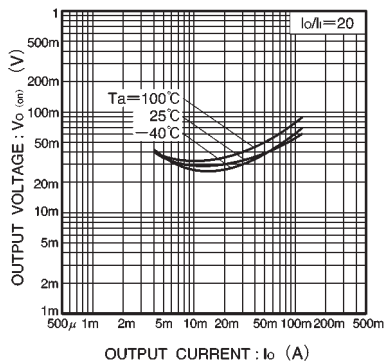


Fig.4 Output voltage vs. output current