KSZ9021RN

Gigabit Ethernet Transceiver with RGMII Support

KSZ9021RN-EVAL Board User's Guide

Revision 1.0 / November 2009

Micrel, Inc. ♦ 2180 Fortune Drive ♦ San Jose, CA 95131 ♦ U.S.A.
408-944-0800 (voice) ♦ 408-474-1000 (fax)
http://www.Micrel.com

Revision History

Revision	Date	Summary of Changes
1.0	11/17/09	Initial Release

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1.0 Introduction

The KSZ9021RN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9021RN reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9021RN can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9021RN provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000 Mbps speed.

The KSZ9021RN Socket Board (KSZ9021RN-EVAL) provides a comprehensive platform to evaluate the KSZ9021RN features. All KSZ9021RN configuration pins are accessible either by jumpers, test points or interface connectors.

2.0 Board Features

- Micrel KSZ9021RN 10Base-T/100Base-TX/1000Base-T Physical Layer Transceiver
- RJ-45 Jack for Ethernet cable interface
- Auto MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- RGMII Loopback for standalone evaluation
- LED Indicators for link status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins
- USB port for MDC/MDIO programming access to KSZ9021RN PHY registers

3.0 Evaluation Kit Contents

The KSZ9021RN Evaluation Kit includes the following hardware:

- KSZ9021RN-EVAL Board (a.k.a. KSZ9021RN Socket Board)
- 5V DC Adapter

And a design package with the following collaterals that can be downloaded from Micrel's website at http://www.micrel.com

- KSZ9021RN Socket Board Schematic (PDF and OrCAD DSN file)
- KSZ9021RN Socket Board Gerber Files (PDF version included)
- KSZ9021RN Socket Board BOM
- KSZ9021RN Socket Board User's Guide (this document)
- KSZ9021RN IBIS Model
- Micrel MDIO Configuration Software

The latest KSZ9021RN Data Sheet is also available from Micrel website.

4.0 Hardware Description

The KSZ9021RN-EVAL board provides a standalone evaluation platform for the KSZ9021RN Gigabit Ethernet Transceiver. Configuration of the KSZ9021RN is accomplished through on-board jumper selections and/or by PHY register access via the KSZ9021RN MDC/MDIO management pins via the USB port (CN1).

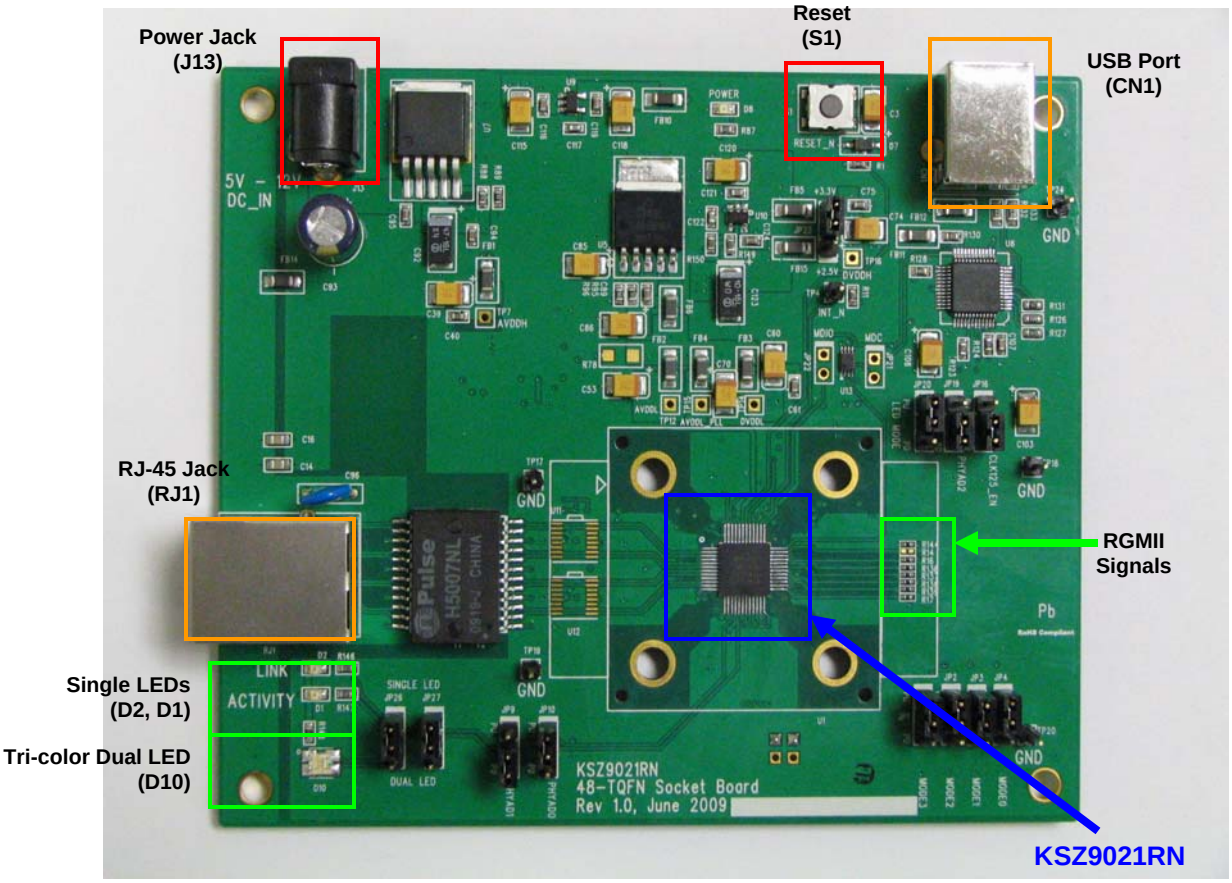


Figure 1. KSZ9021RN-EVAL Board

Features include a RJ-45 Jack for 10/100/1000 Ethernet speed cable connection, programmable LED indicators for reporting link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

On-board, RGMII receive output clock and signals are looped back to RGMII transmit input clock and signals to provide a standalone evaluation platform for the KSZ9021RN device. Optionally, the RGMII loop back path can be opened to allow the RGMII signals to be wired to a Gigabit MAC on another board.

The KSZ9021RN-EVAL board receives power from a DC power jack (J13). A 5V DC power adapter is provided with the board. Any DC power adapter in the range of 5V to 12V with a current rating of 2 Amp or better can also be used.

4.1 Jumper Setting & Definition

At power-up, the KSZ9021RN device is configured via strapping pins that are set by external pull-up and pull-down resistors. The KSZ9021RN-EVAL board provides jumpers for the KSZ9021RN device strap-in settings and for selective board options.

Jumpers allow for quick configuration and re-configuration. To override the current KSZ9021RN device and board settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S1) for the new setting(s) to take effect.

The KSZ9021RN-EVAL board jumper settings are defined in the table below.

Jumper	KSZ9021RN Pin Name	Setting	Function
KSZ9021RN Device Strapping Pins			
JP1	MODE3	Close pins (1, 2)	Set MODE3 = 1
		Close pins (2, 3)	Set MODE3 = 0
JP2	MODE2	Close pins (1, 2)	Set MODE2 = 1
		Close pins (2, 3)	Set MODE2 = 0
JP3	MODE1	Close pins (1, 2)	Set MODE1 = 1
		Close pins (2, 3)	Set MODE1 = 0
JP4	MODE0	Close pins (1, 2)	Set MODE0 = 1
		Close pins (2, 3)	Set MODE0 = 0
JP19	PHYAD2	Close pins (1, 2)	Set PHYAD2 = 1
		Close pins (2, 3)	Set PHYAD2 = 0
JP9	PHYAD1	Close pins (1, 2)	Set PHYAD1 = 1
		Close pins (2, 3)	Set PHYAD1 = 0
JP10	PHYAD0	Close pins (1, 2)	Set PHYAD0 = 1
		Close pins (2, 3)	Set PHYAD0 = 0
JP16	CLK125_EN	Close pins (1, 2)	Enable 125 MHz Clock Output
		Close pins (2, 3)	Disable 125 MHz Clock Output
JP20	LED_MODE	Close pins (1, 2)	Select Single LED Mode
		Close pins (2, 3)	Select Tri-color Dual LED Mode
KSZ9021RN-EVAL Board Settings			
JP26	LED2	Close pins (1, 2)	Use for Single LED Mode
		Close pins (2, 3)	Use for Tri-color Dual LED Mode
JP27	LED1	Close pins (1, 2)	Use for Single LED Mode
		Close pins (2, 3)	Use for Tri-color Dual LED Mode
JP23	DVDDH	Close pins (1, 2) [1]	Select 2.5V for KSZ902RN digital I/Os
		Close pins (2, 3)	Select 3.3V for KSZ9021RN digital I/Os
JP21 [2]	MDC	Close Jumper	Close MDC signal to USB Controller (U8)
		Open Jumper	Open MDC signal to USB Controller (U8)
JP22 [2]	MDIO	Close Jumper	Close MDIO signal to USB Controller (U8)
		Open Jumper	Open MDIO signal to USB Controller (U8)

Note: [1] If DVDDH is set to 2.5V, MDC/MDIO programming via USB Controller (U8) is disabled.

[2] JP21 and JP22 connect the MDC/MDIO signals to U8 when U13 is not populated.

Table 1. KSZ9021RN-EVAL Board – Jumper Definition

The following table lists the strapping pin definitions for the KSZ9021RN-EVAL board jumpers.

<table>
<tr><th>Jumper</th><th>Pin</th><th>Pin Name</th><th>Pin Function</th></tr>
<tr><td>JP1
JP2
JP3
JP4</td><td>27
28
31
32</td><td>MODE3
MODE2
MODE1
MODE0</td><td>The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows:

<table><tr><th>MODE[3:0]</th><th>Mode</th></tr><tr><td>0100</td><td>NAND Tree</td></tr><tr><td>0111</td><td>Chip Power Down</td></tr><tr><td>1100</td><td>RGMII – advertise 1000Base-T full-duplex only</td></tr><tr><td>1101</td><td>RGMII – advertise 1000Base-T full and half-duplex only</td></tr><tr><td>1110</td><td>RGMII – advertise all capabilities (10/100/1000 speed half/full duplex), except 1000Base-T half-duplex</td></tr><tr><td>1111</td><td>RGMII – advertise all capabilities (10/100/1000 speed half/full duplex)</td></tr></table>
All other MODE[3:0] settings not listed are reserved and are not used by the KSZ9021RN-EVAL.

MODE[3:0] = 1111 is the normal RGMII setting and is set as the default for the board.</td></tr>
<tr><td>JP19
JP9
JP10</td><td>35
15
17</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
PHY Address bits [4:3] are always set to ‘00’.

PHYAD[2:0] = 001 is set as the default for the board.</td></tr>
<tr><td>JP16</td><td>33</td><td>CLK125_EN</td><td>CLK125_EN is latched at power-up / reset and is defined as follows:
Pull-up (1) = Enable 125MHz Clock Output
Pull-down (0) = Disable 125MHz Clock Output
Pin 41 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.

CLK125_EN = 0 is set as the default for the board.</td></tr>
<tr><td>JP20</td><td>41</td><td>LED_MODE</td><td>LED_MODE is latched at power-up / reset and is defined as follows:
Pull-up (1) = Single LED Mode
Pull-down (0) = Tri-color Dual LED Mode

LED_MODE = 1 is set as the default for the board.</td></tr>
</table>

Table 2. Strapping Pin Definitions for KSZ9021RN-EVAL Board Jumpers

4.2 Test Point Definition

The KSZ9021RN-EVAL board has 17 usable test points, as defined in the following table.

Test Point	Definition
TP4	Interrupt Signal (KSZ9021RN pin 38) with 4.7K external pull-up
TP7	AVDDH voltage – KSZ9021RN power pins
TP12	AVDDL voltage – KSZ9021RN power pins
TP14	DVDDL – KSZ9021RN power pins
TP15	AVDDL_PLL – KSZ9021RN power pin
TP16	DVDDH – KSZ9021RN power pins
TP17	Signal Ground
TP18	Signal Ground
TP19	Signal Ground
TP20	Signal Ground
TP24	Signal Ground
TP33	Exposed ground connection to KSZ9021RN paddle ground (bottom of chip); Test point is located on solder side of PCB.
TP34	End point for board trace delay for RGMII RX_CLK output clock; Refer to KSZ9021RN Socket Board Schematic for more details.
TP35	1.8ns (10000 mils) board trace delay for RGMII RX_CLK output clock, starting from resistor R144; Refer to KSZ9021RN Socket Board Schematic for more details.
TP36-TP37	450ps (2500 mils) board trace delay for RGMII RX_CLK output clock; Refer to KSZ9021RN Socket Board Schematic for more details.

Table 3. KSZ9021RN-EVAL Board – Test Point Definition

4.3 RJ-45 Copper Interface

The RJ-45 copper interface (RJ1) connects to standard unshielded twisted pair (UTP) CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX/1000Base-T network devices.

The KSZ9021RN copper media interface can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

Auto MDI/MDI-X is supported for automatic detection and correction for straight and crossover cables when interfacing to link partners with fixed MDI or MDI-X setting.

4.4 LED Indicators

The KSZ9021RN device provides two programmable LED output pins, LED2 (pin 15) and LED1 (pin 17). On the KSZ9021RN-EVAL board, these two LED pins are connected to two sets of LEDs to support two LED configurations: Single LED mode and Tri-color Dual LED mode.

4.4.1 Single LED Mode

To enable Single LED mode,

- Close pins (1, 2) of jumpers JP26 and JP27 to select D2 and D1, respectively for the single LEDs.
- Close pins (1, 2) of jumper JP20 to set the LED_MODE strap-in for Single LED mode.
- Power-up the board.

After board power-up, the on-board D2 and D1 LEDs are defined as follows:

LED	LED Definition	Link / Activity
D2	OFF	Link off
	Green – ON	Link on (any speed)
D1	OFF	No Activity
	Green – Blinking	Activity (RX, TX)

Table 4: Single LED Mode – LED Definition

4.4.2 Tri-color Dual LED Mode

To enable Tri-color Dual LED mode,

- Close pins (2, 3) of jumpers JP26 and JP27 to select D10 for the tri-color dual LED.
- Close pins (2, 3) of jumper JP20 to set the LED_MODE strap-in for Tri-color Dual LED mode.
- Power-up the board.

After board power-up, the on-board D10 LED is defined as follows:

LED: D10	Link / Activity
OFF	Link off
Green – ON	1000Mbps Link / No Activity
Green – Blinking	1000Mbps Link / Activity (RX, TX)
Red – ON	100Mbps Link / No Activity
Red – Blinking	100Mbps Link / Activity (RX, TX)
Orange – ON	10Mbps Link / No Activity
Orange – Blinking	10Mbps Link / Activity (RX, TX)

Table 5: Tri-color Dual LED Mode – LED Definition

4.5 Reduced Gigabit Media Independent Interface (RGMII)

The KSZ9021RN-EVAL board provides open access to the KSZ9021RN device's RGMII signals, and enables the RGMII signals to be wired for the following two usages:

- RGMII Loop Back
- RGMII Connection to GMAC

4.5.1 RGMII Loop Back

The KSZ9021RN-EVAL board is shipped with the RGMII signals configured for RGMII Loop Back. Resistors [R144, R16, R136-R139] are populated to connect the RGMII output clock and signals to their respective RGMII input clock and signals, thru resistors [R145 (via TP35 to TP34), R17, R143, R142, R141, R140], respectively. Refer to KSZ9021RN Socket Board Schematic for details.

RGMII Loop Back enables the KSZ9021RN device to operate as a standalone evaluation platform without the need of an external GMAC. Ethernet traffic from the link partner (Spirent SmartBits 6000B in the following figure) are received by the KSZ9021RN device, looped back externally via RGMII pins, and transmitted back to the link partner.

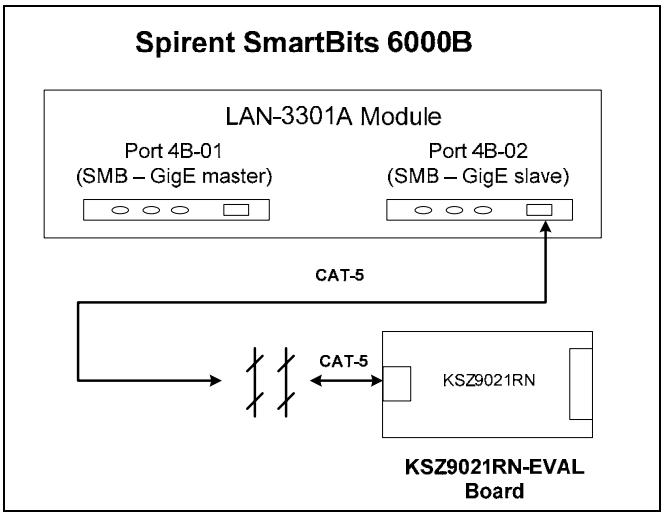


Figure 2. KSZ9021RN-EVAL Board – RGMII Loop Back

RGMII Loop Back is supported for 1000Base-T and 100Base-TX only. 10Base-T requires a MAC due to preamble consumption, and therefore is not supported.

4.5.2 RGMII Connection to GMAC

The KSZ9021RN-EVAL board exposes the RGMII signals at the following series termination (49.9 Ohm) / jumper (0 Ohm) resistor locations, as indicated in the following table.

Resistor (PCB location)	KSZ9021RN-EVAL Signal Name	RGMII Signal Name (per spec)
R144 left pad (PCB – top side)	RX_CLK	RXC
R16 left pad (PCB – top side)	RX_DV	RX_CTL
R136 left pad (PCB – top side)	RXD0	RXD0
R137 left pad (PCB – top side)	RXD1	RXD1
R138 left pad (PCB – top side)	RXD2	RXD2
R139 left pad (PCB – top side)	RXD3	RXD3
R145 top pad (PCB – bottom side)	GTX_CLK	TXC
R17 left pad (PCB – top side)	TX_EN	TX_CTL
R143 top pad (PCB – bottom side)	TXD0	TXD0
R142 top pad (PCB – bottom side)	TXD1	TXD1
R141 top pad (PCB – bottom side)	TXD2	TXD2
R140 top pad (PCB – bottom side)	TXD3	TXD3

Table 6. RGMII Signals access at series termination / jumper resistor locations

Resistors [R144, R16, R136-R139] for the RGMII output clock and signals and the corresponding resistors [R145 (via TP35 to TP34), R17, R143, R142, R141, R140] for the RGMII input clock and signals can be removed to open the RGMII Loop Back path and allow the RGMII signals (in the above table) to be wired to a GMAC on another board for evaluation and testing.

4.6 USB Port

The USB port (CN1) provides programming access to the KSZ9021RN device's PHY registers through its MDC/MDIO management pins.

See following software section for PHY register access.

5.0 MicrelMdioConfig Software – Installation

The Micrel MDIO Configuration Software (**MicrelMdioConfig**) runs on a PC with the Window XP Operating System. It communicates to the KSZ9021RN-EVAL board via USB to provide programming access to the KSZ9021RN device's PHY registers.

The Micrel software is provided in a Microsoft Windows Installer installation package file (*.msi file) with the following file name.

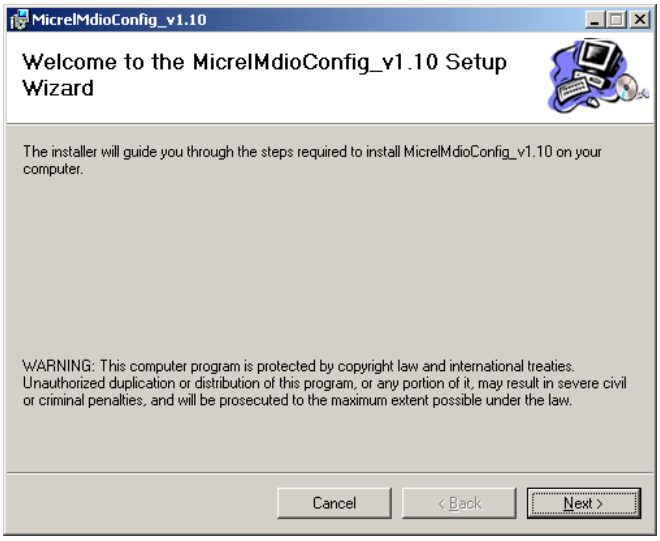
MicrelMdioConfig_verx.xx.msi // where x.xx is the release version number

5.1 MicrelMdioConfig Installation

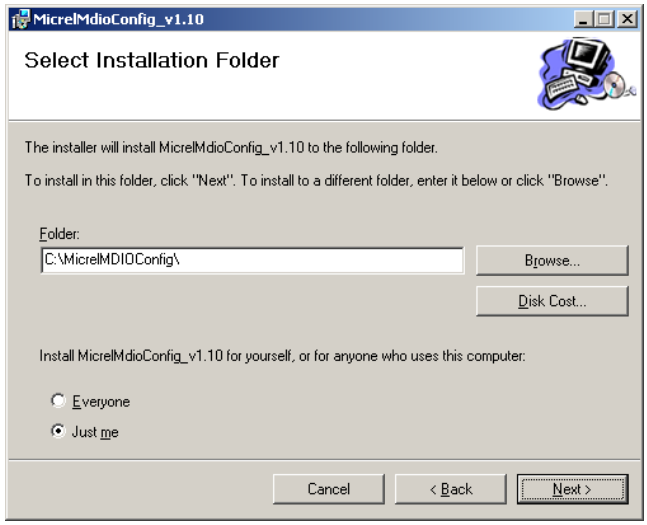
Before running the **MicrelMdioConfig** installation, make sure previously installed version of the **MicrelMdioConfig** software has been removed and the USB cable to the KSZ9021RN-EVAL board is unplugged.

To unpack the **MicrelMdioConfig_verx.xx.msi** file and start the installation, double click on the file name from Windows Explorer, and proceed with the following steps:

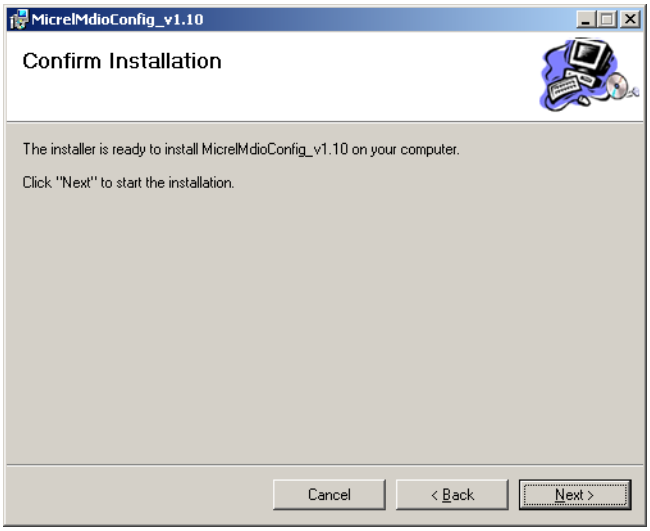
1. At the "**Welcome"** screen, press the **Next>** button.



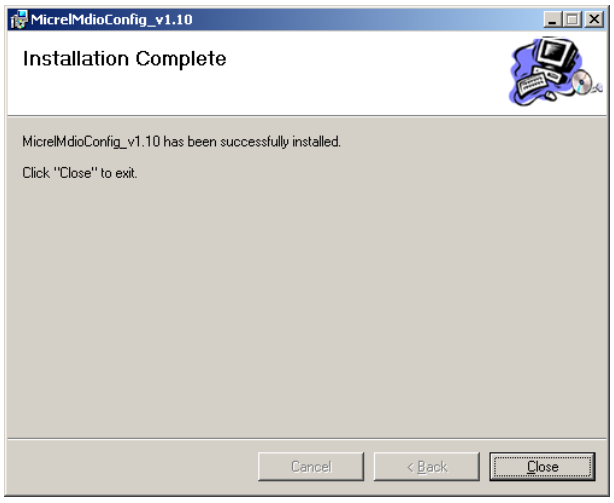
2. At the "**Select Installation Folder"** screen,
    a. Select the folder for the software installation (c:\MicrelMDIOConfig\ is the default installation folder).
    b. Press the **Next>** button.



3. At the "**Confirm Installation"** screen,
    a. Press the **Next>** button for the installation to proceed.
    b. Wait a few seconds for the installation to finish.



4. When the installation is finished, the "**Installation Complete"** screen is returned. Press the **Close>** button to exit.



After the **MicrelMdioConfig** software installation, an installation folder (c:\MicrelMDIOConfig\ is the default installation folder) is created containing the **MicrelMdioConfig** application programs and software drivers for the KSZ9021RN-EVAL board's USB port. Also, a shortcut is created on the Windows Desktop for the Windows GUI program, **MicrelMdioConfigWinApp.exe**.

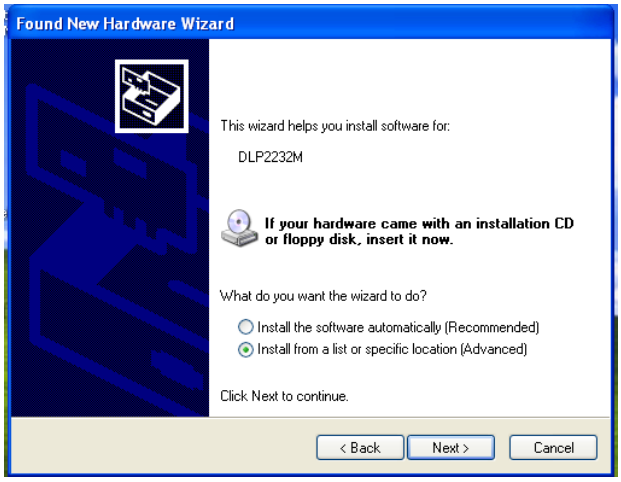
5.2 USB Driver Installation

Before installing the USB driver, complete the **MicrelMdioConfig** software installation in the previous section to extract the USB driver from the **MicrelMdioConfig_verx.xx.msi** installation file and have it copied to the created installation folder.

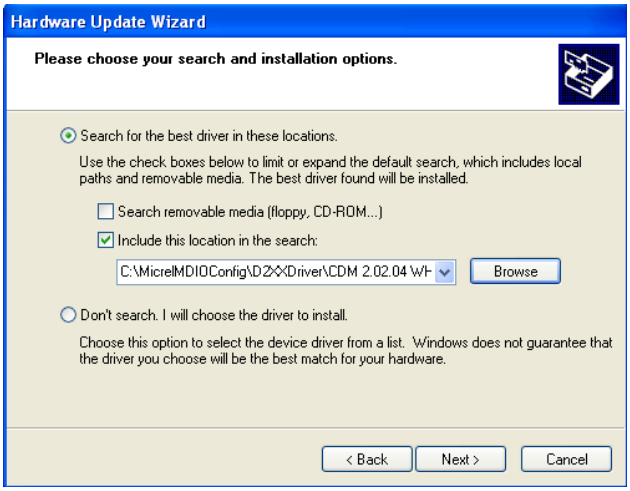
Power-up the KSZ9021RN-EVAL board and connect an USB cable from the board to the PC to initiate the USB driver installation, and proceed with the following steps:

1. Windows XP detects the KSZ9021RN-EVAL board's USB device. At the "**Welcome to the Found New Hardware Wizard"** screen,
    a. Select "**No, not this time".**
    b. Press the **Next>** button.

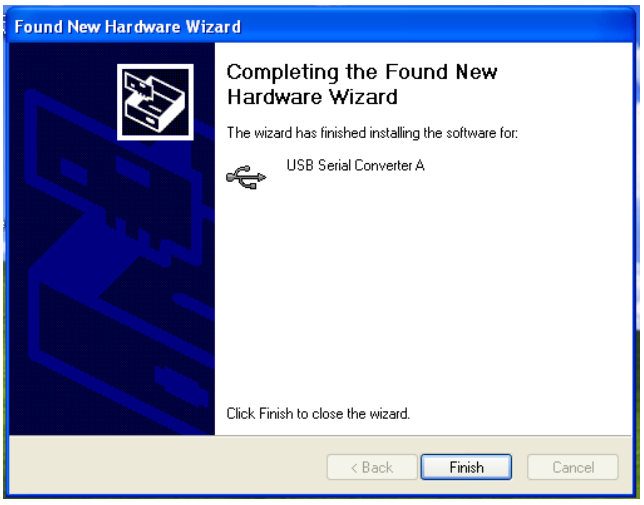
2. At the "**… install software for:"** screen,
    a. Select "**Install from a list or specific location (Advanced)".**
    b. Press the **Next>** button.



3. At the "**Please choose your search and installation options"** screen,
    a. Select **"Include this location in the search:"**
    b. Press the **Browse** button and navigate to and select the USB driver directory (**C:\MicrelMDIOConfig\D2XXDriver\CDM 2.02.04 WHQL Certified** is the USB driver directory for the default installation folder).
    c. Press the **Next>** button for the USB driver installation to proceed.
    d. Wait for the USB driver installation to finish.

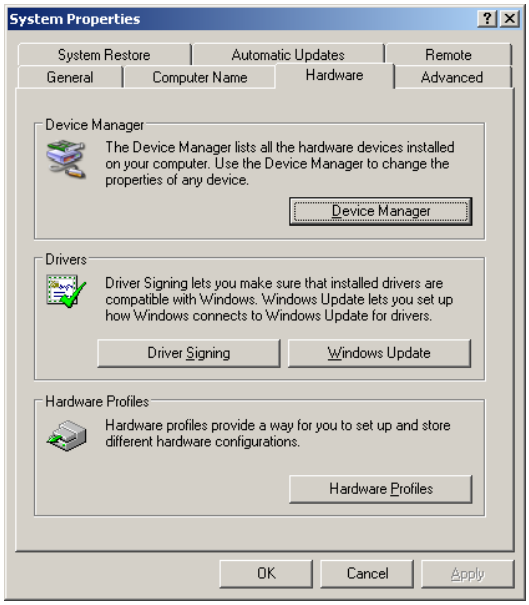


4. At the "**Completing the Found New Hardware Wizard"** screen, press the **Finish** button to close the wizard and exit.



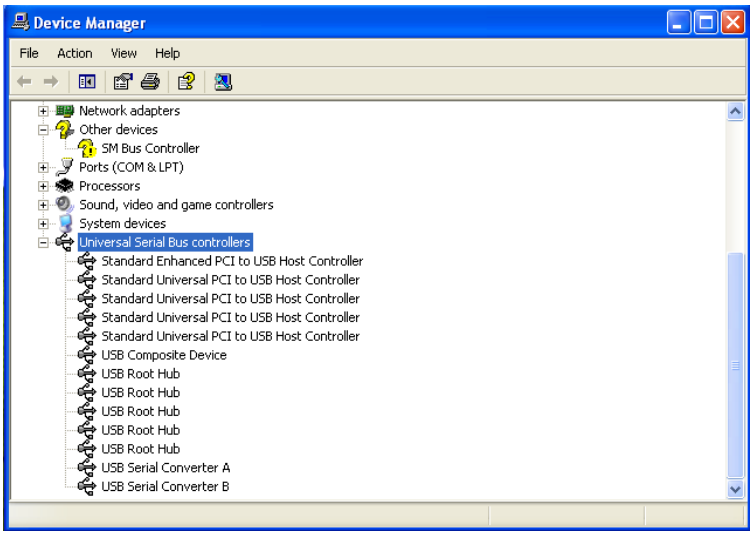
5. After the USB driver installation, verify the USB driver is installed.

   a. Go to the **Windows XP System Properties** box (select the System icon under Windows Start Menu -> Settings -> Control Panel).



b. Press the **Device Manager** button

c. Scroll down to the end of Universal Serial Bus controllers to verify "**USB Serial Converter A**" and "**USB Serial Converter B**" are installed.



6.0 MicrelMdioConfig Software – Application Programs

The **MicrelMdioConfig** application programs reside in the software installation folder created in the previous section (c:\MicrelMDIOConfig\ is the default installation folder). In the folder, there are two application programs that can be used to access the KSZ9021RN device's PHY registers:

- **MicrelMDIOConfigWinApp.exe** // Windows GUI program
- **mdioConfig.exe** // Windows Command Prompt program

Both programs can be opened concurrently. Use the Windows Task Bar to switch between the two programs.

6.1 Windows GUI program

The **MicrelMDIOConfigWinApp.exe** program is the Windows graphical user interface program.

6.1.1 Running the program

To launch the program, double click on either the **MicrelMDIOConfigWinApp.exe** file name from Windows Explorer or the Shortcut created for the program on the Windows Desktop, and proceed with the following steps:

1. At the configuration menu screen,

    a. Select "**KSZ9021 Gigabit Ethernet Transceiver"** for the device to configure.

    b. Set the "**Device Address**" to the KSZ9021RN-EVAL board's PHY address.

    c. Use the "**Pre-config file"** button to load PHY configuration script file (if any). More detail in following sub-section.

    d. Use the default DeviceID value or enter a new value (if the KSZ9021RN DeviceID in PHY registers 2 and 3 is different).

    e. Press the **Next>** button to continue.

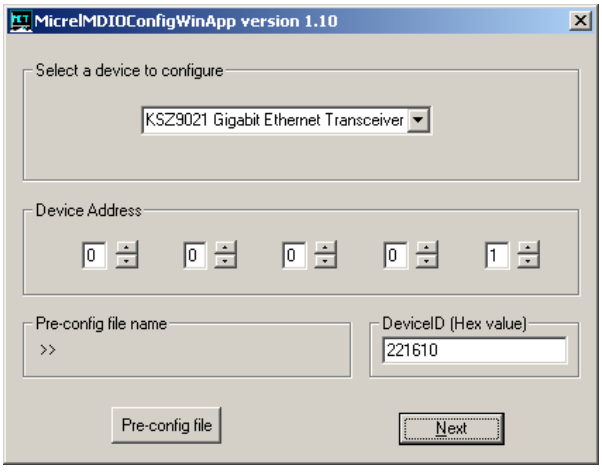


Figure 3. MicrelMDIOConfigWinApp Program – Configuration Menu Screen

2. At the program menu screen,

   a. Use the tabs across the top to select **Reg 0-3**, **Reg 4-7**, etc.

   b. To read the PHY registers,
      i. Press the **Read** button to refresh the register values in the program.

   c. To write to the PHY register(s),
      i. Use the register bit check box to set the bit(s) to "1" (checked) or "0" (unchecked).
      ii. Press the **Write** button.
      iii. Press the **OK** button to continue when the following "**Write Successful**" prompt is returned.

   d. Press the **Exit** button to close and exit the program.

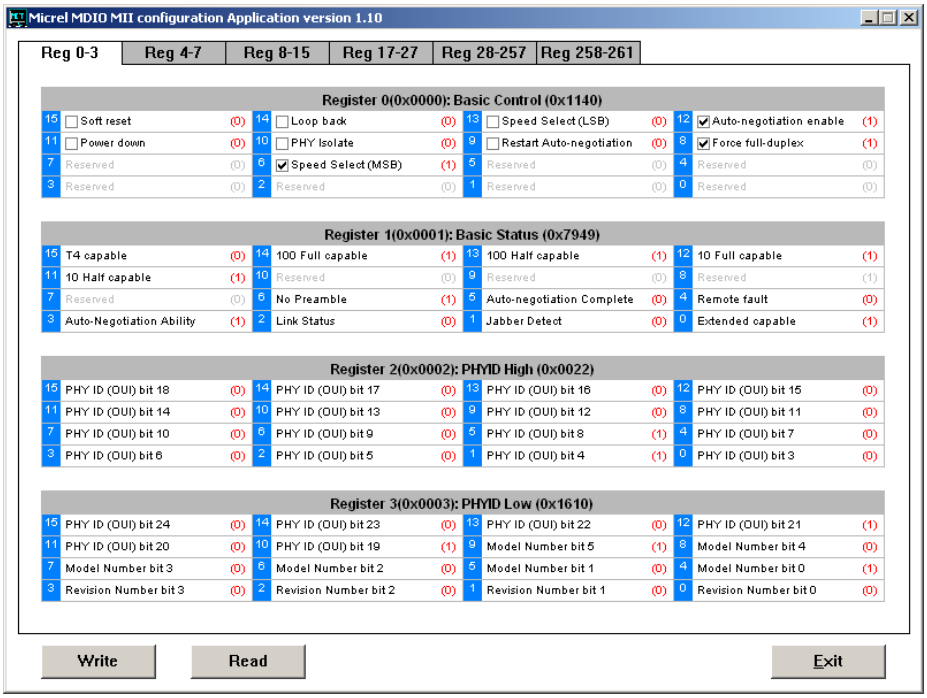


Figure 4. MicrelMDIOConfigWinApp Program – Program Menu Screen

6.1.2 Creating and Loading Script Files

The PHY configuration script file for the **MicrelMDIOConfigWinApp.exe** program is a text file with the *.mdo file name extension. A sample file, pre-config.mdo, is loaded in the program folder during the software installation. The sample file contains the following script:

```
#command syntax: [w|iw] [register address (hex)] [write value (hex)]
#w 0x0 0x1140
#iw 0x104 0xc0c0
#iw 0x105 0x7777
```

Where the parameters are defined as follows:

#	:	# symbol precedes line for comment or removal
w	:	Direct register write for KSZ9021RN's IEEE Defined and Vendor Specific Registers
iw	:	Indirect register write for KSZ9021RN's Extended Registers.\

The PHY configuration script file for the **MicrelMDIOConfigWinApp.exe** program is loaded at the configuration menu during program start-up. Use the "**Pre-config file"** button to load the *.mdo PHY configuration script file, as shown in the following figure.

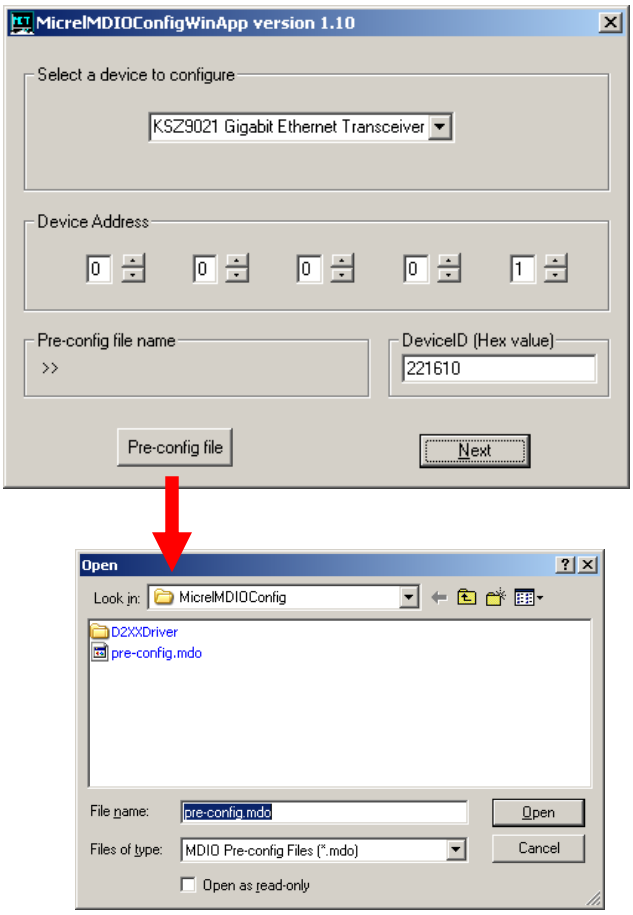


Figure 5. MicrelMDIOConfigWinApp Program – Pre-config Script File Loading

6.2 Windows Command Prompt – Command Line program

The **mdioConfig.exe** program is the command line interface program.

6.2.1 Running the program

The **mdioConfig.exe** program resides in the software installation folder created during the software installation (c:\MicrelMDIOConfig\ is the default installation folder). The program reads in the PHY address from the **deviceinfo.txt** file every time it is executed.

The **deviceinfo.txt** file is loaded in the program folder during the software installation, and has the PHY address set to "1", as the default. If the KSZ9021RN-EVAL board is set to a different PHY address, modify the hex PHY address value accordingly for the following line in the **deviceinfo.txt** file.

address=0x0001

The **mdioConfig.exe** program is executed from a Windows Command Prompt. Open a Windows Command Prompt (select the Command Prompt under Windows Start Menu -> Programs -> Accessories) and navigate to the **mdioConfig.exe** program directory (c:\MicrelMDIOConfig\ is the program directory for the default installation folder), as shown in the following figure.

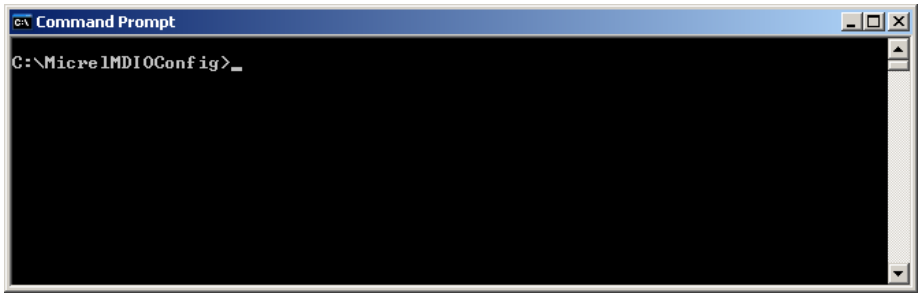


Figure 6. mdioConfig Program – Windows Command Prompt

The **mdioConfig.exe** program is started by typing the **mdioConfig.exe** program name at the Windows Command Prompt and pressing the **ENTER** key. Next, the program displays instruction for direct register read/write, indirect register read/write and to exit the program. Follow the instruction, as shown in the following figure, for the desired action.

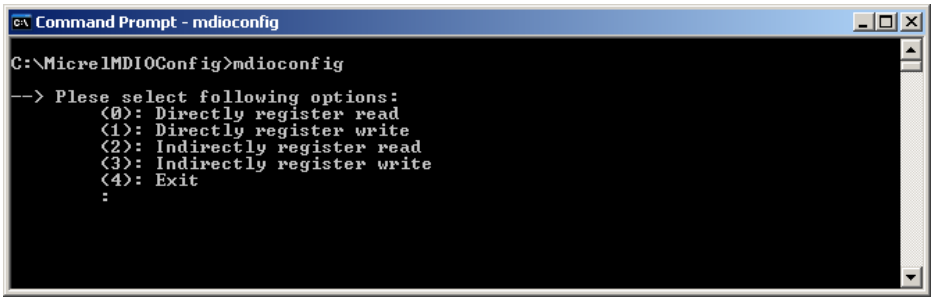


Figure 7. mdioConfig Program – in operation

6.2.2 Creating and Loading Script Files

The **mdioConfig.exe** program can execute with all parameters placed in a single command line, as shown in the following examples:

Direct Register Read

mdioconfig r [register address (hex)]
mdioconfig r 0x0000

Direct Register Write

mdioconfig w [register address (hex)] [write value (hex)]
mdioconfig w 0x0000 0x1940

Indirect Register Read

mdioconfig ir [register address (hex)]
mdioconfig ir 0x0101

Indirect Register Write

mdioconfig iw [register address (hex)] [write value (hex)]
mdioconfig iw 0x0102 0x0011

Where the parameters are defined as follows:

r	: Direct register read for KSZ9021RN's IEEE Defined and Vendor Specific Registers
w	: Direct register write for KSZ9021RN's IEEE Defined and Vendor Specific Registers
ir	: Indirect register read for KSZ9021RN's Extended Registers
iw	: Indirect register write for KSZ9021RN's Extended Registers

A group of single command lines can be put in a batch file (*.bat) to produce a PHY configuration script file. The following Windows Command Prompt capture shows the four examples above run in a script file, "example.bat."

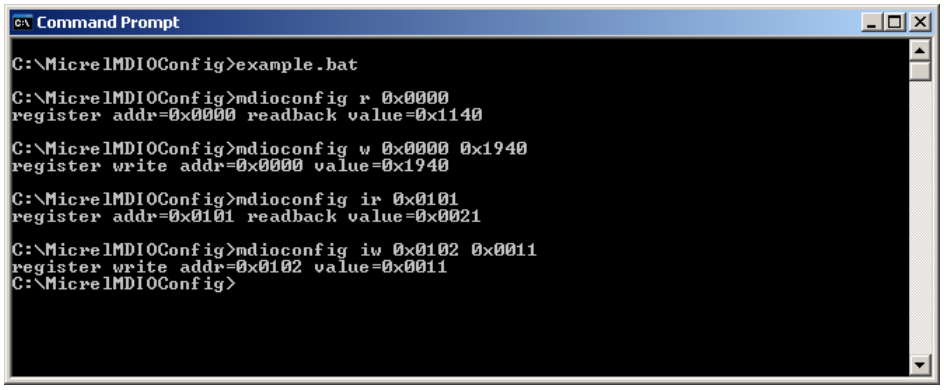


Figure 8. mdioConfig Program – script file "example.bat" run

When the single command line is executed, each direct/indirect register read back is dumped and appended to a log file, "mdiolog.txt."