

M16C/30P Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0088-0080

Rev.0.80

Mar 18, 2005

1. Overview

The M16C/30P Group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP.

These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, TV, home appliance, office/communications/portable/industrial equipment, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 lists Performance Outline of M16C/30P Group.

Table 1.1 Performance Outline of M16C/30P Group

Item		Performance
CPU	Number of Basic Instructions	91 instructions
	Minimum Instruction Execution Time	62.5ns(f(XIN)=16MHz, VCC1=VCC2=4.2 to 5.5V, no wait) 100ns(f(XIN)=10MHz, VCC1=VCC2=2.7 to 5.5V, no wait)
	Operation Mode	Single-chip
	Memory Space	1 Mbyte
	Memory Capacity	See Table 1.2 Product List
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin
	Multifunction Timer	Timer A : 16 bits x 3 channels, Timer B : 16 bits x 3 channels
	Serial Interface	3 channels Clock synchronous, UART, I ² C bus ⁽¹⁾ 1 channels IEBus ⁽²⁾
	A/D Converter	10-bit A/D converter: 1 circuit, 18 channels
	DMAC	2 channels
	CRC Calculation Circuit	CCITT-CRC
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	Internal: 20 sources, External: 7 sources, Software: 4 sources, Priority level: 7 levels
	Clock Generating Circuit	2 circuits Main clock generation circuit (*), Subclock generation circuit (*), (*)Equipped with a built-in feedback resistor.
Electric Characteristics	Supply Voltage	VCC1=VCC2=3.0 to 5.5 V (f(XIN)=16MHz) VCC1=VCC2=2.7 to 5.5 V (f(XIN)=10MHz, no wait)
	Power Consumption	10 mA (VCC1=VCC2=5V, f(XIN)=16MHz) 8 mA (VCC1=VCC2=3V, f(XIN)=10MHz) 1.8 μ A (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7 μ A(VCC1=VCC2=3V, stop mode)
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C
Package		100-pin plastic mold QFP, LQFP

NOTES:

1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. Use the M16C/30P on VCC1 = VCC2.

1.3 Block Diagram

Figure 1.1 is a M16C/30P Group Block Diagram.

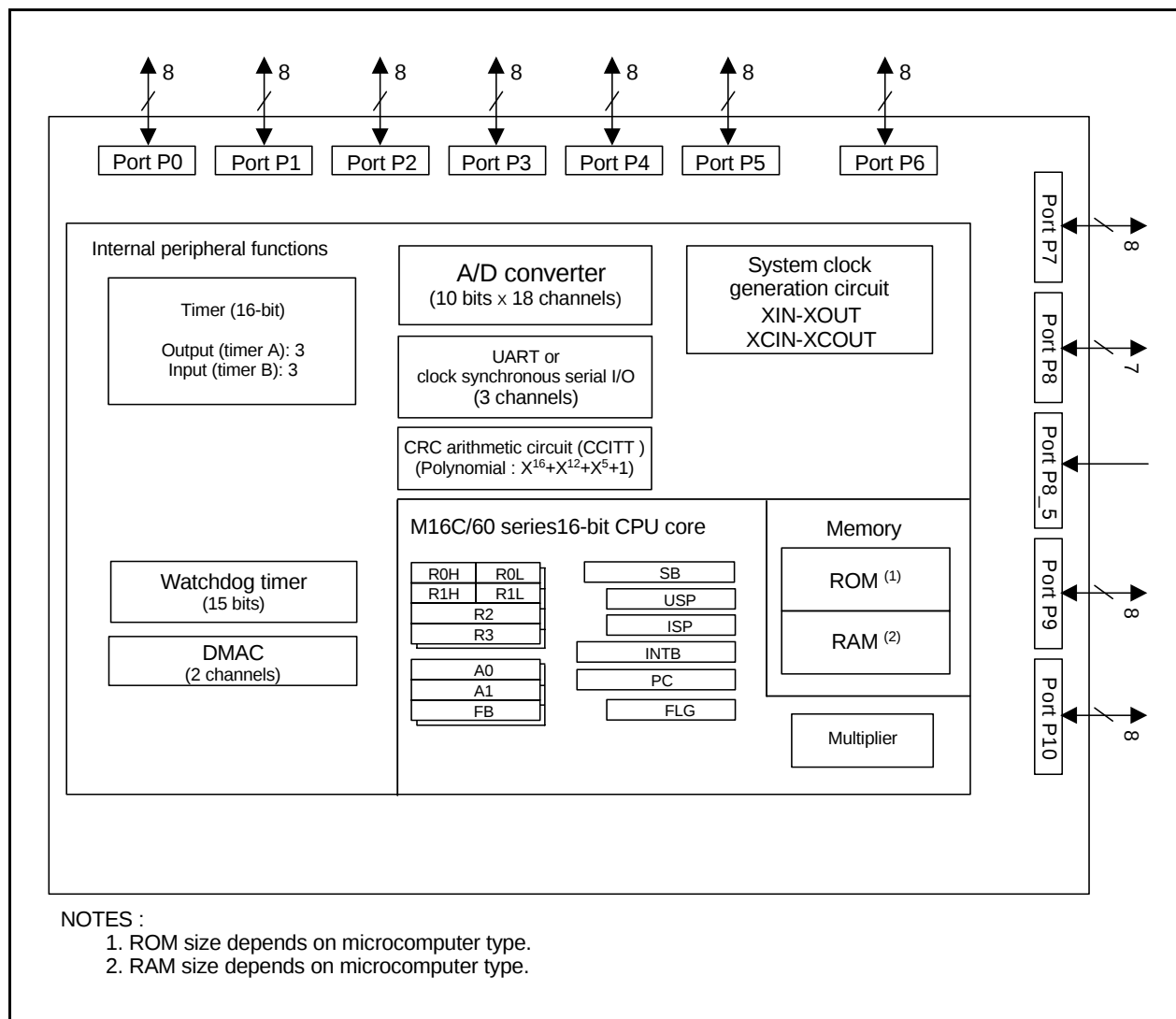


Figure 1.1 M16C/30P Group Block Diagram

1.4 Product List

Table 1.2 lists the M16C/30P group products and Figure 1.2 shows the Type No., Memory Size, and Package.

Table 1.2 Product List

As of Mar 2005

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
M30302MAP-XXXXFP (D)	96 Kbytes	5 Kbytes	100P6S-A	MASK ROM version
M30302MAP-XXXXGP (D)			100P6Q-A	
M30302MCP-XXXXFP (D)	128 Kbytes		100P6S-A	
M30302MCP-XXXXGP (D)			100P6Q-A	
M30302MEP-XXXXFP (D)	192 Kbytes	6 Kbytes	100P6S-A	
M30302MEP-XXXXGP (D)			100P6Q-A	

(D): Under development

(P): Under planning

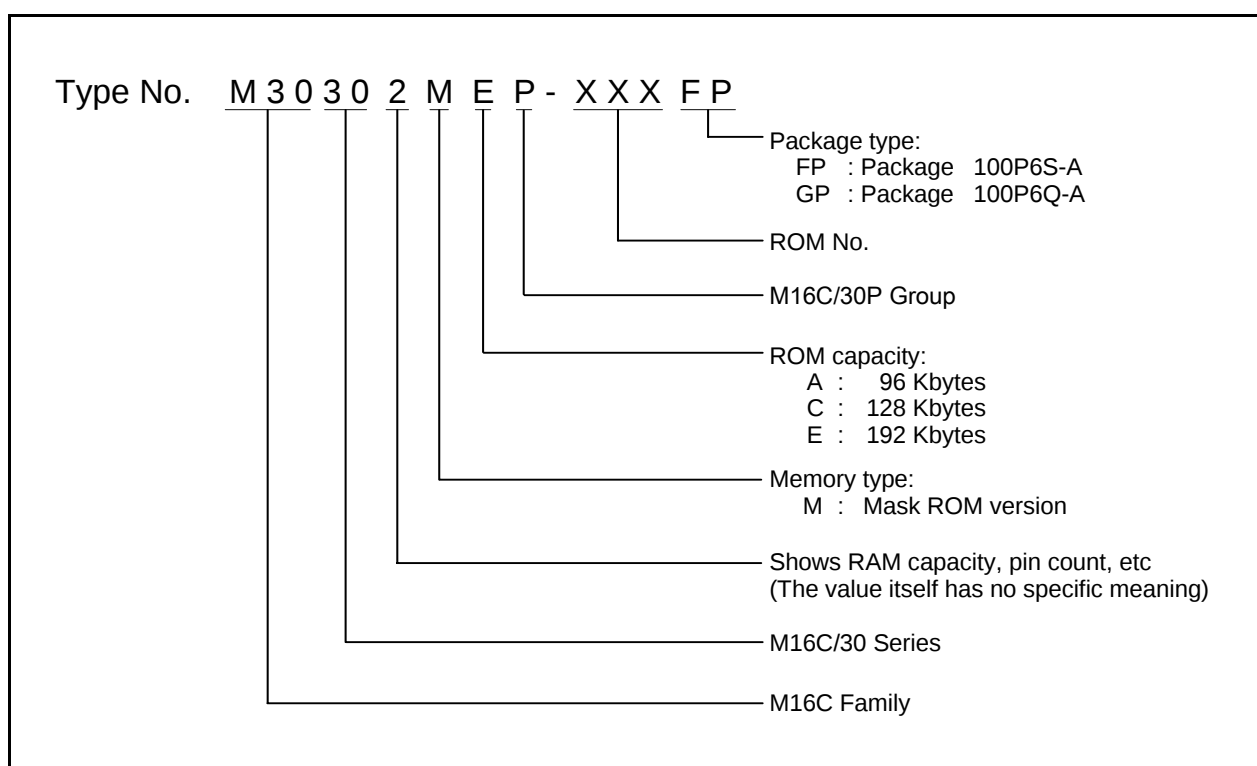


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figures 1.3 to 1.4 show the pin configurations (top view).

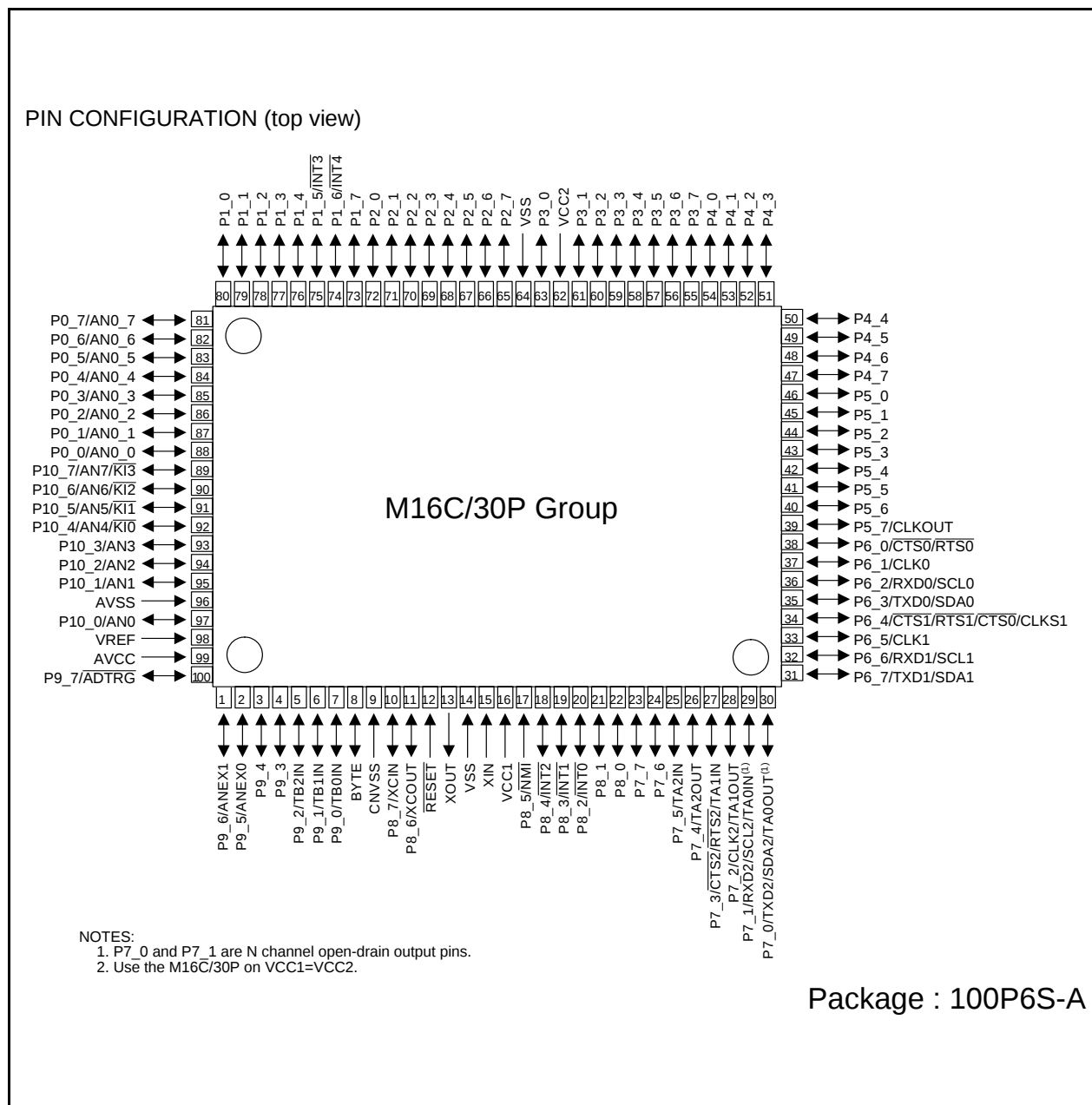


Figure 1.3 Pin Configuration (Top View)

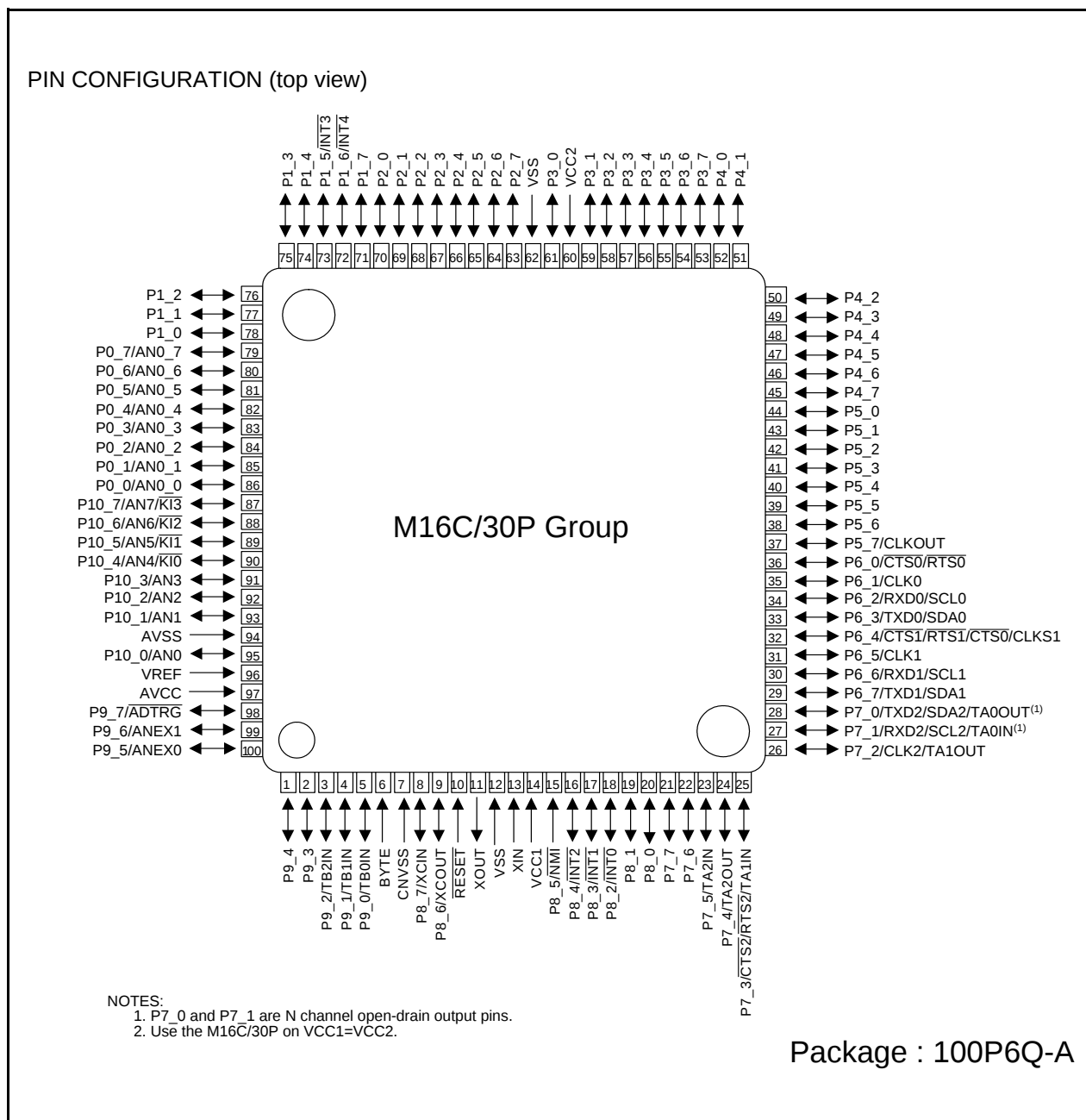


Figure 1.4 Pin Configuration (Top View)

1.6 Pin Description

Table 1.3 Pin Description (1)

Signal Name	Pin Name	I/O Type	Description
Power supply input	VCC1, VCC2 VSS	I	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the Vss pin. The VCC apply condition is that VCC1 = VCC2.
Analog power supply input	AVCC AVSS	I	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS	I	Connect this pin to VSS.
External data bus width select input	BYTE	I	
Main clock input	XIN	I	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt.
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt.
Timer A	TA0OUT to TA2OUT	I/O	These are timer A0 to timer A2 I/O pins. (except the output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA2IN	I	These are timer A0 to timer A2 input pins.
Timer B	TB0IN to TB2IN	I	These are timer B0 to timer B2 input pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	These are send control input pins.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	These are receive control output pins.
	CLK0 to CLK2	I/O	These are transfer clock I/O pins.
	RXD0 to RXD2	I	These are serial data input pins.
	TXD0 to TXD2	O	These are serial data output pins. (except TXD2 for the N-channel open drain output.)
	CLKS1	O	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	These are serial data I/O pins. (except SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	These are transfer clock I/O pins. (except SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

Table 1.4 Pin Description (2)

Signal Name	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Applies the reference voltage for the A/D converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7	I	Analog input pins for the A/D converter.
	ADTRG	I	This is an A/D trigger input pin.
	ANEX0	I/O	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	This is the extended analog input pin for the A/D converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. (except P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7	I/O	I/O ports having equivalent functions to P0.
Input port	P8_5	I	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

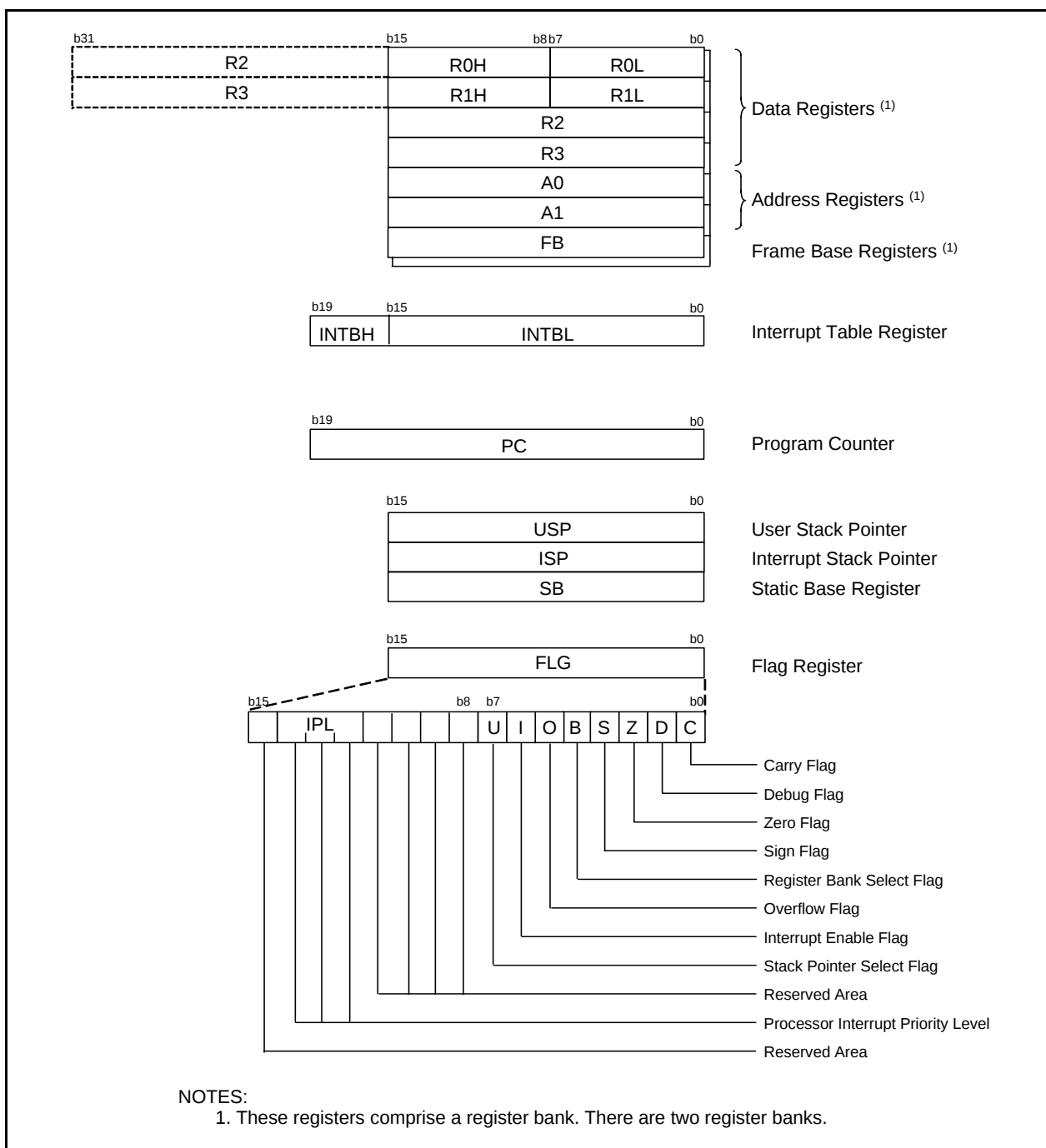


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a Memory Map of the M16C/30P group. The address space extends the 1M bytes from address 00000h to FFFFFh.

The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.

The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 10-Kbyte internal RAM is allocated to the addresses from 00400h to 02BFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.

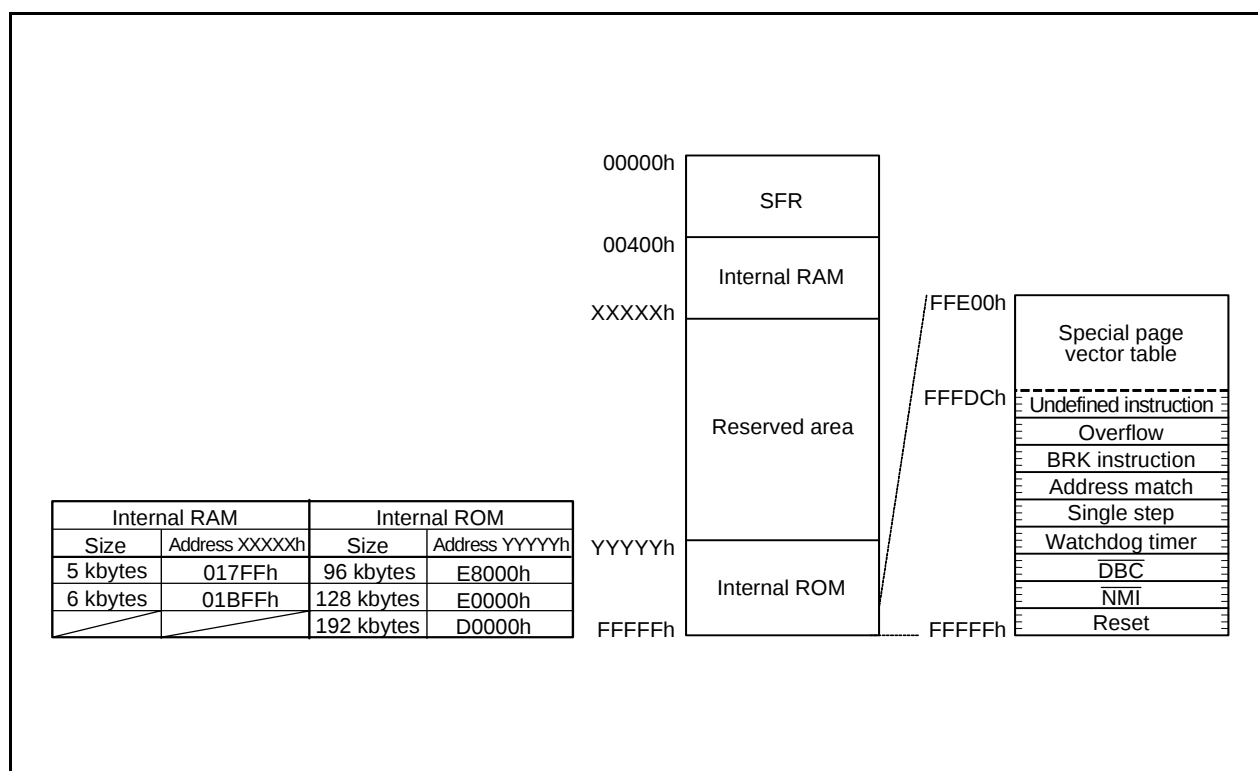


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.5 list the SFR information.

Table 4.1 SFR Information(1) ⁽¹⁾

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 ⁽²⁾	PM0	00h
0005h	Processor Mode Register 1	PM1	00XXX0XXb
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh			
000Ch			
000Dh			
000Eh	Watchdog Timer Start Register	WDTs	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch			
001Dh			
001Eh			
001Fh			
0020h	DMA0 Source Pointer	SAR0	XXh
0021h			XXh
0022h			XXh
0023h			
0024h	DMA0 Destination Pointer	DAR0	XXh
0025h			XXh
0026h			XXh
0027h			
0028h	DMA0 Transfer Counter	TCR0	XXh
0029h			XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h	DMA1 Source Pointer	SAR1	XXh
0031h			XXh
0032h			XXh
0033h			
0034h	DMA1 Destination Pointer	DAR1	XXh
0035h			XXh
0036h			XXh
0037h			
0038h	DMA1 Transfer Counter	TCR1	XXh
0039h			XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset.

X : Nothing is mapped to this bit

Table 4.2 SFR Information(2) ⁽¹⁾

Address	Register	Symbol	After Reset
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
0045h			
0046h	UART1 BUS Collision Detection Interrupt Control Register	U1BCNIC	XXXXX000b
0047h	UART0 BUS Collision Detection Interrupt Control Register	U0BCNIC	XXXXX000b
0048h			
0049h	INT4 Interrupt Control Register	INT4IC	XX00X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXXX000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXXX000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXXX000b
0058h			
0059h			
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXXX000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXXX000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00X000b
0060h to 024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral Clock Select Register	PCLKR	00000011b
025Fh			
0260h to 0335h			
0336h			
0337h			
0338h			
0339h			
033Ah			
033Bh			
033Ch			
033Dh			
033Eh			
033Fh			

NOTES:

- The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.3 SFR Information(3) ⁽¹⁾

Address	Register	Symbol	After Reset
0340h			
0341h			
0342h			
0343h			
0344h			
0345h			
0346h			
0347h			
0348h			
0349h			
034Ah			
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h			
0361h			
0362h			
0363h			
0364h			
0365h			
0366h			
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:

- The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.4 SFR Information(4) (1)

Address	Register	Symbol	After Reset
0380h	Count Start Flag	TABSR	000XX000b
0381h	Clock Prescaler Reset Flag	CPSRF	0XXXXXXXb
0382h	One-Shot Start Flag	ONSF	00XXX000b
0383h	Trigger Select Register	TRGSR	XXXX0000b
0384h	Up-Down Flag	UDF	XX0XX000b (2)
0385h			
0386h	Timer A0 Register	TA0	XXh
0387h			XXh
0388h	Timer A1 Register	TA1	XXh
0389h			XXh
038Ah	Timer A2 Register	TA2	XXh
038Bh			XXh
038Ch			
038Dh			
038Eh			
038Fh			
0390h	Timer B0 Register	TB0	XXh
0391h			XXh
0392h	Timer B1 Register	TB1	XXh
0393h			XXh
0394h	Timer B2 Register	TB2	XXh
0395h			XXh
0396h	Timer A0 Mode Register	TA0MR	00h
0397h	Timer A1 Mode Register	TA1MR	00h
0398h	Timer A2 Mode Register	TA2MR	00h
0399h			
039Ah			
039Bh	Timer B0 Mode Register	TB0MR	00XX0000b
039Ch	Timer B1 Mode Register	TB1MR	00XX0000b
039Dh	Timer B2 Mode Register	TB2MR	00XX0000b
039Eh			
039Fh			
03A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
03A1h	UART0 Bit Rate Generator	U0BRG	XXh
03A2h	UART0 Transmit Buffer Register	U0TB	XXh
03A3h			XXh
03A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
03A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
03A6h	UART0 Receive Buffer Register	U0RB	XXh
03A7h			XXh
03A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
03A9h	UART1 Bit Rate Generator	U1BRG	XXh
03AAh	UART1 Transmit Buffer Register	U1TB	XXh
03ABh			XXh
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
03ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
03AEh	UART1 Receive Buffer Register	U1RB	XXh
03AFh			XXh
03B0h	UART Transmit/Receive Control Register 2	UCON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 Request Factor Select Register	DM0SL	00h
03B9h			
03BAh	DMA1 Request Factor Select Register	DM1SL	00h
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is "0" by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

Table 4.5 SFR Information(5) (1)

Address	Register	Symbol	After Reset
03C0h	A/D Register 0	AD0	XXh
03C1h			XXh
03C2h	A/D Register 1	AD1	XXh
03C3h			XXh
03C4h	A/D Register 2	AD2	XXh
03C5h			XXh
03C6h	A/D Register 3	AD3	XXh
03C7h			XXh
03C8h	A/D Register 4	AD4	XXh
03C9h			XXh
03CAh	A/D Register 5	AD5	XXh
03CBh			XXh
03CCh	A/D Register 6	AD6	XXh
03CDh			XXh
03CEh	A/D Register 7	AD7	XXh
03CFh			XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	XXX000X0b
03D5h			
03D6h	A/D Control Register 0	ADCON0	000X0XXXb
03D7h	A/D Control Register 1	ADCON1	00000XXXb
03D8h			
03D9h			
03DAh			
03DBh			
03DCh			
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	00h
03FEh	Pull-Up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC}	Supply Voltage(V _{CC1} =V _{CC2})		V _{CC1} =V _{CC2} =AV _{CC}	−0.3 to 6.5	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	−0.3 to 6.5	V
V _i	Input Voltage	RESET, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, VREF, XIN		−0.3 to V _{CC} +0.3	V
		P7_0, P7_1		−0.3 to 6.5	V
V _o	Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XOUT		−0.3 to V _{CC} +0.3	V
		P7_0, P7_1		−0.3 to 6.5	V
P _d	Power Dissipation		−40°C<T _{opr} ≤85°C	300	mW
T _{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		−20 to 85 / −40 to 85	°C
T _{stg}	Storage Temperature			−65 to 150	°C

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply Voltage (V _{CC1} =V _{CC2})		2.7	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	HIGH Input Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	0.8V _{CC}		V _{CC}	V
		P7_0, P7_1	0.8V _{CC}		6.5	V
V _{IL}	LOW Input Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	0		0.2V _{CC}	V
I _{OH(peak)}	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-10.0	mA
I _{OH(avg)}	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-5.0	mA
I _{OL(peak)}	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
I _{OL(avg)}	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA
f(XIN)	Main Clock Input Oscillation Frequency (4)	V _{CC} =4.2V to 5.5V	0		16	MHz
		V _{CC} =2.7V to 4.2V	0		4×V _{CC} -0.8	MHz
f(XCIN)	Sub-Clock Oscillation Frequency			32.768	50	kHz
f(BCLK)	CPU Operation Clock		0		16	MHz

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = -20 to 85°C / -40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9 and P10 must be 80mA max. The total I_{OL(peak)} for ports P3, P4, P5, P6, P7 and P8_0 to P8_4 must be 80mA max. The total I_{OH(peak)} for ports P0, P1, and P2 must be -20mA max. The total I_{OH(peak)} for ports P3, P4 and P5 must be -40mA max. The total I_{OH(peak)} for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total I_{OH(peak)} for ports P8_6, P8_7 and P9 must be -40mA max. Set Average Output Current to 1/2 of peak.
4. Relationship between main clock oscillation frequency, and supply voltage.

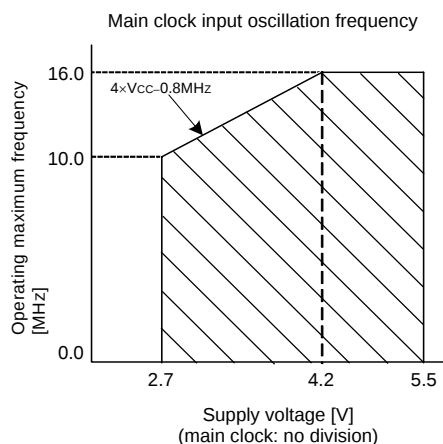


Table 5.3 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		VREF=VCC				10	Bits
INL	Integral Non-Linearity Error	10bit	VREF=VCC=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±5	LSB
			VREF=VCC=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±7	LSB
		8bit	VREF=VCC=3.3V				±2	LSB
–	Absolute Accuracy	10bit	VREF=VCC=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±5	LSB
			VREF=VCC=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input			±7	LSB
		8bit	VREF=VCC=3.3V				±2	LSB
–	Tolerance Level Impedance					3		kΩ
DNL	Differential Non-Linearity Error						±2	LSB
–	Offset Error						±5	LSB
–	Gain Error						±5	LSB
RLADDER	Ladder Resistance		VREF=VCC		10		40	kΩ
tCONV	10-bit Conversion Time, Sample & Hold Function Available		VREF=VCC=5V, ϕAD=10MHz		3.3			μs
tCONV	8-bit Conversion Time, Sample & Hold Function Available		VREF=VCC=5V, ϕAD=10MHz		2.8			μs
tsAMP	Sampling Time				0.3			μs
VREF	Reference Voltage				3.0		VCC	V
VIA	Analog Input Voltage				0		VREF	V

NOTES:

1. Referenced to $V_{CC}=AV_{CC}=V_{REF}=3.3$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified.
2. ϕ_{AD} frequency must be 10 MHz or less.
3. When sample & hold function is disabled, ϕ_{AD} frequency must be 250 kHz or more, in addition to the limitation in Note 2.
When sample & hold function is enabled, ϕ_{AD} frequency must be 1MHz or more, in addition to the limitation in Note 2.

Table 5.4 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_d(P-R)$	Time for Internal Power Supply Stabilization During Powering-On	$V_{CC}=2.7V$ to $5.5V$			2	ms
$t_d(R-S)$	STOP Release Time				1500	μs
$t_d(W-S)$	Low Power Dissipation Mode Wait Mode Release Time				1500	μs

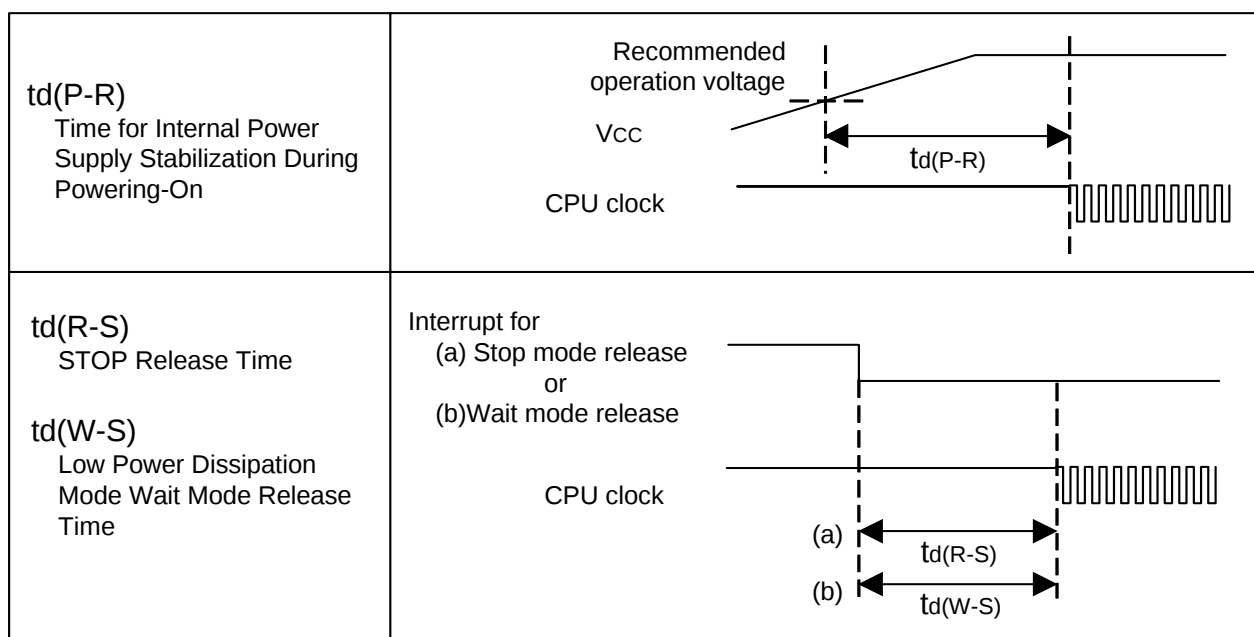


Figure 5.1 Power Supply Circuit Timing Diagram

$$V_{CC1}=V_{CC2}=5V$$

Table 5.5 Electrical Characteristics (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	IOH=−5mA	V _{CC} −2.0		V _{CC}	V
VOH	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	IOH=−200μA	V _{CC} −0.3		V _{CC}	V
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=−1mA	V _{CC} −2.0		V _{CC}	V
		LOWPOWER	IOH=−0.5mA	V _{CC} −2.0		V _{CC}	V
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		V
VOL	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	IOL=5mA			2.0	V
VOL	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	IOL=200μA			0.45	V
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	V
		LOWPOWER	IOL=0.5mA			2.0	V
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		V
VT+−VT−	Hysteresis	TA0IN to TA2IN, TB0IN to TB2IN, INT0 to INT4, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK2, TA0OUT to TA2OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2		0.2		1.0	V
VT+−VT−	Hysteresis	RESET		0.2		2.5	V
VT+−VT−	Hysteresis	XIN		0.2		0.8	V
I _{IH}	HIGH Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I =5V			5.0	μA
I _{IL}	LOW Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I =0V			−5.0	μA
R _{PULLUP}	Pull-Up Resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	V _I =0V	30	50	170	kΩ
R _{IXIN}	Feedback Resistance	XIN			1.5		MΩ
R _{IXCIN}	Feedback Resistance	XCIN			15		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V
I _{CC}	Power Supply Current (V _{CC1} =V _{CC2} =4.2V to 5.5V)	In single-chip mode, the output pins are open and other pins are V _{SS}	Mask ROM	f(XIN)=16MHz No division	10		mA
				f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾	25		μA
				f(XCIN)=32kHz Wait mode ⁽²⁾ , Oscillation capacity High	7.5		μA
				f(XCIN)=32kHz Wait mode ⁽²⁾ , Oscillation capacity Low	2.0		μA
				Stop mode T _{opr} =25°C	0.8	3.0	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = −20 to 85°C / −40 to 85°C, f(XIN)=16MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.6 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.7 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	40		ns

Table 5.8 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	200		ns

Table 5.9 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	100		ns

Table 5.10 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	100		ns

Table 5.11 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.12 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiN Input Setup Time	200		ns

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.13 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.14 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.15 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.16 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW Pulse Width	125		ns

Table 5.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.18 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	250		ns

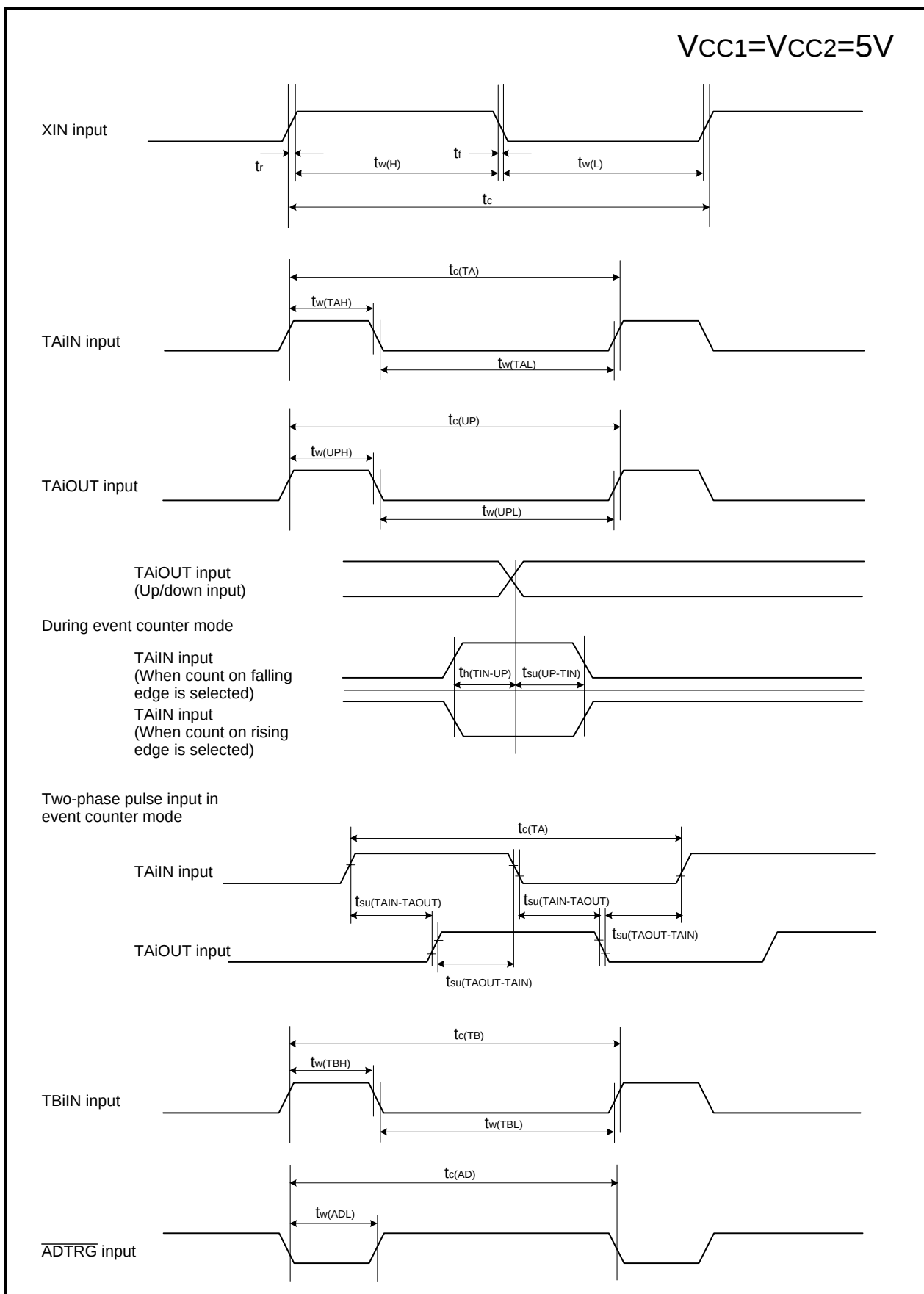


Figure 5.2 Timing Diagram (1)

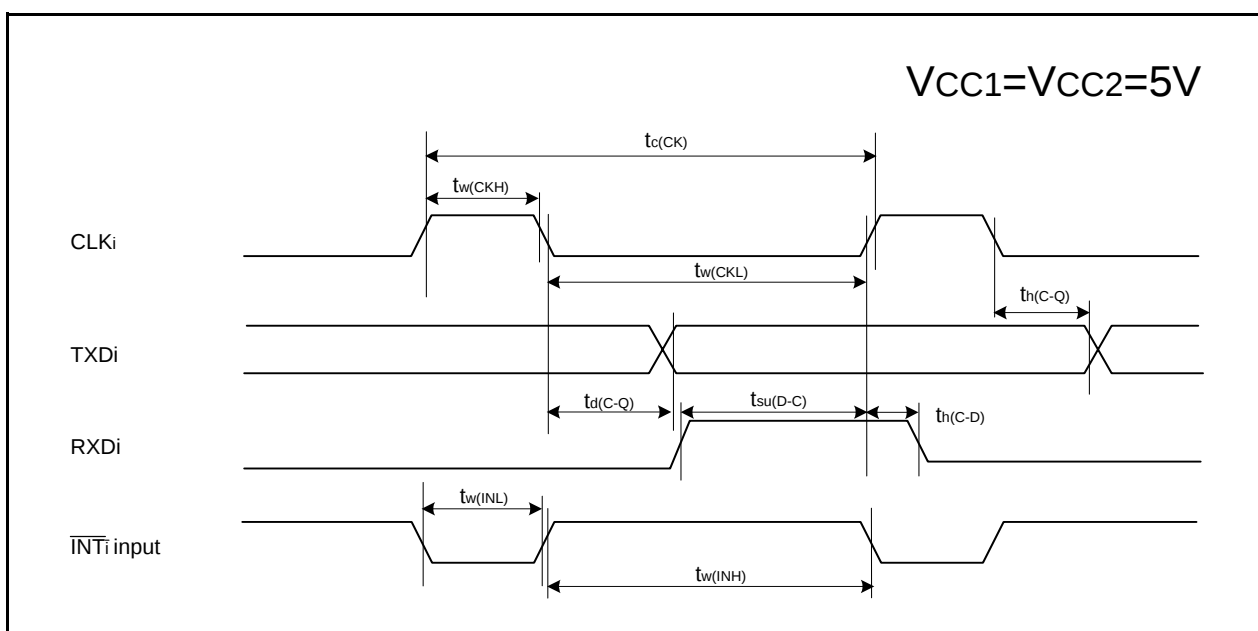


Figure 5.3 Timing Diagram (2)

$$V_{CC1}=V_{CC2}=3V$$

Table 5.19 Electrical Characteristics (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OH} =-1mA	V _{CC} -0.5		V _{CC}	V
V _{OH}	HIGH Output Voltage XOUT	HIGHPOWER	I _{OH} =-0.1mA	V _{CC} -0.5		V _{CC}	V
		LOWPOWER	I _{OH} =-50μA	V _{CC} -0.5		V _{CC}	V
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		V
V _{OL}	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} =1mA			0.5	V
V _{OL}	LOW Output Voltage XOUT	HIGHPOWER	I _{OL} =0.1mA			0.5	V
		LOWPOWER	I _{OL} =50μA			0.5	V
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		V
V _{T+} -V _{T-}	Hysteresis	TA0IN to TA2IN, TB0IN to TB2IN, INT0 to INT4, NMI, ADTRG, CTS0 to CTS2, RXD0 to RXD2, CLK0 to CLK2, TA0OUT to TA2OUT, KI0 to KI3, SCL0 to SCL2, SDA0 to SDA2		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2	(0.7)	1.8	V
V _{T+} -V _{T-}	Hysteresis	XIN		0.2		0.8	V
I _{IH}	HIGH Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I =3V			4.0	μA
I _{IL}	LOW Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I =0V			-4.0	μA
R _{PULLUP}	Pull-Up Resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	V _I =0V	50	100	500	kΩ
R _{I_{XIN}}	Feedback Resistance	XIN			3.0		MΩ
R _{I_{XCIN}}	Feedback Resistance	XCIN			25		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V
I _{CC}	Power Supply Current (V _{CC1} =V _{CC2} =2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are V _{SS}	Mask ROM	f(XIN)=10MHz, no wait No division		8	mA
				f(XCIN)=32kHz, Low power dissipation mode, ROM (3)		25	μA
				f(XCIN)=32kHz, Wait mode (2), Oscillation capacity High		7.0	μA
				f(XCIN)=32kHz, Wait mode (2), Oscillation capacity Low		1.8	μA
				Stop mode, T _{opr} =25°C		0.7	3.0 μA

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 3.3V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.20 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	100		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	40		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	40		ns
t_r	External Clock Rise Time		18	ns
t_f	External Clock Fall Time		18	ns

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.21 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	150		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	60		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	60		ns

Table 5.22 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	600		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	300		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	300		ns

Table 5.23 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	300		ns
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	150		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	150		ns

Table 5.24 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiN Input HIGH Pulse Width	150		ns
$t_{w(TAL)}$	TAiN Input LOW Pulse Width	150		ns

Table 5.25 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	3000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1500		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	600		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	600		ns

Table 5.26 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN Input Cycle Time	2		μs
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiN Input Setup Time	500		ns

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.27 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns

Table 5.28 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.29 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.30 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input LOW Pulse Width	200		ns

Table 5.31 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	150		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	150		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		160	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	100		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.32 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

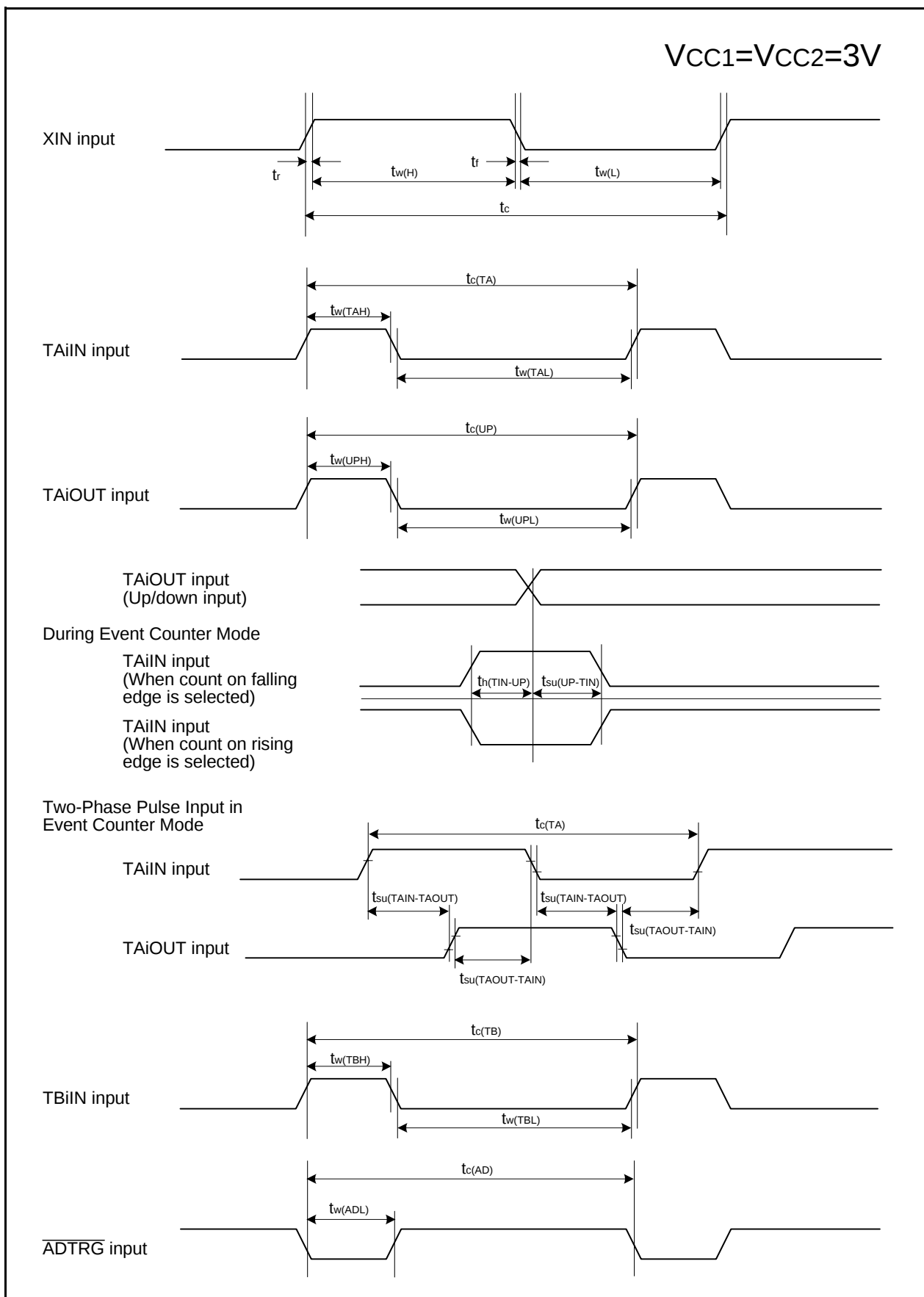


Figure 5.4 Timing Diagram (1)

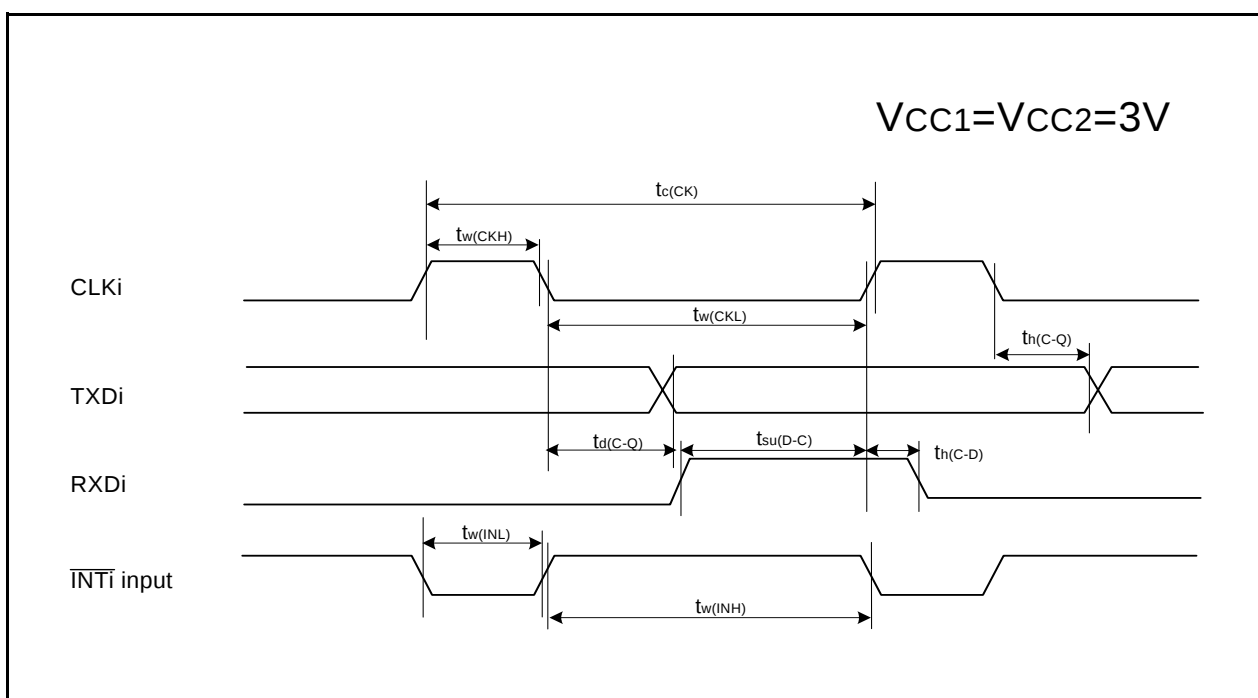


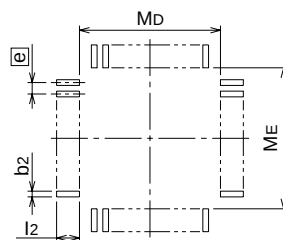
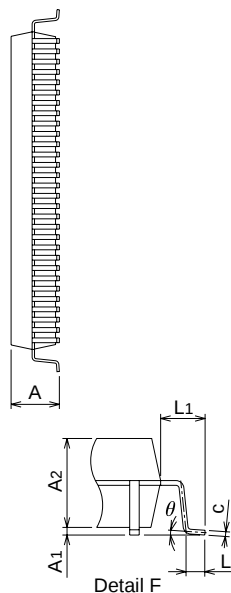
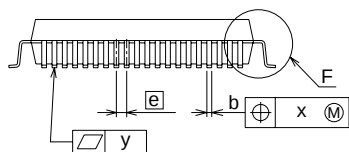
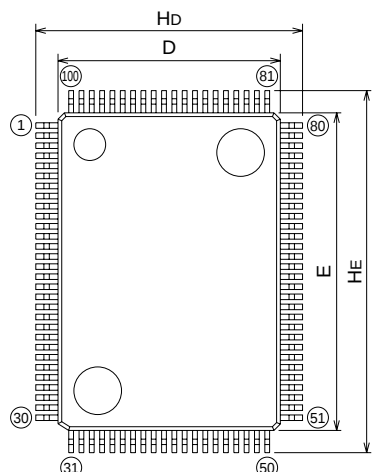
Figure 5.5 Timing Diagram (2)

Appendix 1. Package Dimensions

100P6S-A Recommended

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	—	1.58	Alloy 42



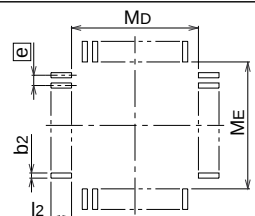
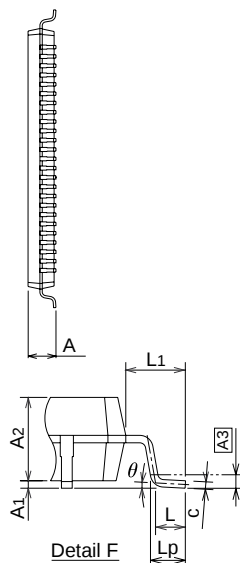
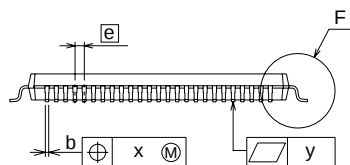
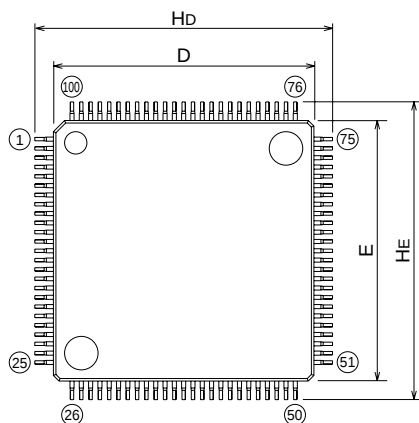
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.65	—
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	—	1.4	—
x	—	—	0.13
y	—	—	0.1
θ	0°	—	10°
b2	—	0.35	—
l2	1.3	—	—
Md	—	14.6	—
ME	—	20.6	—

100P6Q-A Recommended

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	—	0.63	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	—	0.5	—
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	10°
b2	—	0.225	—
l2	0.9	—	—
Md	—	14.4	—
ME	—	14.4	—

REVISION HISTORY	M16C/30P Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.70	Aug 26, 2004	–	First Edition issued
0.80	Mar 18, 2005	–	development support tools -> development tools
		–	BCLK -> CPU clock
		2	Table 1.1 Performance Outline of M16C/30P Group Serial interface is revised.
		4	Figure 1.2 Type., Memory Size, and Package is partly revised.
		8	Table 1.4 Pin Detection (2) is partly revised.
		20	Note 2 Table 5.3 A/D Conversion Characteristics is partly revised.
		21	Symbol of Table 5.4 Power Supply Circuit Timing Characteristics is partly revised.
		22	Table 5.5 Electrical Characteristics is revised.
		28	Table 5.19 Electrical Characteristics is revised.

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