

EC3600ETTS-40.000M TR

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REGULATORY COMPLIANCE (Data Sheet downloaded on Nov 26, 2017)


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ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVCMOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 40.000MHz ± 100 ppm -40°C to +85°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	40.000MHz
Frequency Tolerance/Stability	± 100 ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Operating Temperature Range	-40°C to +85°C
Supply Voltage	3.3Vdc $\pm 10\%$
Input Current	25mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	4nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 $\pm 10\%$ (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Pin 1 Connection	Tri-State (High Impedance)
Tri-State Input Voltage (Vih and Vil)	90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)
Standby Current	10 μ A Maximum (Disabled Output: High Impedance)
RMS Phase Jitter	1pSec Maximum (12kHz to 20MHz offset frequency)
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

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LINE	MARKING
1	E40.000 <i>E=Eclipsek Designator</i>
2	XXXXXX <i>XXXXXX=Eclipsek Manufacturing Identifier</i>

1-800-ECLIPTEK or 714.433.1200

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OUTPUT WAVEFORM & TIMING DIAGRAM



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Test Circuit for CMOS Output



Note 1: An external $0.1\mu F$ low frequency tantalum bypass capacitor in parallel with a $0.01\mu F$ high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance ($<12pF$), 10X attenuation factor, high impedance ($>10M\Omega$), and high bandwidth ($>300MHz$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

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Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

All Dimensions in Millimeters

Compliant to EIA-481

